SECTION III

Operation of the Am2900 Evaluation and Learning Kit

INTRODUCTION

The Am2900 Learning and Evaluation Kit design exemplifies the basic microprogrammed architecture of a typical minicomputer. The kit consists of a microprogram control section and a CPU. The microprogram control section contains most of the elements found in the microprogram control section of a typical computer control unit. All that need be added is an instruction register and op code mapping PROM. The CPU section of the kit contains a condition code register and shift matrix multiplexer linkage.

Toggle switches are used in the kit to control the clock select circuitry and to enter data into the microprogram memory. These toggle switches are also used to control the data display section selection points throughout the learning kit. The kit contains three LED display ports. One four-bit display is used in conjunction with the microprogram memory, the second LED display is used to view the contents of the pipeline register, and the third LED display is used to examine data at various points in the kit.

BLOCK DIAGRAM

A detailed block diagram of the Am2900 kit is shown in Figure 1. Basically, the left-hand side in the block diagram represents the microprogram control section and the right-hand side of the block diagram represents the CPU section. Likewise, various switches and multiplexers are shown in conjunction with the function described above. That is, address select switches, microprogram memory data switches, and RAM and MUX select switches are connected to the microprogram control section of the kit. Three separate LED displays are used to view the microprogram memory outputs, the pipeline register output, and the various data paths.

MICROPROGRAM SEQUENCER

One Am2909 Bipolar Microprogram Sequencer is used for the central control point for the microprogram memory. The output of the Am2909 Microprogram Sequencer represents the address of the next microinstruction to be executed. This four-bit address is applied to the four address lines of the microprogram memory. The microprogram memory consists of eight Am27S03 64-bit RAM's. These 64-bit RAM's are organized as a 16-word by 4-bit memory. Therefore, using eight of the Am27S03 Memories, a microprogram memory storage of 16 words by 32 bits is realized.

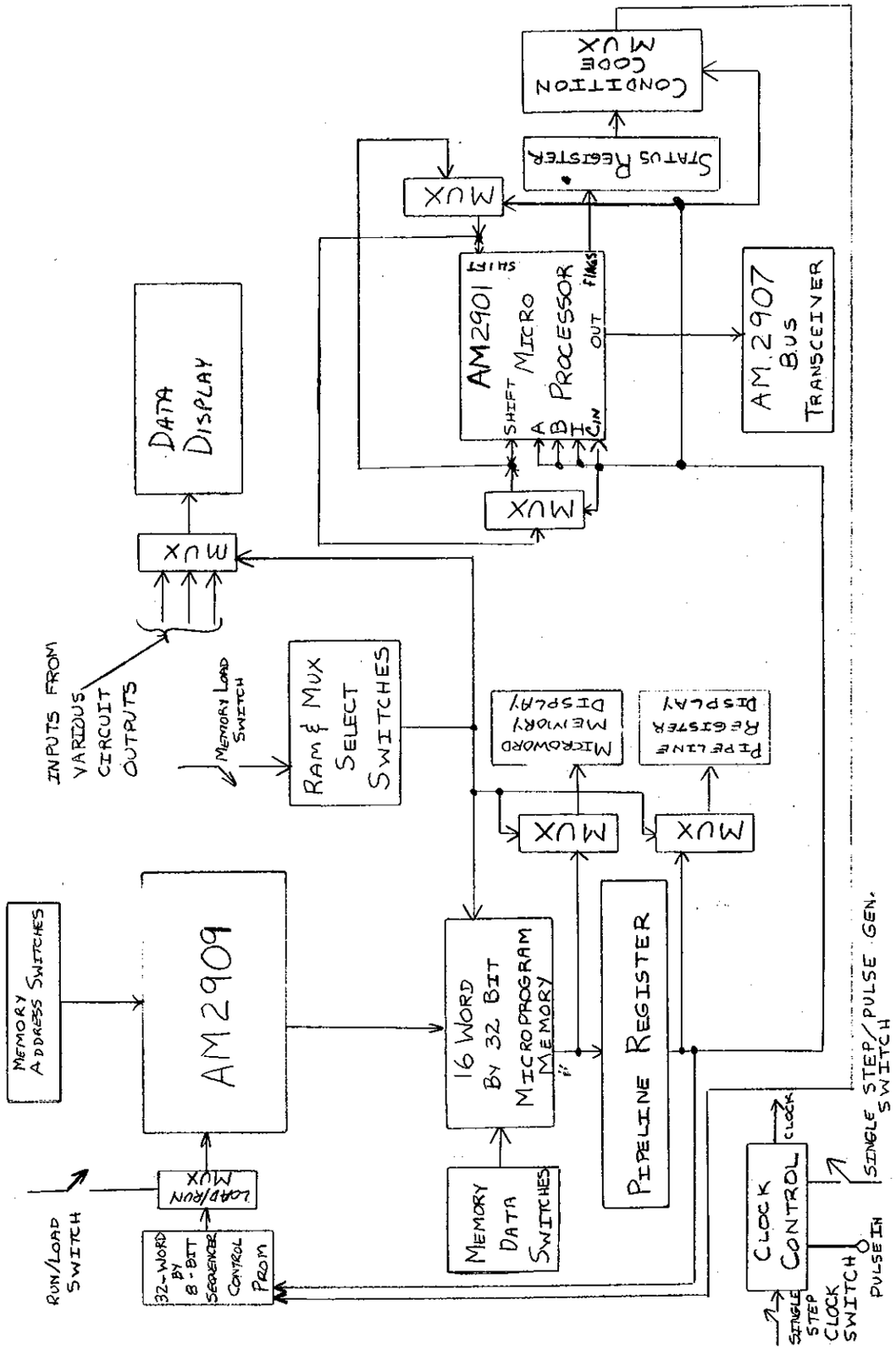

FIGURE 1: Block Diagram of the Am2900 Evaluation and Learning Kit

Four Am25LS151 eight-input Multiplexers are used at the output of the microprogram memory such that the RAM and MUX SELECT switches are used to view the contents of the RAM on the microprogram memory LED display. Thus, the user can examine the contents of each Am27S03 four bits at a time.

Eight Am2918 Four-bit Registers are used at the output of the microprogram memory to form a 32-bit pipeline register. The pipeline register contains the microinstruction currently being executed. This instruction consists of the two parts described previously. That is, the pipeline register provides the various signals to control the Am2901 and the associated shift matrix multiplexer. It also provides the necessary control signals for selecting the address of the next microinstruction. These signals include the control inputs to the Am29751 PROM and a four-bit branch address field.

The field definition for the pipeline register bits is shown in Figure 2. The definition is as follows:

Bit Position	Description
0-3	Am2901 Data Input
4-7	Am2901 B Address
8-11	Am2901 A Address
12-14	ALU Function
15	Am2901 Carry Input
16-18	Am2901 Source Operand Select
19	Am25LS253 Shift Matrix A Input (MUX_0)
20-22	Am2901 Destination Control
23	Am25LS253 Shift Matrix B Input (MUX_1)
24-27	Next Microinstruction Address Select Control
28-31	Microprogram Branch Address

The above definition shows 24 of the bits in the pipeline register are used to control the CPU section of the machine and 8 bits of the pipeline register are used for next microinstruction address control. It should be remembered that when the microprogram memory is being loaded with data, it is being loaded four bits at a time. The heavy lines in Figure 2 show the breakout of the four fields for each of the possible binary positions of the RAM and MUX SELECT switch positions. Thus, the microprogram memory is loaded four bits at a time across the eight individual fields associated with each microprogram memory word.

The next microinstruction address control four-bit field is used to select the source of the next microinstruction. This source may allow for a conditional address or an unconditional address select. The definition of the four-bit field associated with the Am2900 Evaluation and Learning Kit is shown in Figure 3. Here, the four-bit instruction field associated with the PROM is P_3, P_2, P_1, and P_0, where $P_0 = A_1$, $P_1 = A_2$, $P_2 = A_3$, and $P_3 = A_4$. The condition code enable bit controls the A_0 input to the PROM. If both the A_0 and $\overline{A_0}$ inputs contain the same address selection, the next address is unconditional. If the A_0 and $\overline{A_0}$ inputs point to different sources for the next address selection, the source of the next microinstruction address is conditional.

Microprogram Memory Field Definition

RAM & MUX SELECT	7				6				5				4				3				2				1				0			
RAM LOCATION	U9				U7				U8				U6				U5				U4				U3				U2			
BIT NUMBER	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT DEFINITION	BR_3	BR_2	BR_1	BR_0	P_3	P_2	P_1	P_0	MUX$_1$	I_8	I_7	I_6	MUX$_0$	I_2	I_1	I_0	C_n	I_5	I_4	I_3	A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	D_3	D_2	D_1	D_0
FIELD DEFINITION	BRANCH ADDRESS				NEXT MINSTRUCTION CONTROL				MUX$_1$	DESTINATION CONTROL			MUX$_0$	SOURCE SELECT			C_n	ALU			"A"				"B"				"D"			

FIGURE 2: Definition of the Field of the 32-bit Microprogram Memory Word

Am2909 Next Address Control PROM

Binary Code	$P_3P_2P_1P_0$	Function
0	0 0 0 0	Branch Register if F≠0
1	0 0 0 1	Branch Register
2	0 0 1 0	Continue
3	0 0 1 1	Branch Map (D Switches)
4	0 1 0 0	Jump-to-Subroutine if F≠0
5	0 1 0 1	Jump-to-Subroutine
6	0 1 1 0	Return-from-Subroutine
7	0 1 1 1	File Reference
8	1 0 0 0	End Loop & Pop if F=0
9	1 0 0 1	Push (and continue)
10	1 0 1 0	Pop (and continue)
11	1 0 1 1	End Loop & Pop if C_{n+4}
12	1 1 0 0	Branch Register if F=0
13	1 1 0 1	Branch Register if F_3
14	1 1 1 0	Branch Register if OVR
15	1 1 1 1	Branch Register if C_{n+4}

FIGURE 3: Instructions in the Am29751 Next Address Control PROM Supplied in the Am2900 Kit

It is this set of instructions defined in Figure 3 that is contained in the Am29751 PROM. This PROM is installed in the kit assembly in a socket (U27) such that the user can define different microinstruction source select control sets and install other PROM's in this position. The actual coding for the PROM is shown in Figure 4.

CENTRAL PROCESSOR UNIT (CPU)

The heart of the CPU section in the Am2900 Evaluation and Learning Kit is the Am2901 Four-bit Microprocessor Slice. This device contains a 16-word by 4-bit, 2-port RAM, a high-speed ALU, and the associated shifting, decoding, and multiplexing circuitry required by a high-speed cascadable element. A nine-bit micro-instruction word is used to control the various functions of the device. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. While the Am2900 Evaluation and Learning Kit contains only one Am2901, the Microprocessor Slice is cascadable with full lookahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU.

SHIFT MATRIX CONTROL

Referring to the block diagram of Figure 1, the Am2901 Microprocessor uses multiplexers at the four bi-directional shift data pins. The most significant bit or least significant bit data transfers occur over these lines when the device is in the shift mode. The Am2900 Evaluation and Learning Kit uses two Am25LS253 Multiplexers to perform this function. The Am25LS253 Multiplexer select input (A and B) are controlled from the pipeline register MUX_0 and MUX_1 control bits. Thus, the multiplexer can perform four different functions. These include enter zeros, single length rotate, double length rotate, and arithmetic shift. These four functions can be performed in either the shift left mode or shift right mode of operation as shown in the coding table of Figure 5.

STATUS REGISTER

The status register in the Am2900 Evaluation and Learning Kit utilizes an Am25LS08 Four-bit Register with clock enable. The status register is used to store the four status flags on the Am2901 Microprocessor. These status flags are the carry output, overflow, zero detect, and sign bit.

The Am25LS08 Register clock enable function is used to hold the data in the status register during conditional tests. Thus, whenever the microprogram control function is a conditional test on one of the bits in the status register, the clock enable input is brought HIGH so the Am25LS08 Register will retain the current status word. This allows sequential testing of all four status bits in the Am2900 kit. Control for the clock enable input to the register comes from the Am29751 Microprogram Sequencer Control PROM.

Next μ Instruction Code	CCE	MUX Select	File	OR	Status Register
0	0	Reg	Inhibit	Low	Inhibit
	1	PC			
1	0	Reg	Inhibit	Low	Enable
	1				
2	0	PC	Inhibit	Low	Enable
	1				
3	0	D	Inhibit	Low	Enable
	1				
4	0	Reg	Enable &Push	Low	Inhibit
	1	PC	Inhibit		
5	0	Reg	Enable &Push	Low	Enable
	1				
6	0	File	Enable & Pop	Low	Enable
	1				
7	0	File	Inhibit	Low	Enable
	1				
8	0	File	Inhibit	Low	Inhibit
	1	PC	Enable & Pop		
9	0			Low	
	1	PC	Enable & Push		Enable
10	0	PC	Enable & Pop	Low	Enable
	1				
11	0	File	Inhibit	Low	Inhibit
	1	PC	Enable & Pop		
12	0	PC	Inhibit	Low	Inhibit
	1	Reg			
13	0	PC	Inhibit	Low	Inhibit
	1	Reg			
14	0	PC	Inhibit	Low	Inhibit
	1	Reg			
15	0	PC	Inhibit	Low	Inhibit
	1	Reg			

Figure 4A

Function Definition of Am29751
Next Microinstruction Control PROM

Next μInstruction Code	PROM Address $A_4A_3A_2A_1A_0$	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
0	0 0 0 0 0	1	0	0	0	1	0	1	X
	0 0 0 0 1	1	0	0	0	0	0	1	X
1	0 0 0 1 0	0	0	0	0	1	0	1	X
	0 0 0 1 1	0	0	0	0	1	0	1	X
2	0 0 1 0 0	0	0	0	0	0	0	1	X
	0 0 1 0 1	0	0	0	0	0	0	1	X
3	0 0 1 1 0	0	0	0	0	1	1	1	X
	0 0 1 1 1	0	0	0	0	1	1	1	X
4	0 1 0 0 0	1	0	0	0	1	0	0	1
	0 1 0 0 1	1	0	0	0	0	0	1	X
5	0 1 0 1 0	0	0	0	0	1	0	0	1
	0 1 0 1 1	0	0	0	0	1	0	0	1
6	0 1 1 0 0	0	0	0	0	0	1	0	0
	0 1 1 0 1	0	0	0	0	0	1	0	0
7	0 1 1 1 0	0	0	0	0	0	1	1	X
	0 1 1 1 1	0	0	0	0	0	1	1	X
8	1 0 0 0 0	1	0	0	0	0	1	1	X
	1 0 0 0 1	1	0	0	0	0	0	0	0
9	1 0 0 1 0	0	0	0	0	0	0	0	1
	1 0 0 1 1	0	0	0	0	0	0	0	1
10	1 0 1 0 0	0	0	0	0	0	0	0	0
	1 0 1 0 1	0	0	0	0	0	0	0	0
11	1 0 1 1 0	1	0	0	0	0	1	1	X
	1 0 1 1 1	1	0	0	0	0	0	0	0
12	1 1 0 0 0	1	0	0	0	0	0	1	X
	1 1 0 0 1	1	0	0	0	1	0	1	X
13	1 1 0 1 0	1	0	0	0	0	0	1	X
	1 1 0 1 1	1	0	0	0	1	0	1	X
14	1 1 1 0 0	1	0	0	0	0	0	1	X
	1 1 1 0 1	1	0	0	0	1	0	1	X
15	1 1 1 1 0	1	0	0	0	0	0	1	X
	1 1 1 1 1	1	0	0	0	1	0	1	X

X = Don't Care

FIGURE 4B: PROM Code for the Next Microinstruction Control PROM in the Am2900 Kit

CODE	MUX_1 MUX_0	UP	DOWN
0	0 0	ZERO	ZERO
1	0 1	ROTATE	ROTATE
2	1 0	DOUBLE LENGTH ROTATE	DOUBLE LENGTH ROTATE
3	1 1	DOUBLE LENGTH ARITHMETIC "0" → Q_0	DOUBLE LENGTH ARITHMETIC F_3 → RAM_3

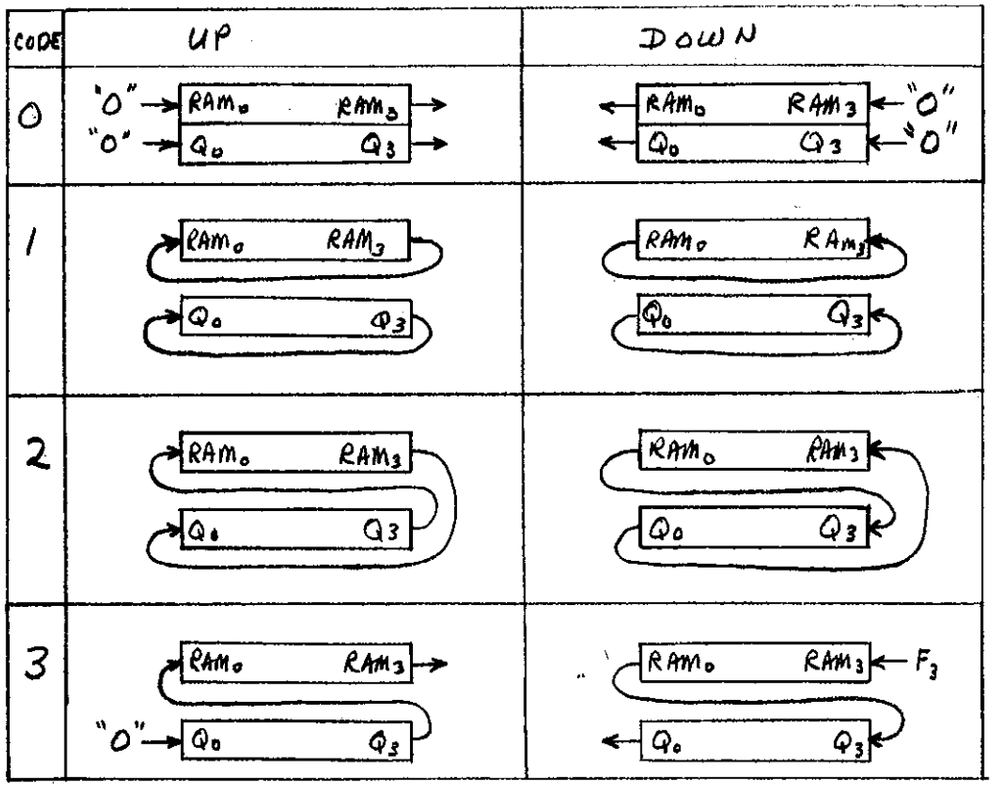

FIGURE 5: Definition of the Shift Matrix Multiplexer Control Functions

The outputs of the Am25LS08 Status Register drive an Am9309 Four-input Multiplexer. This allows one of the four status register bits to be selected at the multiplexer output as the condition code enable (CCE) input. In the Am2900 Kit, the Am9309 Four-input Multiplexer select inputs are controlled from the pipeline register. The actual control signals used are the two least significant bits of the next address control field associated with the Am29751 Microsequencer Control PROM. This allows the condition code multiplexer select inputs to share the same field as the next address control field for the microprogram sequencer.

DETAILED DESCRIPTION OF SWITCH AND DISPLAY FUNCTIONS

RAM and MUX SELECT Switches

Three toggle switches (S1, S2, S3) are used to implement the RAM and MUX SELECT control. They can access eight different fields which we will refer to as binary 0 through binary 7. The RAM and MUX SELECT switches control the three 4-bit LED displays as well as the select of an Am27S03 Microprogram Memory. Figure 2 shows the RAM location, bit definition, and the field definition for the eight RAM and MUX SELECT switch positions associated with the Random Access Memories of the pipeline register. Figure 6 shows the definition of the eight fields associated with the data display LED's as controlled by the RAM and MUX SELECT switches.

MEMORY ADDRESS Switches

The MEMORY ADDRESS switches are used to select one of the sixteen possible addresses of the microprogram memory. These MEMORY ADDRESS switches (S8, S9, S10, and S11) are used to select memory words binary 0 through binary 15. The switches connect to the D inputs of the Am2909 Microprogram Sequencer and are enabled by forcing the Am2909 internal multiplexer to select the D input. This is accomplished using the RUN/LOAD switch to be described later. Note the Am29751 PROM must be installed to inhibit OR_0, OR_1 and OR_2 from overriding MEMORY ADDRESS switches.

MEMORY DATA Switches

The MEMORY DATA switches provide the control of the individual data bits to be written into the microprogram memory. These MEMORY DATA switches (S4, S5, S6, and S7) are connected to the data inputs of the Am27S03 RAM's. Since the Am27S03 RAM's invert the data from data-in to data-out, the MEMORY DATA switches are connected such that the opposite polarity is applied to the RAM's. That is, when the MEMORY DATA switches are in the binary 0 position (pointing toward the bottom of the PC board) they apply a high logic level to the inputs to the Am27S03 RAM's. Thus, when this data is loaded into the RAM's, it will appear at the RAM output as a logic LOW level. This results in correctly entering binary 0 when the MEMORY DATA switches are in the binary 0 position.

The actual data entered into the data fields can be thought of in several different numbering schemes. For example, the A and B address fields for the Am2901 might be thought of in a hexidecimal format. These fields might also be considered to be a binary format. Data entered into the field connected to the data inputs of the Am2901 might be considered to be two's complement data or magnitude only data. Fields associated with the ALU, source operand selection and destination control might be thought of as octal represented fields. Other fields such as carry-in may be thought of as a single bit field having the capability of supplying only a logic zero or a logic one.

The following table is included for users not familiar with the standard binary number representations. This table shows the most commonly used representations for the various number schemes that are useful when using this kit.

RAM & MUX Select Switch	Data Display LED Lamps 8	4	2	1	Function
0	Y_3	Y_2	Y_1	Y_0	Am2909 Output
1	μP_3	μP_2	μP_1	μP_0	Am2901 Output
2	C_{n+4}	OVR	F_3	F=0	Am2901 Flags
3	Parity	CCE	$\overline{P}$	$\overline{G}$	Miscellaneous
4	ST_3	ST_2	ST_1	ST_0	Status Register
5	Q_0	Q_3	RAM_0	RAM_3	Am2901 Shift
6	BUS_3	BUS_2	BUS_1	BUS_0	Am2907 Bus
7	R_3	R_2	R_1	R_0	Am2907 Receiver

FIGURE 6: The DATA DISPLAY Field Definition as a Function of the RAM and MUX SELECT Switch Position

BINARY CODE REPRESENTATIONS

Code	Decimal	Octal	Hexidecimal	Two's Complement
0000	0	0	0	0
0001	1	1	1	1
0010	2	2	2	2
0011	3	3	3	3
0100	4	4	4	4
0101	5	5	5	5
0110	6	6	6	6
0111	7	7	7	7
1000	8	10	8	-8
1001	9	11	9	-7
1010	10	12	A	-6
1011	11	13	B	-5
1100	12	14	C	-4
1101	13	15	D	-3
1110	14	16	E	-2
1111	15	17	F	-1

MEMORY LOAD Switch

The MEMORY LOAD switch (S14) is a momentary switch used to load data into the Am27S03 Microprogram Memories. Each time the MEMORY LOAD switch is depressed, data from the MEMORY DATA switches will be loaded into the address selected by the MEMORY ADDRESS switches of the memory field selected the RAM and MUX SELECT switches. For this to occur, the RAM/LOAD SELECT switch must be in the LOAD position.

RUN/LOAD Switch

The RUN/LOAD SELECT switch (S12) is used to control the basic loading of the microprogram in memory. When the RUN/LOAD switch is in the LOAD position, the MEMORY LOAD switch can be used to enter data into the microprogram memory. When the RUN/LOAD switch is in the RUN position, the MEMORY LOAD switch is inhibited and the microprogram sequencer control PROM (U27) is enabled. Thus, the Am2900 Evaluation and Learning Kit will be in the "Operate" mode. The kit will now perform all of its functions using either the SINGLE STEP CLOCK or the CLOCK PULSE GENERATOR.

SINGLE STEP CLOCK Switch

The SINGLE STEP CLOCK switch (S15) is used to generate a clock pulse for the Am2900 Evaluation and Learning Kit. This clock pulse is applied to all clocked devices in the kit. That is, the clock pulse is applied to the Am2901, Am2909, status register, and pipeline register. The SINGLE STEP CLOCK switch is a momentary

switch that generates one clock pulse each time it is depressed. The switch is debounced using an Am9314 Latch. This ensures that one and only one clock pulse will be applied to the system for each depression of the SINGLE STEP CLOCK switch.

It is important to understand that the SINGLE STEP CLOCK switch is enabled when the RUN/LOAD switch is in the LOAD position. That is, when the microprogram memory is being loaded, the contents of the memory can be clocked into the pipeline register and executed in the Am2901 Microprocessor. This is a very useful feature for loading data into the RAM inside the Am2901.

When the SINGLE STEP/PULSE GEN switch (S13) is in the PULSE GEN mode, the SINGLE STEP CLOCK switch is inhibited and does not affect the clock input to the kit.

SINGLE STEP/PULSE GENERATOR SELECT Switch

The SINGLE STEP/PULSE GEN switch is used to select the source of the clock pulse for the Am2900 Evaluation and Learning Kit. The clock input can either be the SINGLE STEP CLOCK switch (S15) or can come from an external pulse generator. If an external pulse generator is used, it is attached to the PULSE GEN terminals at the R9 position. The pulse generator coax cable shield should be attached to the terminal closest to the bottom of the board and the pulse generator center wire should be attached to the terminal closest to the top of the board. The terminal closest to the bottom of the board is connected to ground in the Am2900 Evaluation and Learning Kit.

CLOCK TEST Turret Terminal

A turret terminal labeled CLOCK TEST is soldered into the center left-hand side of the printed circuit board. This terminal connects directly to the clock line of the Am2900 Evaluation and Learning Kit. This test point is supplied as a convenient test output for connection of an oscilloscope when using the kit with a pulse generator. This test point represents the actual clock signal applied to the Am2901 Microprocessor and Am2909 Microprogram Sequencer as well as the remainder of the kit registers.

SYNC TEST Turret Terminal

The SYNC TEST test point is connected directly to the carry output of the incrementer in the Am2909 Microprogram Sequencer. This test point is intended to be used as a convenient sync point in evaluating microprogram sequences. The limitation of using this point, of course, is that the microprogram must be written so that binary 15 of the microprogram memory addresses is used only once. The result is that a sync pulse will be generated each time the microprogram sequencer address outputs is binary 15. From this discussion,

it can be seen that if the user wishes to provide a sync pulse, he can branch in microprogram control from the current address to address 15 and then branch back. This will generate a SYNC pulse at the desired time.

Thus, if the Am2900 Evaluation and Learning Kit is programmed properly, the SYNC TEST turret test pint can be used to provide synchronization to an oscilloscope.

V_{CC} and GROUND Turret Inputs

The V_{CC} and GND inputs are used to apply power to the Am2900 Evaluation and Learning Kit. The V_{CC} terminal should be connected to the +5 volt connection of a 5 volt power supply capable of delivering 2 amps of current. The GND terminal should be connected to the Ground terminal of the +5 volt power supply. Needless to say, if these terminals are accidentally reversed, many of the integrated circuits in the kit will probably be destroyed. Therefore, the user should take particular care in connecting the power supply to the kit.

ADDRESS SYNC TURRET TERMINAL

A turret terminal labeled ADDRESS SYNC is soldered into the lower left-hand corner of the printed circuit board. This terminal connects directly to the A = B output of an Am9324 Comparator. The purpose of this test point is to provide a synchronization or reference signal for the microprogram address field when using the kit with conjunction with an oscilloscope. Four bits of one comparator input field are connected to the MEMORY ADDRESS switches. The other four-bit field of the comparator is connected to the Am2909 Y output field. In this manner, the MEMORY ADDRESS switches can be used to select the microprogram address at which a sync pulse or reference pulse is provided. This provides a handy signal for use as a reference trace on the oscilloscope.

PROGRAMMING GUIDE

A handy programming guide defining the functions of the various control fields in the 32-bit microprogram word is given in Figure 7. This figure defines the five different control fields of the microprogram word. These fields include the ALU, the ALU source operand, the ALU destination, the shift array multiplexer, and the next microinstruction control fields. These five fields make up 15 bits of the microprogram memory word.

Seventeen bits of the microprogram memory word are used to provide undecoded control. These include the four-bit data field, the four-bit A address field, the four-bit B address field, the four-bit branch address field, and the carry input. In these five cases, the binary value in the field represents the binary value required for control.

The user will find the programming guide of Figure 7 a most useful tool in programming the kit. Therefore, it is recommended that the user become very familiar with this guide and all the various functions it represents.

ALTERNATE NEXT INSTRUCTION PROM

The Am2900 Evaluation and Learning Kit is designed such that a next address PROM can be used in conjunction with the OR inputs. While this technique does not demonstrate all the capability of conditional OR branching, it does allow the kit user to experiment with the OR inputs. Figure 8 shows the next address select control functions and Figure 9 shows the PROM coding for an Am27LS09 PROM with OR branching. When using such an alternate PROM with the Am2900 Evaluation and Learning Kit, the user should remember the initialization problem. That is, when power is applied to the Am2900 Kit, the status register, pipeline register and microprogram memory can turn on in either the logic 1 or logic 0 state. Thus, some of the Am2909 outputs may be forced HIGH due to the OR inputs. When the RUN/LOAD select switch is placed in the load position, it is possible for the address select switches to be overridden by the OR inputs. Therefore, when power is initially applied to the Am2900 kit, an initialization procedure is required. The recommended procedure is to place the memory address select switches to the binary 15 position and use this word in microprogram memory to clear the Am2909 next address control function such that the Am27LS09 PROM cannot conditionally force any of the OR inputs HIGH. This word should be loaded into the pipeline register using the SINGLE STEP CLOCK momentary switch. Now, the microprogram memory can be loaded in the normal fashion. In fact, an initialization procedure may be required each time a new program is loaded. If data is to be entered in the Am2901 to initialize the RAM inside the four-bit microprocessor slice, microprogram memory word binary 15 should be used for this function. Then, the user does not have to worry about the conditions of the various flags in the status register.

Am2909 Next Address Control

CODE	FUNCTION
0	BRANCH
1	CONTINUE
2	PUSH
3	POP
4	JUMP - SUBROUTINE
5	RETURN - SUBROUTINE
6	FILE REFERENCE
7	JUMP D
8	END LOOP, F=0
9	END LOOP, F_3
10	END LOOP, OVR
11	END LOOP, C_{n+4}
12	BRANCH, F=0
13	BRANCH, " F_3
14	BRANCH, OVR
15	BRANCH, C_{n+4}

NOTE: CODE IS DECIMAL EQUIVALENT OF BINARY

ALU Function Select

CODE	FUNCTION
0	R plus S
1	S minus R
2	R minus S
3	R OR S
4	R AND S
5	$\overline{R}$ AND S
6	R EX-OR S
7	R EX-NOR S

Source Operand Select

CODE	R	S
0	A	Q
1	A	B
2	O	Q
3	O	B
4	O	A
5	D	A
6	D	Q
7	D	O

Destination Select

CODE	LOAD	Y Output
0	F→Q	F
1	NONE	F
2	F→ RAM	A
3	F→ RAM	F
4	F/2 → RAM; Q/2 → Q	F
5	F/2 → RAM	F
6	2F → RAM; 2Q → Q	F
7	2F → RAM	F

F = ALU OUTPUT

MUX_0, MUX_1 Control

CODE	UP	DOWN
0	ZERO	ZERO
1	ROTATE	ROTATE
2	DOUBLE LENGTH ROTATE	DOUBLE LENGTH ROTATE
3	ARITHMETIC (DOUBLE LENGTH ZERO → RAM_0	ARITHMETIC (DOUBLE LENGTH F_3 → RAM_3

FIGURE 7: Programming Guide for the Am2900 Evaluation and Learning Kit

ALTERNATE NEXT ADDRESS PROM

Binary Code	$P_3P_2P_1P_0$	Function
0	0000	Continue
1	0001	PUSH (and continue)
2	0010	POP (and continue)
3	0011	Jump Register if C_{n+4}
4	0100	Jump-to-Subroutine
5	0101	Return-from-Subroutine
6	0110	Jump Register
7	0111	End Loop and POP if C_{n+4}
8	1000	Jump Register if F=0
9	1001	Jump Register if F_3
10	1010	File Reference
11	1011	Jump D
12	1100	Force OR3 if F=0
13	1101	Force OR2 if F_3
14	1110	Force OR1 if OVR
15	1111	Force OR_0 if C_{n+4}

FIGURE 8: Alternate Next Address PROM Instructions

Next Microinstruction Code	PROM Address	O_7 O_6 O_5 O_4 O_3 O_2 O_1 O_0
0	00000	0 0 0 0 0 0 1 X
	00001	0 0 0 0 0 0 1 X
1	00010	0 0 0 0 0 0 0 1
	00011	0 0 0 0 0 0 0 1
2	00100	0 0 0 0 0 0 0 0
	00101	0 0 0 0 0 0 0 0
3	00110	1 0 0 0 0 0 1 X
	00111	1 0 0 0 1 0 1 X
4	01000	0 0 0 0 1 0 0 1
	01001	0 0 0 0 1 0 0 1
5	01010	0 0 0 0 0 1 0 0
	01011	0 0 0 0 0 1 0 0
6	01100	0 0 0 0 1 0 1 X
	01101	0 0 0 0 1 0 1 X
7	01110	1 0 0 0 1 0 1 X
	01111	1 0 0 0 0 0 0 0
8	10000	1 0 0 0 0 0 1 X
	10001	1 0 0 0 1 0 1 X
9	10010	1 0 0 0 0 0 1 X
	10011	1 0 0 0 1 0 1 X
10	10100	0 0 0 0 0 1 1 X
	10101	0 0 0 0 0 1 1 X
11	10110	0 0 0 0 1 1 1 X
	10111	0 0 0 0 1 1 1 X
12	11000	1 0 0 0 0 0 1 X
	11001	1 1 0 0 0 0 1 X
13	11010	1 0 0 0 0 0 1 X
	11011	1 0 0 0 0 0 1 X
14	11100	1 0 0 0 0 0 1 X
	11101	1 0 1 0 0 0 1 X
15	11110	1 0 0 0 0 0 1 X
	11111	1 0 0 1 0 0 1 X

FIGURE 9: Alternate Next Address PROM Coding