

**Q20000 SERIES
RAPID REFERENCE
AND QUICK START**

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1 Q20000 Rapid Reference and Quick Start

1.1 Introduction

This document is not intended as a replacement for the Q20000 Series Design Manual, class note set or Design Guide. It is intended to provide the designer with a compact cross-reference to the tables for all bipolar arrays in the Q20000 Series to allow design decisions affecting the selection of an array within the series. These decisions include operating speed, sizing, population, macro options, maximum current, power, packaging, loading and fan-out limits.

The assumption is that the designer has previously reviewed:

- ◆ The Design Manual for the Q20000 Series Arrays, Vol I, all sections.
- ◆ The Design Submission Document Design Manual Vol II, Section 6.
- ◆ AMCC EWS Schematic Rules and Conventions Design Manual Vol II, Section 3 and Section 7.
- ◆ AMCC Vector Submission Rules and Guidelines Design Manual Vol II, Section 4.
- ◆ Bipolar/BiCMOS Design Validation Design Manual Vol II, Section 5.

1.2 Equivalent Gates - Relative Sizing

The number of equivalent gates possible is a sizing measure for the AMCC logic arrays, used to gauge the relative sizes of different arrays. An equivalent gate is loosely defined as a 2-input NOR gate for the bipolar arrays. A measure of design density is the number of these gates that would be required to construct the design in SSI logic.

To estimate the equivalent gate counts for the Q20000 Series arrays, a 3:1 MUX with a D F/F is defined as 11 gates and a full adder as 16 gates. The number of cells required for each of these macros and the number of cells available on the array lead to the equivalent gate count.

An I/O cell can be estimated as 2 gates but is not included in either of the gate counts shown below.

Table 1-1 Sizes of the AMCC Q20000 Bipolar Arrays in Equivalent Gates

ARRAY NAME	MUX F/F METHOD	Full Adder METHOD
Q20120	12700	17800
Q20080	8000	11000
Q20045	4500	6300
Q20P025	2150	3000
Q20025	2700	3800
Q20P010	650	900
Q20010	1000	1400

Note: There is no ERC check for equivalent gates. Equivalent gate counts may not be used in sizing for design submission.

1.2.1 Circuit Density

The actual circuit density obtained is a function of the design objectives, design approach and macros selected. The Q20000 Series uses 3-level series gating to maximize the logic density per switch.

A denser design is possible if the more complex macros are used first - start with cell-efficient, dense macros - keeping the use of SSI-level AND, OR, NOR, NAND gates to a minimum. Designs with balanced delay path requirements use more cells than a minimized design; high-speed designs may use more cells if heavily loaded paths are to be broken up into parallel structures.

1.3 Maximum Operating Frequency

The actual speed at which a circuit may operate must be computed from a worst-case maximum critical-path timing analysis and must include the intrinsic macros delays (specified as "Tpd" in the macro documentation) and the extrinsic loading delays as computed using Front-Annotation (estimate) or Back-Annotation (specification).

For I/O macros, the toggle frequency should be documented via the AMCCANN user interface. AMCCANN produces AMCCPKG.LST. Document TTL running faster than 50MHz and all ECL over 400 MHz. Documenting 200MHz is preferred.

The maximum operating frequency is specified as the maximum I/O switching rate for an I/O macro or the maximum internal toggle rate for an internal macro.

1.4 Maximum Operating Frequency For All Q20000 Series Libraries

Table 1-2 List TTL I/O Frequencies via AMCCANN when > 50 MHz

	OPTION	fmaxinMHz	PWinns	Comments
TTL INPUT	L	30	14.0	
	S	60	7.0	
	H	100	4.2	
TTL OUTPUT	L	20	20.0	
	S	45	9.0	
	H	90	4.5	

Table 1-3 List ECL Input Frequencies via AMCCANN when > 400MHz

	OPTION	fmaxinMHz	PWinns	Comments
ECL INPUT*	S	600	0.65	Single ended
	H	800	0.50	differential
	D***	1.2GHz	0.38	differential

* Maximum frequency may be limited by specific package selection.

Table 1-4 List ECL Output Frequencies via AMCCANN when > 400MHz

	OPTION	Fmaxin MHz	PWin ns	Comments
ECL OUTPUT*		350	1.15	Single ended
-standard		800	0.50	differential
-on-chip series termination:		250		
-Darlington*		600	0.65	
-CML.**		1.2GHz	0.35	differential

* Maximum frequency may be limited by specific package selection.

** 50 Ohm termination; 200mV peak to peak swing qualified by package type.

*** 1.2GHz ECL inputs require a 45-55% duty cycle.

Table 1-5 Internal Switching Frequency

	OPTION	Fmaxin MHz	PWin ns	Comments
INTERNAL		600	0.65	All single-ended Internal macros, including flip/flops
		800	0.50	
		1.2GHz	0.35	
		1.2GHz	0.35	
		350	1.15	Complementary macros-all except flip/flops
		650	0.62	
		900	0.45	
		900	0.45	

Note: These are guidelines - not the specifications. Refer to the macro documentation for the frequency specified for a specific macro.

1.5 Timing Checks

Pulse-width check is only implemented on flip/flops, latches and output macros. Pulse-width violation will cause error messages during simulation if timing checks are enabled. Pulse width checking only confirms that a given operating condition minimum or maximum simulation is or is not correct. No simulation for min/max across the different libraries is performed. That computation and comparison must be done manually.

1.6 Internal Resources

In selecting an array, one of the first sizing considerations is the number and type of internal cells and interface cells available. The internal core area of the Q20000 Series bipolar arrays is composed of logic (L) cells in a Sea of Cells architecture.

Internal cell usage is reported by the population ERC.

1.7 I/O Resources - In General

The flexible I/O of the Q20000 Series Arrays allows a broad selection of I/O modes.

- ◆ ECL inputs are either 10K or 100K and are typed by the chip macro.
 - ECL bidirectionals are treated as inputs (UEnn or UKnn macros)
 - Only one type is allowed per array and the type must match the chip macro)
 - Only the ECL outputs may be of mixed types (OEnn and OKnn macros)
- ◆ Modes may be:
 - 100% ECL 10K or ECL 100K or both ECL output types on one array with a single -5.2V, -4.5V or +5V supply;
 - 100% ECL 10K or ECL 100K or both ECL output types on one array with a dual supply of +5V and -5.2V or +5V and -4.5V;
 - TTL/ECL 10K or TTL/ECL 100K or TTL with both ECL output types with a dual supply of +5V and -5.2V or +5V and -4.5V or a single supply of +5V.
- ◆ There is a limit on the number of TTL output macros that may be used on the Q20000 arrays. Refer to the cell resource table for specific limits.
 - PLL array use edge-controlled 8mA TTL outputs. Consult AMCC for these macros.
- ◆ The AMCC MacroMatrix AMCCERC population report will show an error if more than the allowed TTL output macros are used for the Q20000 Series arrays.
- ◆ There is a limit on the number of ECL output macros that may be used on the Q20000 Series arrays. Refer to the cell resource table for specific limits.
- ◆ The AMCC MacroMatrix population ERC will show an error if more than the allowed ECL output macros are used for the Q20000 Series arrays.
- ◆ Darlington type macros cannot be used with a single power supply.
- ◆ Single-cell 25 Ohm ECL outputs are Darlington macros and require dual power supplies.
- ◆ Refer to AMCCPKG.LST or AMCCIO.LST for information on the fixed power and ground pads provided with the array.
- ◆ The number of fixed thermal diode and AC monitor pads (4) and their locations for a given array is listed in AMCCPKG.LST.
- ◆ There are no placement restrictions due to both ECL 10K and ECL 100K outputs appearing on the same circuit.
- ◆ There may be parametric deviations when both ECL 10K and ECL 100K appear on the same circuit (due to non-standard voltages being used).
- ◆ Cell and pad usage is reported by the population ERC. Package signal pin requirements are also reported

Table 1-6 Q20000 Series I/O and Internal Cell Resources

Array Name	Internal Cells	Digital I/O Cells (for signals)	I/O Cells (fixed) *	I/O Signals – PLL Related
Q20120	3414	198	4	N/A
Q20080	2044	162	4	N/A
Q20045	1233	128	4	N/A
Q20P025	595	76	4	12
Q20025	733	100	4	N/A
Q20P010	177	54	4	12
Q20010	267	66	4	N/A

* 2 pads are used by the AC Speed Monitor and 2 by the thermal diode.

** Only for the largest package, 100_LDCC for the Q20P010 and 132_LDCC for the Q20P025

Table 1-7 A20000 Series ECL, TTL, PLL Power/Ground Resources

Array Name	ECL Outputs Limit	TTL Outputs Limit	PLL Power/Ground	Digital Power/Ground
Q20120	172	100	N/A	78
Q20080	130	80	N/A	52
Q20045	100	64	N/A	52
Q20P025	51	51*	8	22
Q20025	80	48	N/A	36
Q20P010	34	34*	8	20
Q20010	50	24	N/A	32

* Edge-controlled 8 mA TTL outputs only.

Add last two columns to find total number of fixed power and grounds.

Table 1-8 Chip Macros And I/O Modes

Chip Macro	Allowed Input Type	Allowed Output Type	Default Supply
QxxxxxECL10K	ECL10K	ECL10K,	-5.2V
		ECL100K	
QxxxxxECL100K	ECL100K	ECL10K,	-4.5V
		ECL100K	
QxxxxxDECL10K	ECL10K	ECL10K,	-5.2V,+5V
		ECL100K	
QxxxxxDECL100K	ECL100K	ECL10K,	-4.5V,+5V
		ECL100K	
QxxxxxMIX10K	ECL10K,	ECL10K,	-5.2V,+5V
	TTL	ECL100K	
		TTL	
QxxxxxMIX100K	ECL100K,	ECL10K,	-4.5V, +5V
	TTL	ECL100K,	
		TTL	
QxxxxxTTL	CONSULT AMCC		
QxxxxxTTL10K	ECL10K,	ECL10K,	+5V
**	TTL	ECL100K	
		TTL	
QxxxxxTTL100K	ECL100K,	ECL10K,	+5V
**	TTL	ECL100K,	
		TTL	

Substitute 20120, 20080, 20045, 20P025, 20P010, 20025 or 20010 for xxxxx.

For PLL arrays substitute 20P025 and 20P010

PLL arrays allowed I/O modes: MIX10K, MIX100K, TTL10K, or TTL100K

Power_Supply Parameter On The ECL10K and ECL100K chip

Macros Can Be Set To Be STD5 (-5.2V), STD4 (-4.5V) or 5VREF (+5V).

Power_Supply Parameter On The DECL10K, DECL100K, MIX10K, and MIX100K Chip Macros Can Be Set To Be STD5 or STD4.

** Darlington macros cannot be used on single-supply circuits.

Table 1-9 Power-Ground Pad Resources *

		Q20120	Q20080	Q20045	Q20025	Q20010	Q20P025	Q20P010
I/O MODE: TOTAL	PWR / GNDS:	78	52	52	36	32	47	30
100% ECL, Single Supply	core GND (*) Ξ	20	16	16	8	8		
	core V- (**)=	18	16	16	8	8		
	I/O GND (*)=	40	20	20	20	16		
100% ECL dual supply	CORE GND (0V)	20	16	16	8	8		
	CORE V- (**)	18	16	16	8	8		
	I/O V+ (+5V)	8	4	4	4	4		
	I/O GND (0V)	32	16	16	16	12		
ECL/TTL MIX, dual supply	CORE GND (0V)	20	16	16	8	8	10	6
	CORE V- (**)	18	16	16	8	8	16	11
	I/O V+ (+5V)	8	4	4	4	4	2	2
	I/O GND (0V)	32	16	16	16	12	19	11
ECL/TTL MIX, single supply	CORE GND (0V)	18	16	16	8	8	10	6
	CORE V+ (+5V)	20	16	16	8	8	16	11
	I/O V+ (+5V)	28	16	16	16	12	19	11
	I/O GND (0V)	12	4	4	4	4	2	2

* For a detailed list, see AMCCIO.LST ** CORE V: -5.2V for STD-REF ECL 10K

-4.5V for STD-REF ECL 100K

0V for +5V-REF ECL 10K or ECL 100K

* CORE GND: 0V for STD-REF ECL 10K or ECL 100K

+5V for +5V-REF ECL 10K or ECL 100K

Table 1-10 Fixed Pad Numbers for Thermal Diodes and AC-Speed Monitor

Array Name	Thermal Diode		AC Speed Monitor	
	Cathode Pad #	Anode Pad #	VEE Pad #	ECL Pad #
Q20120	207	208	12	34
Q20080	161	162	9	33
Q20045	136	137	4	25
Q20P025	97	93	3	26
Q20025	103	104	3	26
Q20P010	88	87	10	24
Q20010	74	75	10	24

1.8 Adding Extra Power or Ground - IEVCC

The Q20000 Series Logic Arrays require that an extra ECL VCC pad be added when the number of simultaneously switching ECL 50 Ohm outputs exceeds four (4). Add an IEVCC macro for each group of four (4) simultaneously switching ECL outputs after the first four (4). These must be interspersed within the switching group.

Non-50 Ohm outputs are equated to 50 Ohm outputs as follows:

- ◆ ECL 25 Ohm outputs count as two (2) 50 Ohm outputs.
- ◆ ECL 50 Ohm differential outputs count as one (1) 50 Ohm output.

The IEVCC PAD should be placed to allow connection to the internal package plane and not to an external package pin, when internal planes are available. Consult AMCC for IEVCC placement restrictions if you are doing preplacement.

The designer must use the **SWGROU**P macro parameter (property) on all simultaneously switching output macros and on the IEVCC macros added per the equation below. Failure to tag the added IEVCC macros can result in SSO error messages.

Use the following method to compute the number of IEVCC required:

$$\text{Estimate} = \frac{\left| \begin{array}{c} \text{number of equivalent} \\ \text{ECL 50 Ohm SSOs} - 1 \end{array} \right|}{4}$$

Note: In +5V ECL or ECL/TTL mixed circuits, IEVCC is considered to be power. It is considered to be ground for all other cases.

Table 1-11 # of Simultaneously Switching ECL per group - Add ECL VCC

	# SSOs/Group	# Added ECL VCC
50 Ohm ECL in any system; 100% ECL or mixed mode	0 - 4	0
	5 - 8	1
	9 - 12	2
	13 - 16	3
	17 - 20	4
	etc.	

1.9 Adding Extra Power or Ground - ITPWR, ITGND

The Q20000 Series Logic Arrays require that an extra pair of TTL PWR and TTL GND pads be added when the number of simultaneously switching TTL 8 mA outputs exceeds eight (8). Add a TTL power-ground pair (ITPWR and ITGND) for each group of eight (8) simultaneously switching TTL outputs after the first eight (8). These must be interspersed within the switching group. Non-8 mA outputs are equated to 8 mA outputs as follows:

- ◆ A TTL 20mA output counts as two (2) 8mA outputs.

The power-ground pads should be placed to allow connection to the internal package plane and not to an external package pin, when internal planes are available. Consult AMCC for ITPWR and ITGND placement restrictions if you are doing preplacement.

The designer **MUST** use the SWGROU P macro parameter (property) on all simultaneously switching output macros and on the ITPWR and ITGND macros added per the equation below. Failure to tag the added power and ground macros can result in SSO error messages.

Use the following to estimate the number of TTL power and ground pairs.

$$\left| \text{number of equivalent} \right|$$

$$\text{Estimate} = \frac{\text{TTL 8mA SSOs} - 1}{8}$$

1.10 Additional ITPWR, ITGND

Table 1-12 # of Simultaneously Switching TTL per group - Add TTL Pairs

	# SSOs/Group	# Added PPL PWR/GND Pairs
8 mA TTL in any system	0 - 8	0
	9 - 16	1
	17 - 24	2
	etc.	

There are no quadrants on the Q20000 arrays.

1.11 Additional Power/Ground Rules

- ◆ Estimate one added ground or power pad between ECL and TTL groups and between ECL input and ECL output groups for isolation.
- ◆ Use the IEVCC (ECL ground) for ECL isolation.
- ◆ Isolate high-speed CMOS input from ECL signals (array and package isolation).

1.12 Maximum Internal Cell Utilization

The internal cell utilization limit is a guideline for the routability of an array. It is one means of estimating the feasibility of a design on a given array. The specified cell utilization limit is designed as a sizing guideline. The cell utilization refers to the internal array matrix (L cells) only and should not be considered to be the only population or routing check. Designs meeting the restrictions are expected to be routable designs, provided they also satisfy internal pin count limits.

The internal cell utilization limit is 95% for the Q20000 Series arrays.

Cell utilization is reported by the population ERC.

1.13 Internal Pin Count Limit

A more specific check on routability is the internal pin count limit

- ◆ An array is routable if the number of internal pins that must be routed does not exceed the maximum pin count limit.
- ◆ It is considered to be a *risky* design if the number of pins is up to +10% over the maximum pin count limit.
- ◆ It is considered to be an *extremely risky* design if the number of pins is from +11% to +18% over the maximum pin count limit.
- ◆ A design is *unacceptable* if the number of pins is \geq +18% over the maximum allowed pin count.

Table 1-13 Maximum Internal Pin Count

Array	Actual Limit	Estimated Limit
Q20120	7548	6038
Q20080	4586	3668
Q20045	3097	2478
Q20P025	1555	1244
Q20025	1883	1507
Q20P010	453	362
Q20010	733	586

The AMCC MacroMatrix internal pin count ERC reports the internal pin count of the design and checks it against the *ACTUAL* limit.

1.13.1 Estimated Limit for Internal Pin Counts - use of

Use the estimated limit when performing preliminary checks on a block-level conversion or design.

1.13.2 Estimating Internal Pin-Count for the Circuit

If the number of internal pins that must be routed (pin-count) is not available for a design in its early stages (prior to capture), estimate it by:

$$\text{routable pins} = 2.5 * (\# \text{ of L cells}) + 1.5 * (\# \text{ of I/O cells})$$

1.14 Fan-Out Restrictions

The individual macro fan-out load limits are specified in the Design Manual, Volume I, Section 6. Derating requirements are discussed in Volume I, Section 2.

- ◆ Derate all clock lines and distortion-sensitive paths by 20% for speeds below the breakpoint and by 40% for speeds at or above the breakpoint.

1.14.1 Derated Fan-Out Load Limits (Standard / 20% Derated / 40% Derated)

Table 1-14 Derating Breakpoint : 600 MHz

MACRO TYPE	OPTION	LIMIT **
ECL INPUT, BIDIRECTIONAL	L,S,H	18/14/10
TTL INPUT	L,S,H	18/14/10
TTL MIX BIDIRECTIONAL	L,S,H	9/07/05
SINGLE-SUPPLY TTL BIDIRECTIONAL	L,S,H	18/14/10
INTERNAL MACROS	L,S,H	18/14/10
DRIVERS (ANY)	D	32/26/20

** standard /20% derated / 40% derated

Table 1-15 Breakpoint = 600 MHz Derating Guideline

OPERATING SPEED:	DERATE BY:	FOD VALUE
< 600MHz	20%	20
≥ 600MHz	40%	40

The fan-out ERC checks for excessive loading. It will check for a derated load limit only if the FOD net parameter has been used.

1.15 Fan-In

The fan-in load (presented to its driver) for each macro input pin is listed in the macro documentation in Section 6. No asterisks are used to alert the designer to fan-in greater than one since so many inputs do exceed one load. H-option macros may have a different fan-in than S- and L-option macros.

1.16 Macro Size and Cell Counts

Basic macros cannot be assumed to be one cell in the Q20000 Series library. Size is documented in the macro documentation in Section 6. H-option macros may use more cells than the S- and L-option macros.

1.17 Macro Timing Specifications

The macro timing specifications are worst-case maximum and worst-case minimum. No worst-case timing multipliers are used for the Q20000 Series arrays. Adjustment factors are used to convert specifications from one library to another.

1.17.1 Commercial Specification

ECL with a -5.2V or +5V supply: Commercial worst-case timing data is for 0°C ambient to 70°C ambient with ± 5% power supply variation and a maximum junction temperature of 130°C.

ECL with a -4.5V supply: Commercial worst-case timing is for 0°C ambient to 70°C ambient with ±7% power supply variation and a maximum junction temperature of 130°C. (Power supply is -4.5V, -4.2V maximum and -4.8V minimum.)

For a junction temperature that is > 130°C or for any other violation of the commercial environment specification, use the Military worst-case timing data when computing path propagation or set-up and hold times.

1.17.2 Military Specification

ECL with a -5.2V or +5V supply: Military worst-case timing is for -55°C ambient to +125°C case with ±10% power supply variation (+5V or -5.2V) and a maximum junction temperature of 150°C.

ECL with a -4.5V supply: Military worst-case timing is for -55°C ambient to +125°C case with a power supply variation of -4.5V to -4.8V and a maximum junction temperature of 150°C. MIL-STD-883C Class B screening is used.

For a junction temperature that is > 150°C or for a violation of any other military environment specification, consult AMCC.

1.18 Product_Grade Chip Macro Parameter

The MIL (military) and COM (commercial) values assigned to the PRODUCT_GRADE chip macro parameter will affect:

1. The power computation
2. ECL V_{OH} and V_{OL} levels
3. The testing procedures used for the part
4. The annotation delay files

1.19 Extrinsic Delay Computation - Internal Nets

$$t_{ex} = k_{fo} * L_{fo} + k_{net} * L_{net}$$

Note: k_{fo} is equal to k_{net}

$$t_{ex} = k_{fo} * (L_{fo} + L_{net})$$

Compute delays for rising and falling edges.

L_{fo} = sum of all electrical loads on the net (sum of the fan-ins for all macros driven)

L_{net} = Front or Back-Annotation metal loading

t_{ex} for internal nets is computed by AMCCANN and is available in the annotation files.

1.20 Extrinsic Delay Computation - Output Nets

$$t_{ex} = k_{cap} * \text{Capacitive load}$$

Capacitive load = sum of package signal pin capacitance and system capacitive load for the package signal pin. t_{ex} is the delay resulting from that load

Compute delays for both rising and falling edges.

t_{ex} for external nets is computed by AMCCANN and is available in the annotation files.

Table 1-16 EXAMPLE K-FACTORS – CCOM5MAX LIBRARY - kfo = knet; kcap**

Macro Type	Description	min/max	units
ECL input, Bidi and	rising	2.3/5.1	ps/LU
internal macros - L option	falling	3.9/8.5	ps/LU
ECL input, Bidi and	rising	1.8/3.9	ps/LU
internal macros - S option	falling	3.0/6.5	ps/LU
ECL input, Bidi and	rising	1.4/3.1	ps/LU
internal macros - H option	falling	2.4/5.2	ps/LU
ECL input, Bidi and	rising	1.1/2.3	ps/LU
internal macros - drivers	falling	1.5/3.3	ps/LU
ECL output - 50 Ohm	rising	16.0/36.0	ps/pF
standard	falling	20.0/44.0	ps/pF
ECL output - 25 Ohm	rising	13.0/30.0	ps/pF
Darlington	falling	15.0/34.0	ps/pF
ECL output - 50 Ohm	rising	13.0/30.0	ps/pF
Darlington	falling	21.0/46.0	ps/pF
TTL input and Bidi (Non-	rising	3.0/6.5	ps/LU
-Turbo) S, L, H options	falling	6.0/13.0	ps/LU
TTL input and Bidi (Turbo)	rising	1.4/3.1	ps/LU
S, L, H options	falling	2.4/5.2	ps/LU
TTL output - 20 mA	rising	33.0/72.0	ps/pF
	falling	33.0/72.0	ps/pF
TTL output - 8 mA	rising	33.0/72.0	ps/pF
	falling	54.0/117.0	ps/pF

** Individual macro k-factors are specified in the macro library documentation in the Design Manual, Volume I, Section 6.

Table 1-17 Front-Annotation Estimated Metal Loads - Lnet

PinsDriven	Q20120	Q20080	Q20045	Q20025	Q20010	Q20P025	Q20P010
1	12.00	11.00	9.00	7.50	6.00	7.50	6.00
2	19.49	18.12	15.14	13.06	10.82	13.06	10.82
3	25.89	24.26	20.52	18.06	15.27	18.06	15.27
4	31.67	29.85	25.46	22.74	19.49	22.74	19.49
5	37.02	35.05	30.09	27.18	23.57	27.18	23.57
6	42.06	39.96	34.50	31.45	27.52	31.45	27.52
7	46.85	44.65	38.73	35.57	31.37	35.57	31.37
8	51.45	49.16	42.81	39.59	35.14	39.59	35.14
9	55.87	53.51	46.77	43.50	38.84	43.50	38.84
10	60.14	57.73	50.61	47.32	42.48	47.32	42.48
11	64.29	61.83	54.36	51.07	46.06	51.07	46.06
12	68.33	65.83	58.03	54.75	49.60	54.75	49.60
13	72.27	69.73	61.62	58.37	53.09	58.37	53.09
14	76.12	73.55	65.14	61.94	56.54	61.94	56.54
15	79.88	77.30	68.60	65.45	59.96	65.45	59.96
16	83.57	80.98	72.00	68.92	63.34	68.92	63.34
17	87.20	84.59	75.35	72.35	66.69	72.35	66.69
18	90.76	88.14	78.65	75.73	70.01	75.73	70.01
19	94.26	91.64	81.90	79.08	73.30	79.08	73.30
20	97.70	95.09	85.12	82.39	76.56	82.39	76.56
21	101.10	98.49	88.29	85.67	79.81	85.67	79.81
22	104.44	101.84	91.42	88.92	83.03	88.92	83.03
23	107.74	105.16	94.52	92.14	86.22	92.14	86.22
24	111.00	108.43	97.59	95.33	89.40	95.33	89.40
25	114.22	111.66	100.62	98.49	92.56	98.49	92.56
26	117.40	114.86	103.63	101.63	95.69	101.63	95.69
27	120.54	118.03	106.60	104.75	98.81	104.75	98.81
28	123.65	121.16	109.55	107.84	101.91	107.84	101.91
29	126.72	124.26	112.47	110.91	105.00	110.91	105.00
30	129.77	127.33	115.37	113.96	108.07	113.96	108.07
31	132.78	130.37	118.24	116.99	111.12	116.99	111.12
32	135.76	133.38	121.09	120.00	114.16	120.00	114.16
33	138.72	136.37	123.92	122.99	117.19	122.99	117.19

Where pins driven = the internal net physical pin count minus 1.

For the Q20000, netsize - 1 = number of macro pins driven. Electrical fan-out loading is taken care of in the Lfo term.

1.21 Front-Annotation Load Units

The Front-Annotation statistical wire load units table was calculated using the following :

$$** b$$

$$LU = a * (\text{pins driven})$$

Table 1-18 Estimated Front-Annotation Load Units - LU

ARRAYS	b	a
Q20120	0.70	12.00
Q20080	0.72	11.00
Q20045	0.75	9.00
Q20P025	0.80	7.50
Q20025	0.80	7.50
Q20P010	0.85	6.00
Q20010	0.85	6.00

used to generate
estimated wire loads
table

1.22 Back-Annotation Load Unit Conversion Factors

The Back-Annotation delay file is derived using the following:

Table 1-19 Back-Annotation Load Unit Conversion Factors – LU/mm

	Rising	Falling	Conversion Factor
Metal 2	10	10	c2
Metal 3	10	9	c3

$$LnetBA = LU = (M3 * c3) + (M2 * c2)$$

M3 = length of metal 3 in mm

M2 = length of metal 2 in mm

c3 = conversion in LU/mm

c2 = conversion in LU/mm

LU = load units due to actual metal, used as Lnet

1.23 Macro Specification - MAX/MIN - Computing COM5MINMAX from COM5MINMIN, etc.

1.23.1 The Adjustment Factors

The macro specifications for Tpd and k-factors in the COM5 portion of Section 6 show COM5MAXmax and COM5MINmin for the COM5 libraries. To find COM5MAXmin, multiply COM5MAXmax by the number shown in the following table. To find COM5MINmax, multiply COM5MINmin by the number shown in the table. The numbers vary with the macro outputs. Use the same methods for the MIL5, COM4 and MIL4 libraries.

1.23.2 Converting COM5 to COM4; Converting MIL5 to MIL

To convert the timing and k-factor specifications supplied in Volume I, Section 6 from COM5 to COM4 or from MIL5 to MIL4, use the adjustment factors.

For a path delay under MIL4 or COM4 operating conditions:

$$\text{tpath} = \text{adjustment} * (\text{Tpds}_{\text{sum}} + \text{tex}_{\text{sum}})$$

factor

Note that ALL data is represented in the workstation libraries.

TABLE 1-20 TIMING ADJUSTMENT FACTORS

COMMERCIAL		
For Single-Ended Macros		
COMnMAXmin	=	0.76 * COMnMAXmax
COMnMINmax	=	1.24 * COMnMINmin
For Complementary Output Macros		
COMnMAXmin	=	0.70 * COMnMAXmax
COMnMINmax	=	1.30 * COMnMINmin
MILITARY		
For Single-Ended Macros		
MILnMAXmin	=	0.64 * MILnMAXmax
MILnMINmax	=	1.36 * MILnMINmin
For Complementary Output Macros		
MILnMAXmin	=	0.54 * MILnMAXmax
MILnMINmax	=	1.46 * MILnMINmin

n = 5 or 4

COM4MINmin	=	COM5MINmin	*	0.95
COM4MAXmax	=	COM5MAXmax	*	1.05
MIL4MINmin	=	MIL5MINmin	*	1.00
MIL4MAXmax	=	MIL5MAXmax	*	1.00

1.23.3 Using the Libraries

Simulations are performed using the maximum and minimum extremes for a given set of operating conditions. Select the library, then select the min or max data within the library.

Table 1-21 Library Selection

	Power Supply	Product Grade	Extreme	Library Name	Data Range
COMMERCIAL	+5V	COM	MAX	COM5MAX	min/max
	-5.2V	COM	MAX	COM5MAX	min/max
	-4.5V	COM	MAX	COM4MAX	min/max
COMMERCIAL	+5V	COM	MIN	COM5MIN	min/max
	-5.2V	COM	MIN	COM5MIN	min/max
	-4.5V	COM	MIN	COM4MIN	min/max
MILITARY	+5V	MIL	MAX	MIL5MAX	min/max
	-5.2V	MIL	MAX	MIL5MAX	min/max
	-4.5V	MIL	MAX	MIL4MAX	min/max
MILITARY	+5V	MIL	MIN	MIL5MIN	min/max
	-5.2V	MIL	MIN	MIL5MIN	min/max
	-4.5V	MIL	MIN	MIL4MIN	min/max

Example: When a COM5 (Commercial with a +5V or -5.2V supply) analysis is to be performed, use the COM5MAX library and the max data within the library for the maximum worst-case and use the COM5MIN library and the min data within the library for the minimum worst-case.

Note: the COM5MAX library does have min data and the COM5MIN library has max data. Simulations can be run using these selections if desired but those simulations are not part of design submission.

Design Submission Extremes

Design submission requires simulation at two extremes for the given operating conditions. Choose one pair:

- ◆ COM5MINmin and COM5MAXmax
- ◆ COM4MINmin and COM4MAXmax
- ◆ MIL5MINmin and MIL5MAXmax
- ◆ MIL4MINmin and MIL4MAXmax

1.24 AMCCANN File Names

Both the internal net delays and the output net delays are computed by AMCCANN and files generated for use with the simulation software. AMCCANN is described in the *AMCCANN User's Manual*. The file names for the Q20000 Series are changed as of this library release. **Table 1-22 AMCCANN Delay File Names**

Minimum	Maximum	Product Grade	Power Supply
FNTC4MN.ews	FNTC4MX.ews	COMMERCIAL	-4.5V
FNTC5MN.ews	FNTC5MX.ews	COMMERCIAL	-5.2V or +5V
FNTM4MN.ews	FNTM4MX.ews	MILITARY	-4.5V
FNTM5MN.ews	FNTM5MX.ews	MILITARY	-5.2V or +5V
BCKC4MN.ews	BCKC4MX.ews	COMMERCIAL	-4.5V
BCKC5MN.ews	BCKC5MX.ews	COMMERCIAL	-5.2V or +5V
BCKM4MN.ews	BCKM4MX.ews	MILITARY	-4.5V
BCKM5MN.ews	BCKM5MX.ews	MILITARY	-5.2V or +5V

ews = (dsy, men, val, tim, lsr, lsr-rc, ver)

where

dsy	=	Dazix
val	=	Valid
tim	=	Valid Timing Verifier (when available)
lsr	=	Lasar 6 (prior to 1Q92 release)
lsr-rc	=	Lasar 6 (RC tree - after 1Q92) (Back-Annotation only)
ver	=	Verilog

1.25 Annotation Differences

Differences between the Front-Annotation simulations performed at the customer's site and the Back-Annotation simulations performed at AMCC include the differences between the estimated net delay due to estimated metal length and the actual delay due to actual metal length.

Differences between the release macro library and the internal macro library at AMCC may also exist due to on-going development and refinement of the library. AMCC will perform Back-Annotation simulations using the internal library.

1.26 Worst-Case Maximum Current Multiplication Factors

The Q20000 Series uses three worst-case current multipliers, one for core macros, one for interface macros and one for overhead current.

Table 1-23 Worst-Case Maximum Current Multipliers

Core WCCM1	Interface WCCM2	Overhead WCCM3	Treat Value As
1.25	1.30	1.25	Typical

1.27 Typical Overhead Current

The overhead current is fixed regardless of I/O cell or internal cell usage.

Table 1-24 Typical Overhead Current in mA

ARRAY	EECL Mode Single Supply IEE, mA	ECL Mode DECL Dual Supply IEE/ICC, mA	ECL/TTL Mixed Mode Single Supply IEE/ICC, mA	ECL/TTL Mixed Mode Dual Supply ICC
Q20120	410	410/26	410/26	410
Q20080	220	220/26	220/26	220
Q20045	187	187/26	187/26	187
Q20P025	Not Allowed	Not Allowed	101/26	101
Q20025	128	128/26	128/26	128
Q20P010	Not Allowed	Not Allowed	63/13	63
Q20010	67	67/13	67/13	67

The macro occurrence ERC includes overhead current in the power dissipation computation.

Multiply by 1.25 to determine worst-case maximum overhead current.

1.28 ECL Output Termination Current

The ECL termination current is a function of the actual load. When a macro is selected it should be capable of driving a resistive load equal to or greater than its rating. The ERCs will assume the load to be equal to the rated load.

The ECL output termination currents shown below are used by the AMCC MacroMatrix AMCCERC software. The currents shown are the average current (average of IOH and IOL) and represent 50% terminations active.

Table 1-25 ECL 10K/100K Termination Current *

Termination	Current
25 Ohm	28.0 mA
50 Ohm	14.0 mA

* the average current (average of IOH and IOL) for termination to -2V

1.28.1 When 50 / 25 Ohm Terminations Not Used

The ERC software cannot detect when a load does not match that for which the macro is rated. Therefore, if other ECL output load resistances are used, the actual current value must be computed for use in this equation. For a termination of -2V, to find the average current in mA use:

$$I(\text{in mA}) = \frac{0.7}{R \cdot (10^{-3})} \text{ for any } R$$

For the Q20000 Series arrays, the macro occurrence ERC uses either a 50 Ohm or a 25 Ohm to -2V termination, depending on the macro.

1.28.2 When $V_T \neq -2V$

For other termination voltages, an adjustment to the power dissipation computation must be made by the designer. For a termination voltage V_T , to find the average current in mA use:

$$I(\text{in mA}) = \frac{(-1.3V - V_T)}{R \cdot (10^{-3})} \text{ for any } R$$

1.28.3 Darlington ECL Output

Darlington ECL outputs are treated as a standard ECL output for power computations.

1.28.4 • Series Termination; CML Macros

There is no IOEF output current for on-chip series termination or CML outputs. The current specification for these macros includes any load-dependent dissipation.

1.29 Array PAD Count (optional report)

Array pad count is only reported by the population ERC when the selected array has one or more packages that do not use internal power and ground planes. The array pad count is the sum of all array signal pads, all array fixed power and ground pads, all array fixed signal pads and all added power and ground macro pads required due to simultaneously switching outputs 3-state drivers, etc. The array pad count of a design may not exceed the array pad count limit for the array when internal power and ground planes are not used in the package.

Table 1-26 Array Pad Count Limit *

Array Name	Array Signal PADS (1)	Array Fixed Power/Ground PADS	Total Array External PADS
Q20120	202/198	78	280
Q20080	166/162	52	218
Q20045	132/128	52	184
Q20P025	55/51+12PLL	26+8PLL	96/92
Q20025	104/100	36	140
Q20P010	38/34+12PLL	20+8PLL	68/64
Q20010	70/66	32	102

(1) Four (4) are required for AC speed monitor; thermal diode. The lower number is the number of other I/O signals that may be on the array. PLL arrays have 12 I/O positions dedicated to the PLL macro; which are not available for other signals.

* The number of I/O pads useable depends on the package.

1.30 MIN PKG Signal Pins; MAX PKG Signal Pins

Maximum package signal pins required is reported by the population ERC and is used to select package size when all of the standard packages available for the array use internal power/ground planes. MAX PKG SIGNAL PINS is the count of: the fixed signal pads which must reach a package pin (for the AC speed monitor and the thermal diode); all I/O signals; and all added power and grounds. MIN PKG SIGNAL PINS excludes the added power and grounds. MAX PKG SIGNAL PINS should be used in the initial package selection.

Refinement of the number of package signal pins required by the circuit can be made after placement when the need for package signal pins for use by added power and ground macro pads is known.

1.30.1 Package Signal Pins Required by the Circuit

ERC REPORT:	(AFTER PLACEMENT)	ERC REPORT:
MIN PKG SIGNAL PINS	≤ Actual Pkg Pins	≤ MAX PKG SIGNAL PINS
	Required by the	
	Circuit	

1.30.2 Signal Pins Available vs. Signal Pins Required

Package Signal Pins Required \leq Package Signal Pins Available by the Circuit

- ◆ Thermal Diode and AC speed monitor fixed signal pads go to external package signal pins.
- ◆ All I/O signals go to external package signal pins.
- ◆ Fixed power and ground pads go to internal package planes, for all packages designed for the Q20000 Series.
- ◆ Added power and ground pads should go to the internal package planes if the package uses planes (placement restriction). Where this placement cannot be achieved, the added power and ground pads that do not bond to an internal plane must go to external package signal pins.
- ◆ The number of power and ground pins provided for a package is listed in the package matrix.
- ◆ The pins available for signals for a package are listed in the package matrix.

2 AMCC Q20000 Standard Packaging Matrix

Table 2-1 AMCC Q20000 Standard Packaging Matrix

Package	I/O Signal Pins	PLL Signals	Fixed I/O Signals	Total I/O Signals	Array
Leaded Chip Carriers					
68_LDCC	23	12	4	39	Q20P010
100_LDCC	66		4	70	Q20010
100_LDCC	34	12	4	50	Q20P010
100_LDCC	45	12	4	61	Q20P025
132_LDCC	92		4	96	Q20025
132_LDCC	51	12	4	67	Q20P025
196_LDCC	128		4	132	Q20045
196_LDCC	132		4	136	Q20080
Pin Grid Arrays					
100_PGA_CD	66		4	70	Q20010
149_PGA_CD	100		4	104	Q20025
209_PGA_CD	128		4	132	Q20045
251_PGA_CD	162		4	166	Q20080
301_PGA_CD	198		4	202	Q20120

I/O Signal Pins is the number of I/O signals allowed.

PLL Signals represents the 12 PLL signals allocated for the PLL macros on the PLL arrays. These pins are not available to other I/O macros.

Fixed I/O Signals is the four dedicated pins for the thermal diode and the AC Speed Monitor. **Total I/O Signals** - this is the number to compare to the *maximum package signal pins required* number computed by AMCCERC.

2.1 Power Computation

2.1.1 DC Power Computation

Sum all interface macro currents and multiply by the interface macro worst-case current multiplier, 1.40. Keep IEE and ICC separate.

Sum all internal macro currents and multiply by the internal macro worst-case current multiplier, 1.37. Keep IEE and ICC separate.

Find the IEE and ICC overhead currents and multiply them by the worst-case overhead current multiplier, 1.25. Keep IEE and ICC separate.

Add all IEE currents together.

Add all ICC currents together.

Find the worst-case VCC and VEE voltages.

Multiply IEE * VEE.

Multiply ICC * VCC.

Compute ECL static power dissipation: $P_{oef} = 1.3 * \text{termination current} * \text{number of outputs}$

Add all items together.

This is the worst-case DC power dissipated by the circuit.

2.1.2 AC Power Computation

The equations used to compute internal cell power dissipation are:

For all ECL Darlington output macros:

$$PD_{AC} = f * n * 15 \text{ microwatts}$$

where f = maximum frequency of the Darlington outputs in MHz

n = number of ECL Darlington output macros toggling at frequency f

The number of Darlington outputs can be determined from the I/O statistics ERC report and from the AC Bipolar/BiCMOS Macro Occurrence worksheet.

Count the number of Darlington output macros switching at the fastest frequency and compute the power due to those macros. Count the number of Darlington output macros switching at the next fastest frequency and compute their power. Repeat until all Darlington output macros are accounted for.

For all ECL inputs and all internal macros:

$$PI_{AC} = 0.2 * f * n * 3.25 \text{ microwatts}$$

where f = maximum frequency of operation in MHz

n = number of ECL input macros and number of internal macros

0.2 represents the assumed 20% of macros switching at one time

The number of internal macros can be found from the population ERC. The number of ECL input macros can be found in the population I/O Statistics report.

$$Pd_{AC} = PI_{AC} + PD_{AC}$$

Sum the two results together and convert to watts (or to the same units as was used for DC power). This equation provides an estimate of the worst-case AC power dissipation for the Q20000 array.

Use the same equation for MILITARY and COMMERCIAL computations.

2.1.3 Total Power

Add the DC power computation result to the AC power computation result.

$$P_d = P_{dDC} + P_{dAC}$$

The result is the worst-case power dissipation to be used in computing junction temperature.

2.2 Computing Junction Temperature

For COMMERCIAL devices, the maximum junction temperature is 130 °C.

For MILITARY devices, the maximum junction temperature is 150 °C.

The thermal resistance between the die junction and the ambient environment depends on several factors: die size, thermal resistance of the package, thermal resistance of the heatsink, the shape of the heatsink, ambient temperature, air flow speed and the direction of the air flow with respect to the package or heatsink fins.

◆ Computing Junction Temperature For Commercial Grade Devices

To compute the junction temperature for COMMERCIAL grade devices, the designer needs to determine the maximum power dissipation of the die (P_d), the thermal resistance between the die and the ambient environment (Θ_{ja}), and the maximum ambient temperature (T_a). The maximum junction temperature is:

$$T_j = (P_d * \Theta_{ja}) + T_a$$

With proper thermal management, an ambient temperature $T_a = 70^\circ\text{C}$ can be maintained for most applications.

◆ Computing Junction Temperature For Military Grade Devices

To compute the junction temperature for MILITARY devices, the designer needs to determine the maximum power dissipation of the die (P_d), the thermal resistance between the die and the case (package) (Θ_{jc}), and the maximum case temperature (T_c). The maximum junction temperature is:

$$T_j (P_d * \Theta_{jc}) + T_c$$

The maximum case temperature T_c is taken as 125°C for MILITARY applications.

Table 2-2 **AMCC Q20000 SERIES PACKAGING MATRIX** Θ_{jc} in °C/W

PACKAGE	Q20P010; Q20010	Q20P025; Q20025	Q20045	Q20080	Q20120
LDCC					
68_LDCC	6.0 *				
100_LDCC	6.5	5.0 **			
132_LDCC		5.0			
196_LDCC			4.5	4.0	
PGA					
100_PGA_CD	6.0				
149_PGA_CD		4.5			
209_PGA_CD			4.0		
251_PGA_CD				3.5	
301_PGA_CD					3.0

Q20P010 Θ_{jc} same as Q20010 Θ_{jc} ; Q20P025 Θ_{jc} same as Q20025 Θ_{jc} unless otherwise noted.

* Q20P010 is available in a 68_LDCC; Q20010 is not.

** Q20P025 is available in a 100_LDCC; Q20025 is not.

2.3 Package Selection and AMCCANN

The package selected will be used by the AMCCANN program to supply package pin capacitance. Front-Annotation uses one package pin value for all package pins; Back-Annotation uses pin-specific values of capacitance, available only after placement has been completed and signed-off by the designer.

The following table is a guide to the default package pin capacitances. For further information on the operation of AMCCANN or for information on the override of default values, refer to the *AMCCANN User's Guide*. Always check the table date and use the latest information available. For those with close tolerances, consult AMCC.

Table 2-3 AMCCANN Default Package Pin Capacitance By Package

Package	Min Pf	Typ Pf (Not Used)	Max Pf	Array	Default For The Array
LDCC					
68_LDCC	2.1	2.8	3.9	Q20P010; Q20010	
100_LDCC	1.5	2.2	3.1	Q20P010; Q20010; Q20P025	
132_LDCC	2.0	2.6	3.5	Q20025; Q20P025	
196_LDCC	3.0	4.6	5.6	Q20045; Q20080	
PGA					
100_PGA_CD	3.2	3.8	4.6	Q20010	X
149_PGA_CD	4.0	5.3	6.2	Q20025	X
209_PGA_CD	4.3	5.6	6.5	Q20045	X
251_PGA_CD	7.3	9.6	12.3	Q20080	X
301_PGA_CD	8.0	11.1	15.0	Q20120	X

MAX is value used for COM-MAX or MIL-MAX computations

MIN is value used for COM-MIN or MIL-MIN computations

If these numbers are not in the current software on your system, or if you wish to use other numbers, insert them through the use of the AMCCANN interface.