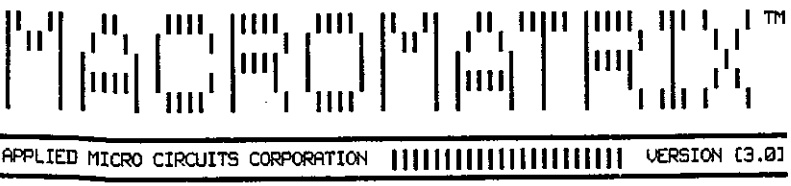
APNOTE 1
APPENDIX A
TRANSCRIPT OF CIRCUIT

(809)

Figures:

Note: for AC TEST files, see Volume II, Section 4

```
CLASS809> RUN_AMCC
```




```
      1: Part One:   Run DANCE, DRINK, AGIF and ERCs
      2: Part Two:   Run AMCCANN
      3: Part Three: Run SIFT and SOM_MAKER
      4: Part Four:  Run SOM and TCAL
      5: Part Five:  Run AMCCSIMFMT
      6: Part Six:   Run AMCCVRC
      0: Exit Program:

      Please Enter [0 - 6] : >1
```

DANCE, DRINK, AGIF, ERCs

FIGURE A1

APPLIED MICRO CIRCUITS CORPORATION ▌▌▌▌▌▌▌▌▌▌▌▌▌▌▌▌▌▌▌▌▌▌ VERSION [3.0]

1: Part One: Run DANCE, DRINK, AGIF and ERCs

2: Part Two: Run AMCCANN

3: Part Three: Run SIFT and SOM_MAKER

4: Part Four: Run SOM and TCAL

5: Part Five: Run AMCCSIMFMT

6: Part Six: Run AMCCVRC

0: Exit Program:

Please Enter [0 - 6] : >1

****** RUNNING DANCE -T -N -ERR -M3 ********

********** DANCE OK !!!!! **********

********** RUNNING DRINK -T -M3 **********

********** DRINK OK !!!!! **********

********* RUNNING AGIF NETLISTER **********

********* AGIF NETLIST COMPLETE !!! ********

********** RUNNING AMCCERC **********

```
AMCC MacroMatrix ERCs VERSION  3.40
Loading Netlist ...
 Signal I/O List written to AMCCIO.LST
 Signal/Component Cross-Reference written to AMCCXREF.LST
Checking Population.
I/O Statistics Check.
```

FIGURE A1

Continued

```
shell:05.02:08                    CURRENT CONTEXT: /USER/CLASS/MUX16

          ************ RUNNING AMCCERC ************

AMCC MacroMatrix ERCs VERSION  3.40
Loading Netlist ...
 Signal I/O List written to AMCCIO.LST
 Signal/Component Cross-Reference written to AMCCXREF.LST
Checking Population.
I/O Statistics Check.
Checking Valid Names.
Checking Pin Class.
Checking Fan-Out.
Checking Internal Pin Count.
Checking Pin Hookup and Unused Pins.
Checking Bipolar Macro Occurrence and Power Dissipation.
Checking Circuit Technology.
All Done.

          ************ AMCCERC OK !!!!! ************
```

FIGURE A1

Continued

```
Date:  19 SEP 88 14:32    File:  ERC/AMCCERC.LST


*************************************************************
*          AMCC Schematic Data Interface                    *
*          Revision [1.Ø]                                   *
*************************************************************


   Netlister version number =              7Ø8
   SDI version number =                    2.1Ø
   Netlist generation date =               19 SEP 1988
   Netlist generation time =               14:25
   Engineering workstation type =          DAISY/DNIX
   Engineering workstation path name =     /USER/CLASS/MUX16
   Product Name =                          MUX16
   Product Number =                        XXXX
   Product Grade =                         MIL
   EWS Library =                           Q5ØØØ
   EWS Library Rev =                       8Ø4
   Macro Parameter family =                Q5ØØØ
   The ARRAY type =                        Q5ØØØT
   Chip Macro Name =                       Q5ØØØTTTL1ØK
   Circuit Family =                        Q5ØØØ
   Circuit Technology =                    P
   ECL Level =                             1ØK


*************************************************************
*          SIGNAL I/O LIST                                  *
*          REVISION 1.Ø                                     *
*************************************************************


   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5ØØØ
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


   No errors found.
```

AMCCERC.LST

FIGURE A2

```
**************************************************************
*          POPULATION ERC                                    *
*          VERSION  2.8Ø                                     *
**************************************************************

   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5ØØØ
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


   No errors found.

                      Circuit   Available
---------------------------------------
SUM_INPUT:             23.Ø              PADS
SUM_OUTPUT:             5.Ø              PADS
SUM_X_TTL_PWR:          3.Ø              PADS
SUM_X_TTL_GND:          3.Ø              PADS
SUM_X_ECL_GND:          3.Ø              PADS
---------------------------------------
SUM_TOTAL_I/O          37.Ø    16Ø.Ø     CELLS
SUM_INTERNAL            9.5    352.Ø     CELLS
---------------------------------------
TOTAL ARRAY PADS       61.Ø    184.Ø     PADS
---------------------------------------

Cell utilization is:                    2.7 %

Total fixed power pins:                  12
Total fixed ground pins:                 12
Total added power pins:                   6
Total added ground pins:                  3

Total input signals:                     23
Total output signals:                     5
Total bidirectional signals:              Ø
```

FIGURE A2 CONTINUED

```
**********************************************************
*          I/O Statistics ERC                            *
*          VERSION  1.3Ø                                 *
**********************************************************

   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5ØØØ
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL
```

	number of Objects in the circuit	Object type
Inputs		
TTL	2Ø	PAD
ECL	2	PAD
SubTotal	22	PAD
Outputs		
ECL1ØK	2	PAD
Thermal Diode Connections	4	PAD
SubTotal	6	PAD

```
**********************************************************
*          VALID NAME CHECK ERC                          *
*          VERSION  2.7Ø                                 *
**********************************************************

   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5ØØØ
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


   No errors found.

**********************************************************
*          PIN CLASS ERC                                 *
*          VERSION  2.7Ø                                 *
**********************************************************

   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5ØØØ
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


   No errors found.
```

FIGURE A2 CONTINUED

```
**********************************************************
*                                                        *
*          FAN-OUT CHECK ERC                             *
*          VERSION  2.8Ø                                 *
**********************************************************

   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5ØØØ
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


   No errors found.
```

FAN-OUT LOADING TABLE FORMAT:

COMPONENT	MACRO NAME	SIGNAL	LIMIT	LOAD	% DERATING	PAGE
GØØØØ	GT99	3S28	9	2		4
GØØØØ	GT99	3S29	9	1		4
G4ØØØØ	GT6ØL	3S3Ø	4	1		4
G4ØØØ1	GT6ØL	3S24	4	1		4
EIØØØØ	IE86	3S36	1	1		4
G4ØØØ2	GT6ØL	3S37	4	1		3
SØØØ1	IT11H	INPØ	9	1		3
SØØØ2	IT11H	INP1	9	1		3
SØØ11	IT11H	INP1Ø	9	1		3
SØØ12	IT11H	INP11	9	1		3
SØØ13	IT11H	INP12	9	1		3
SØØ14	IT11H	INP13	9	1		3
SØØ15	IT11H	INP14	9	1		3
SØØ16	IT11H	INP15	9	1		3
SØØØ3	IT11H	INP2	9	1		3
SØØØ4	IT11H	INP3	9	1		3
SØØØ5	IT11H	INP4	9	1		3
SØØØ6	IT11H	INP5	9	1		3
SØØØ7	IT11H	INP6	9	1		3
SØØØ8	IT11H	INP7	9	1		3
SØØØ9	IT11H	INP8	9	1		3
SØØ1Ø	IT11H	INP9	9	1		3
SØØ21	IE93	INTCLK	7	1	2Ø	2
FFØØØØ	FF13H	INTQN	9	1		2
SØØ22	IE93	INTRST	9	1		2
MXØØØØ	MX25H	INTYØ	9	1		2
MXØØØ1	MX25H	INTY1	9	1		2
MXØØØ2	MX25H	INTY2	9	1		2
MXØØØ3	MX25H	INTY3	9	1		2
MXØØØ4	MX25H	INTY4	9	1		2
SØØØ1	IT11H	PARA1	9	1		3
SØØ1Ø	IT11H	PARA1Ø	9	1		3
SØØ11	IT11H	PARA11	9	1		3
SØØ12	IT11H	PARA12	9	1		3
SØØ13	IT11H	PARA13	9	1		3
SØØ14	IT11H	PARA14	9	1		3
SØØ15	IT11H	PARA15	9	1		3
SØØ16	IT11H	PARA16	9	1		3
SØØ17	IT11H	PARA17	9	1		3
SØØ18	IT11H	PARA18	9	1		3
SØØ19	IT11H	PARA19	9	1		3
SØØØ2	IT11H	PARA2	9	1		3
SØØ2Ø	IT11H	PARA2Ø	9	1		3
SØØØ3	IT11H	PARA3	9	1		3
SØØØ4	IT11H	PARA4	9	1		3
SØØØ5	IT11H	PARA5	9	1		3
SØØØ6	IT11H	PARA6	9	1		3
SØØØ7	IT11H	PARA7	9	1		3
SØØØ8	IT11H	PARA8	9	1		3
SØØØ9	IT11H	PARA9	9	1		2
SØØ21	IE93	PARCLK	9	1		2
SØØ22	IE93	PARRST	9	1		3
SØØ2Ø	IT11H	SELØ	9	4		3
SØØ19	IT11H	SEL1	9	4		3
SØØ18	IT11H	SEL2	9	1		3
SØØ17	IT11H	SEL3	9	1		3

FIGURE A2 CONTINUED

```
************************************************************
*          INTERNAL PIN COUNT ERC                          *
*          VERSION  2.8Ø                                   *
************************************************************

   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5ØØØ
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


                CIRCUIT    AVAILABLE
-----------------------------------------
SUM_INT_PINS:      119         3572
-----------------------------------------

Internal pin count is within bounds.
This array is routable.


   No errors found.



************************************************************
*          PIN HOOKUP & UNUSED PINS CHECK ERC              *
*          VERSION  2.8Ø                                   *
************************************************************

   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5ØØØ
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


   No errors found.
```

FIGURE A2 CONTINUED

```
*************************************************************
*          MACRO OCCURRENCE AND POWER DISSIPATION           *
*          VERSION  2.90                                    *
*************************************************************

   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5000
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


        WORST-CASE INTERNAL CURRENT:   19.85 mA
        MAXIMUM INTERNAL CURRENT SPECIFICATION IS: 1383.00 mA


   No errors found.
```

MACRO NAME	# USED	SPECS ICC mA	SPECS IEE mA	TOTALS ICC mA	TOTALS IEE mA
FF13H	1	2.75	0.00	2.75	0.00
GT60L	3	1.26	0.00	3.78	0.00
GT99	1	0.00	0.00	0.00	0.00
IE86	1	0.00	0.00	0.00	0.00
IE93	2	1.35	0.00	2.70	0.00
IEVCC	3	0.00	0.00	0.00	0.00
IT11H	20	1.35	0.00	27.00	0.00
ITGND	3	0.00	0.00	0.00	0.00
ITPWR	3	0.00	0.00	0.00	0.00
MX25H	5	2.07	0.00	10.35	0.00
OE80	1	5.58	0.00	5.58	0.00
OE81	1	5.58	0.00	5.58	0.00
OE87	3	0.00	0.00	0.00	0.00

	ICC mA	IEE mA
TOTAL TYP MACRO CURRENT mA	57.74	0.00
TOTAL TYPICAL POWERED DOWN CURRENT mA	4.68	0.00
TOTAL TYP OVERHEAD CURRENT mA	309.00	0.00
TOTAL TYP CURRENT mA	362.06	0.00
TOTAL MAX CURRENT mA (TYP CURRENT TIMES 1.40) =	506.88	0.00
WORST CASE POWER DISSIPATION VCC (5.5)V X (506.884)mA/1000 VEE (0)V X (0)mA/1000	2.79 WATTS 0.00 WATTS	
ECL OUTPUT POWER DISSIPATION (14.0)mA X 1.3V X (2)outputs/1000	0.04 WATTS	
TOTAL POWER DISSIPATION	2.82 WATTS	

FIGURE A2 CONTINUED

```
**************************************************************
*          CIRCUIT TECHNOLOGY ERC                            *
*          VERSION  2.8Ø                                     *
**************************************************************

   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5ØØØ
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


   No errors found.


**************************************************************
*          ERC report summary                                *
*          VERSION  3.4Ø                                     *
**************************************************************

   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5ØØØ
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


ERC NAME                              ! ERRORS ! WARNINGS
--------------------------------------------------------
Simultanously Switching Output          Ø          Ø
Population                              Ø          Ø
Valid Name Check                        Ø          Ø
Pin Class                               Ø          Ø
Fanout                                  Ø          Ø
Internal Pin Count                      Ø          Ø
Pin hookup and Unused pins              Ø          Ø
Bipolar Macro Occurrence and ...        Ø          Ø
Circuit Technolgy                       Ø          Ø
```

FIGURE A2 CONTINUED

FIGURE A3

AMCCIO.LST

```
*****************************************************************
*          SIGNAL I/O LIST                                      *
*          REVISION  3.10                                       *
*****************************************************************

   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5000
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


*********************************
* SIGNAL I/O LIST               *
*********************************
```

ITEM #	SIGNAL NAME	INSTANCE NAME	MACRO NAME	LOGIC LEVEL	I/O TYPE	SWITCH GROUP	DIFF PAIRS	FAN-IN IIL(uA)	FAN-IN IIH(uA)
1	DAT0	S0001	IIT11H	TTL	I			0.00	0.00
2	DAT1	S0002	IIT11H	TTL	I			0.00	0.00
3	DAT10	S0011	IIT11H	TTL	I			0.00	0.00
4	DAT11	S0012	IIT11H	TTL	I			0.00	0.00
5	DAT12	S0013	IIT11H	TTL	I			0.00	0.00
6	DAT13	S0014	IIT11H	TTL	I			0.00	0.00
7	DAT14	S0015	IIT11H	TTL	I			0.00	0.00
8	DAT15	S0016	IIT11H	TTL	I			0.00	0.00
9	DAT2	S0003	IIT11H	TTL	I			0.00	0.00
10	DAT3	S0004	IIT11H	TTL	I			0.00	0.00
11	DAT4	S0005	IIT11H	TTL	I			0.00	0.00
12	DAT5	S0006	IIT11H	TTL	I			0.00	0.00
13	DAT6	S0007	IIT11H	TTL	I			0.00	0.00
14	DAT7	S0008	IIT11H	TTL	I			0.00	0.00
15	DAT8	S0009	IIT11H	TTL	I			0.00	0.00
16	DAT9	S0010	IIT11H	TTL	I			0.00	0.00
17	EXTCLK	S0021	IIE93	ECL	I			0.00	0.00
18	EXTRST	S0022	IIE93	ECL	I			0.00	0.00
19	IN001	E10000	IIE86	ECL	I			0.00	0.00
20	OUT001	E00000	IOE87	ECL10K	O				
21	OUTC	E0001	IOE87	ECL10K	O				
22	OUTE	E0002	IOE87	ECL10K	O				
23	PARAM	E04000	IOE81	ECL10K	O				
24	SELCT0	S0020	IIT11H	TTL	I			0.00	0.00
25	SELCT1	S0019	IIT11H	TTL	I			0.00	0.00

26	SELCT2	SØØ18	IT11H	TTL	I				Ø.ØØ	Ø.ØØ
27	SELCT3	SØØ17	IT11H	TTL	I				Ø.ØØ	Ø.ØØ
28	YOUTPT	DØØØØ	OE8Ø	ECL1ØK	O	SWGRPA				
29	ITGND	GNTØ1	ITGND	TTL	G					
3Ø	ITGND	GNTØ2	ITGND	TTL	G					
31	ITGND	GNTØ3	ITGND	TTL	G	SWGRPA				
32	ITPWR	PWØØØ	ITPWR	TTL	P	A				
33	ITPWR	PWØØ1	ITPWR	TTL	P	A				
34	ITPWR	PWØØ2	ITPWR	TTL	P	SWGRPA				
35	ITPWR	PWEØØ4	IEVCC	ECL	P					
36	ITPWR	PWEØØ5	IEVCC	ECL	P					
37	ITPWR	PWEØØ6	IEVCC	ECL	P	SWGRPA				
38	ECLIOVCC			5V	P					
39	ECLIOVCC			5V	P					
4Ø	ECLIOVCC			5V	P					
41	ECLIOVCC			5V	P					
42	ECLVCC			5V	P					
43	ECLVCC			5V	P					
44	ECLVCC			5V	P					
45	ECLVCC			5V	P					
46	ECLVEE			ØV	G					
47	ECLVEE			ØV	G					
48	ECLVEE			ØV	G					
49	ECLVEE			ØV	G					
5Ø	TTLGND			ØV	G					
51	TTLGND			ØV	G					
52	TTLGND			ØV	G					
53	TTLGND			ØV	G					
54	TTLGND			ØV	G					
55	TTLGND			ØV	G					
56	TTLGND			ØV	G					
57	TTLGND			ØV	G					
58	TTLVCC			5V	P					
59	TTLVCC			5V	P					
6Ø	TTLVCC			5V	P					
61	TTLVCC			5V	P					

FIGURE A3 CONTINUED

FIGURE A3 CONTINUED

```
**********************************
* I/O LIST SUMMARY               *
**********************************


Total fixed power pins:                12
Total fixed ground pins:               12
Total added power pins:                 6
Total added ground pins:                3

Total input signals:                   23
Total output signals:                   5
Total bidirectional signals:            Ø


**********************************
* SWITCHING GROUPS               *
**********************************

                    !      !           ! ADDED POWER PINS     ! ADDED GROUND PINS
SWITCHING GROUP     !      !   TYPE    ! REQIRED              ! REQUIRED
NAME                ! SIZE ! (ECL/TTL) ! MIN--MAX / SUPPLIED ! MIN--MAX / SUPPLIED
--------------------------------------------------------------------------------
A                     Ø       TTL          Ø -  Ø /    2          Ø -  Ø /    Ø
SWGRPA                Ø       TTL          Ø -  Ø /    1          Ø -  Ø /    1
SWGRPA                1       ECL          Ø -  Ø /    1
--------------------------------------------------------------------------------
TOTAL # SIMULTANEOUSLY SWITCHING TTL OUTPUTS:  Ø
TOTAL # SIMULTANEOUSLY SWITCHING ECL OUTPUTS:  1
------------------------------------------------------------
```

AMCCXREF.LST

FIGURE A4

Date: 16 SEP 88 16:11 File: ERC/AMCCXREF.LST

Signal Cross-Reference

NETLIST SIGNAL NAME	ORIGINAL SIGNAL NAME	SIGNAL PATHNAME	PAGE NUMBER
3S28	!XSIG1	!@MUX16	!4
3S29	!XSIG2	!@MUX16	!4
3S30	!XSIG27	!@MUX16	!4
3S34	!XSIG42	!@MUX16	!4
3S36	!XSIG5	!@MUX16	!4
3S37	!XSIG54	!@MUX16	!4

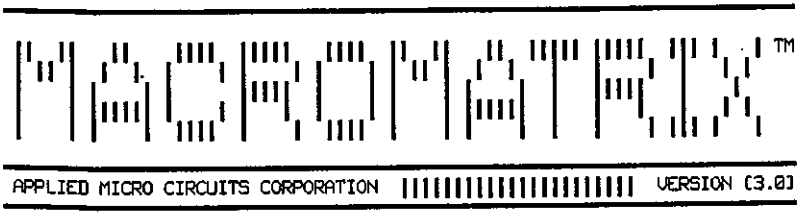
PrePlacement Component Cross-Reference

COMPONENT PATHNAME	PAGE NUMBER	ORIGINAL COMPONENT NAME	NETLIST COMPONENT NAME

Component Cross-Reference

NETLIST COMPONENT NAME	ORIGINAL COMPONENT NAME	COMPONENT PATHNAME	PAGE NUMBER

```
CLASS809> RUN_AMCC
```




```
        1: Part One:   Run DANCE, DRINK, AGIF and ERCs

        2: Part Two:   Run AMCCANN

        3: Part Three: Run SIFT and SOM_MAKER

        4: Part Four:  Run SOM and TCAL

        5: Part Five:  Run AMCCSIMFMT

        6: Part Six:   Run AMCCVRC

        0: Exit Program:

        Please Enter [0 - 6] : >2

        ************** RUNNING AMCCANN **************

        Need to Edit Package Pin Data? (Y or N) ; >Y

AMCC Delay Annotation VERSION  3.30
Loading Netlist ...
Welcome to the output loading system.

(0) Generate a report and exit.
(1) Change the package type.
(2) Edit the default package pin capacitance.
(3) Edit the default system capacitive load for TTL outputs.
(4) Edit the default system capacitive load for ECL outputs.
(5) Edit the system capacitive load for a specific pin or pins.
(6) Edit the package pin capacitance for a specific pin or pins.
(7) Edit the ECL Resistive Load for a specific pin or pins.
(8) Edit the Frequency for a specific pin or pins.
Enter the number of the item you wish to perform:
```

Running AMCCANN

FIGURE A5

```
Date:  16 SEP 88 16:11    File:  ERC/AMCCANN.LST


*************************************************************
*          AMCC Schematic Data Interface                    *
*          Revision [1,Ø]                                   *
*************************************************************

   Netlister version number =              7Ø8
   SDi version number =                    2.1Ø
   Netlist generation date =               19 SEP 1988
   Netlist generation time =               14:25
   Engineering workstation type =          DAISY/DNIX
   Engineering workstation path name =     /USER/CLASS/MUX16
   Product Name =                          MUX16
   Product Number =                        XXXX
   Product Grade =                         MIL
   EWS Library =                           Q5ØØØ
   EWS Library Rev =                       8Ø4
   Macro Parameter family =                Q5ØØØ
   The ARRAY type =                        Q5ØØØT
   Chip Macro Name =                       Q5ØØØTTTL1ØK
   Circuit Family =                        Q5ØØØ
   Circuit Technology =                    P
   ECL Level =                             1ØK



*************************************************************
*          AMCC Delay Annotation                            *
*          VERSION  3.3Ø                                    *
*************************************************************

   Path Name /USER/CLASS/MUX16
   Product Name PRODUCT_NAME
   Circuit family Q5ØØØ
   Circuit technology P
   Date 16 SEP 1988
   Time 12:43
   Product Grade PRODUCT_GRADE


   MIN front annotation file created for DAISY/DNIX
   NOM front annotation file created for DAISY/DNIX
   MIL front annotation file created for DAISY/DNIX

   No errors found.
```

Discard This File

FIGURE A6

```
Date:  14 SEP 88 14:09    File:  ERC/OUTPUT.DLY

pkgkey      1 systtl_cap        15.00 sysecl_cap        10.00 pkgmin_cap        4.00 pkgtyp_cap        5.30 pkgmax_cap        6.20
EXTCLK            0.00
OUT001           10.00          0.00          0.00          0.00        100.00
OUTC             10.00          4.00          5.30          6.20
OUTE             10.00          4.00          5.30          6.20
PARAM            10.00          4.00          5.30          6.20
YOUTPT           10.00          4.00          5.30          6.20
                                12.00         12.00         12.00          0.00        55.00

Date:  16 SEP 88 16:14    File:  ERC/OUTPUT.DLY   * Used in execution

pkgkey      3 systtl_cap        15.00 sysecl_cap         5.00 pkgmin_cap        3.80 pkgtyp_cap        4.40 pkgmax_cap        4.90
EXTCLK            0.00          0.00          0.00          0.00        100.00
OUT001            5.00          3.80          4.40          4.90
OUTC              5.00          3.80          4.40          4.90
OUTE              5.00          3.80          4.40          4.90
PARAM             5.00          3.80          4.40          4.90
YOUTPT            5.00          3.80          4.40          4.90
                                12.00         12.00         12.00          0.00        55.00

Date:  27 AUG 86 13:20    File:  ERC/OUTPUT.DLY

pkgkey     11 systtl_cap        15.00 sysecl_cap         5.00 pkgmin_cap        2.40 pkgtyp_cap        3.00 pkgmax_cap        3.60
DAT0              0.00          0.00          0.00          0.00         80.00
EXTCLK            0.00          0.00          0.00          0.00        100.00
EXTRST            0.00          0.00          0.00          0.00         30.00
OUT001            5.00          2.40          3.00          3.60
OUTC              5.00          2.40          3.00          3.60
OUTE              5.00          2.40          3.00          3.60
PARAM            50.00          2.40          3.00          3.60
YOUTPT           10.00          2.40          3.00          3.60
```

Sample OUTPUT.DLY (data file)

FIGURE A7

AMCCPKG.LST

FIGURE A8

```
Date:  19 SEP 88 14:32   File:  ERC/AMCCPKG.LST

*************************************************************
*          AMCC Output Loading System                       *
*          Version  1.00                                    *
*************************************************************
   Netlister version number =              700
   SDI version number =                    2.10
   Netlist generation date =               19 SEP 1988
   Netlist generation time =               14:25
   Engineering workstation type =          DAISY/DNIX
   Engineering workstation path name =     /USER/CLASS/MUX16
   Product Name =                          MUX16
   Product Number =                        XXXX
   Product Grade =                         NIL
   EWS Library =                           Q5000
   EWS Library Rev =                       004
   Macro Parameter family =                Q5000
   The ARRAY type =                        Q5000T
   Chip Macro Name =                       Q5000TTTL10K
   Circuit Family =                        Q5000
   Circuit Technology =                    P
   ECL Level =                             10K
```

Item #	Signal Name	Instance Name	Macro Name	PAD	Frq MHz	ECL R	System pf	Package Capacitance Min pf	Typ pf	Max pf
1	!DAT0	!S0001	!IT11H	!	!	!	!	!	!	!
2	!DAT1	!S0002	!IT11H	!	!	!	!	!	!	!
3	!DAT10	!S0011	!IT11H	!	!	!	!	!	!	!
4	!DAT11	!S0012	!IT11H	!	!	!	!	!	!	!
5	!DAT12	!S0013	!IT11H	!	!	!	!	!	!	!
6	!DAT13	!S0014	!IT11H	!	!	!	!	!	!	!
7	!DAT14	!S0015	!IT11H	!	!	!	!	!	!	!
8	!DAT15	!S0016	!IT11H	!	!	!	!	!	!	!
9	!DAT2	!S0003	!IT11H	!	!	!	!	!	!	!
10	!DAT3	!S0004	!IT11H	!	!	!	!	!	!	!
11	!DAT4	!S0005	!IT11H	!	!	!	!	!	!	!
12	!DAT5	!S0006	!IT11H	!	!	!	!	!	!	!
13	!DAT6	!S0007	!IT11H	!	!	!	!	!	!	!
14	!DAT7	!S0008	!IT11H	!	!	!	!	!	!	!
15	!DAT8	!S0009	!IT11H	!	!	!	!	!	!	!
16	!DAT9	!S0010	!IT11H	!	!	!	!	!	!	!
17	!EXTCLK	!S0021	!IE93	!	100.0	!	!	!	!	!
18	!EXTRST	!S0022	!IE93	!	!	!	!	!	!	!
19	!INA01	!EI0000	!IE86	!	!	!	!	!	!	!
20	!OUT001	!EO0000	!OE87	!	!	!	5.0	3.80	4.40	4.90
21	!OUTC	!EO001	!OE87	!	!	!	5.0	3.80	4.40	4.90
22	!OUTE	!EO0002	!OE87	!	!	!	5.0	3.80	4.40	4.90
23	!PARAM	!EO4000	!OE81	!	!	!	5.0	3.80	4.40	4.90
24	!SELCT0	!S0020	!IT11H	!	!	!	!	!	!	!
25	!SELCT1	!S0019	!IT11H	!	!	!	!	!	!	!

26	!SELCT2	!S0018	!IT11H										
27	!SELCT3	!S0017	!IT11H										
28	!YOUTPT	!D0000	!OE80			55.0!		5.0!	12.00!	12.00!	12.00!		
29	!ITGND	!GNT003	!ITGND										
30	!ITGND	!GNT002	!ITGND										
31	!ITGND	!GNT001	!ITGND										
32	!ITPWR	!PW0002	!ITPWR										
33	!ITPWR	!PW0001	!ITPWR										
34	!ITPWR	!PW0000	!ITPWR										
35	!IOECLVCC	!PWE006	!IEVCC										
36	!IOECLVCC	!PWE005	!IEVCC										
37	!IOECLVCC	!PWE004	!IEVCC										
38	!ECLIOVCC				139!								
39	!ECLIOVCC				2!								
40	!ECLIOVCC				47!								
41	!ECLIOVCC				94!								
42	!ECLVCC				152!								
43	!ECLVCC				173!								
44	!ECLVCC				60!								
45	!ECLVCC				81!								
46	!ECLVEE				153!								
47	!ECLVEE				172!								
48	!ECLVEE				61!								
49	!ECLVEE				80!								
50	!TTLGND				1!								
51	!TTLGND				140!								
52	!TTLGND				141!								
53	!TTLGND				164!								
54	!TTLGND				48!								
55	!TTLGND				49!								
56	!TTLGND				92!								
57	!TTLGND				93!								
58	!TTLVCC				142!								
59	!TTLVCC				183!								
60	!TTLVCC				50!								
61	!TTLVCC				91!								

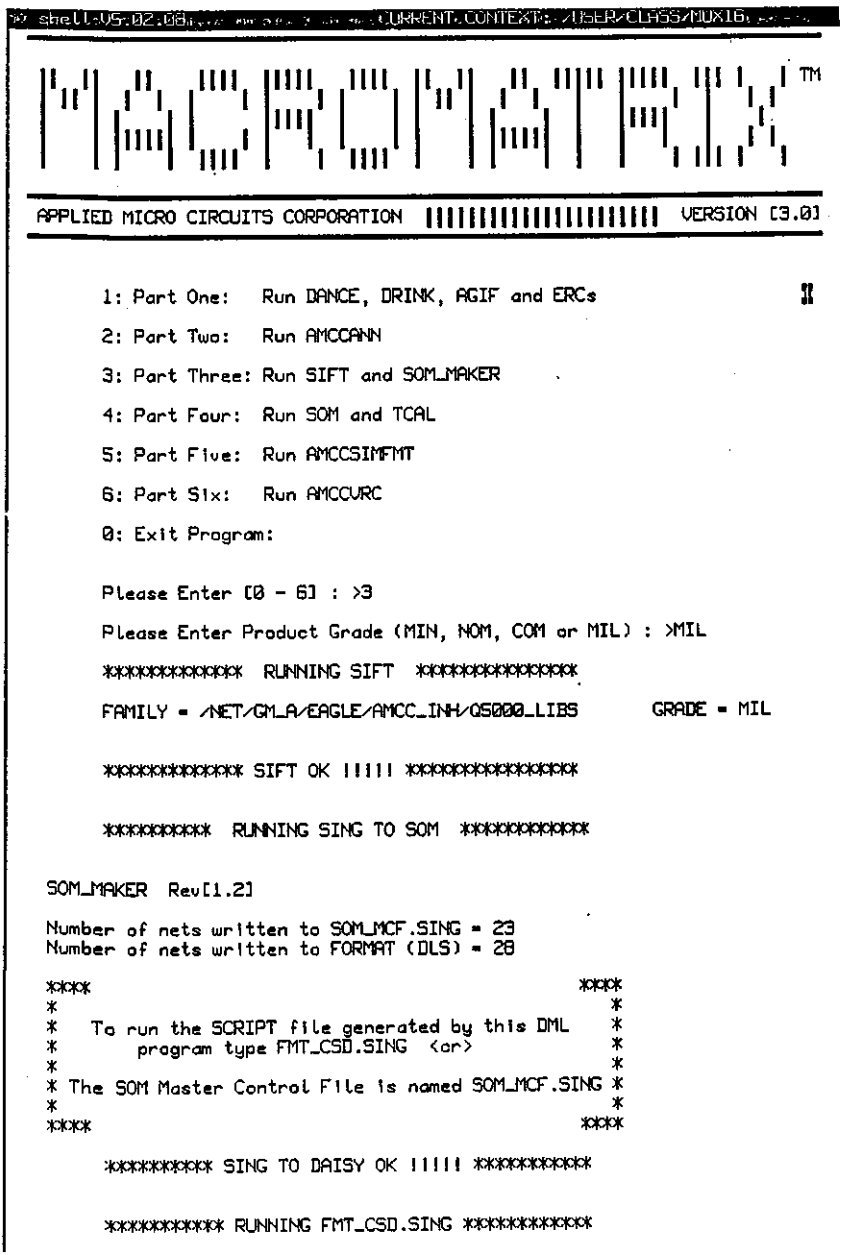
FIGURE A8 CONTINUED

```
Date:  19 SEP 88 14:34    File:  FNTMIL.DSY

/* Daisy design pathname:  /USER/CLASS/MUX16  */
$CONTROL
MODE ADD
SECTION DELAY:N:6
$DELAY
/*                                  R I S E          F A L L          */
/*                                Typ  Min  Max    Typ  Min  Max     */
@MUX16/4:XSIG1      =   Ø    Ø    Ø    Ø    Ø    Ø  ;
@MUX16/4:XSIG2      =   Ø    Ø    Ø    Ø    Ø    Ø  ;
@MUX16/4:XSIG27     =  26   23   28   51   46   56  ;
@MUX16/4:XSIG42     =  26   23   28   51   46   56  ;
@MUX16/4:XSIG5      =   Ø    Ø    Ø    Ø    Ø    Ø  ;
@MUX16/4:XSIG54     =  26   23   28   51   46   56  ;
@MUX16/2:INPØ       =  13   12   14   26   23   28  ;
@MUX16/2:INP1       =  13   12   14   26   23   28  ;
@MUX16/2:INP1Ø      =  13   12   14   26   23   28  ;
@MUX16/2:INP11      =  13   12   14   26   23   28  ;
@MUX16/2:INP12      =  13   12   14   26   23   28  ;
@MUX16/2:INP13      =  13   12   14   26   23   28  ;
@MUX16/2:INP14      =  13   12   14   26   23   28  ;
@MUX16/2:INP15      =  13   12   14   26   23   28  ;
@MUX16/2:INP2       =  13   12   14   26   23   28  ;
@MUX16/2:INP3       =  13   12   14   26   23   28  ;
@MUX16/2:INP4       =  13   12   14   26   23   28  ;
@MUX16/2:INP5       =  13   12   14   26   23   28  ;
@MUX16/2:INP6       =  13   12   14   26   23   28  ;
@MUX16/2:INP7       =  13   12   14   26   23   28  ;
@MUX16/2:INP8       =  13   12   14   26   23   28  ;
@MUX16/2:INP9       =  13   12   14   26   23   28  ;
@MUX16/2:INTCLK     =  26   23   28   26   23   28  ;
@MUX16/2:INTQN      =  13   12   14   26   23   28  ;
@MUX16/2:INTRST     =  26   23   28   26   23   28  ;
@MUX16/2:INTYØ      =  13   12   14   26   23   28  ;
@MUX16/2:INTY1      =  13   12   14   26   23   28  ;
@MUX16/2:INTY2      =  13   12   14   26   23   28  ;
@MUX16/2:INTY3      =  13   12   14   26   23   28  ;
@MUX16/2:INTY4      =  13   12   14   26   23   28  ;
@MUX16/3:PARA1      =  13   12   14   26   23   28  ;
@MUX16/3:PARA1Ø     =  13   12   14   26   23   28  ;
@MUX16/3:PARA11     =  13   12   14   26   23   28  ;
@MUX16/3:PARA12     =  13   12   14   26   23   28  ;
@MUX16/3:PARA13     =  13   12   14   26   23   28  ;
@MUX16/3:PARA14     =  13   12   14   26   23   28  ;
@MUX16/3:PARA15     =  13   12   14   26   23   28  ;
@MUX16/3:PARA16     =  13   12   14   26   23   28  ;
@MUX16/3:PARA17     =  13   12   14   26   23   28  ;
@MUX16/3:PARA18     =  13   12   14   26   23   28  ;
@MUX16/3:PARA19     =  13   12   14   26   23   28  ;
@MUX16/3:PARA2      =  13   12   14   26   23   28  ;
@MUX16/3:PARA2Ø     =  13   12   14   26   23   28  ;
@MUX16/3:PARA3      =  13   12   14   26   23   28  ;
@MUX16/3:PARA4      =  13   12   14   26   23   28  ;
@MUX16/3:PARA5      =  13   12   14   26   23   28  ;
@MUX16/3:PARA6      =  13   12   14   26   23   28  ;
@MUX16/3:PARA7      =  13   12   14   26   23   28  ;
@MUX16/3:PARA8      =  13   12   14   26   23   28  ;
@MUX16/3:PARA9      =  13   12   14   26   23   28  ;
@MUX16/2:PARCLK     =  26   23   28   26   23   28  ;
@MUX16/2:PARRST     =  26   23   28   26   23   28  ;
@MUX16/2:SELØ       =  36   33   4Ø   72   65   8Ø  ;
@MUX16/2:SEL1       =  36   33   4Ø   72   65   8Ø  ;
@MUX16/2:SEL2       =  13   12   14   26   23   28  ;
@MUX16/2:SEL3       =  13   12   14   26   23   28  ;

OUTPUT LOAD DELAYS

@MUX16/4:OUTØØ1     =  56   47   65   46   39   53  ;
@MUX16/4:OUTC       =  56   47   65   46   39   53  ;
@MUX16/4:OUTE       =  56   47   65   46   39   53  ;
@MUX16/4:PARAM      =  56   47   65   46   39   53  ;
@MUX16/2:YOUTPT     =  1Ø1  91   111  83   75   91  ;
$END
```

Front-Annotation

FIGURE A9

APNOTE 1.DNIX A24

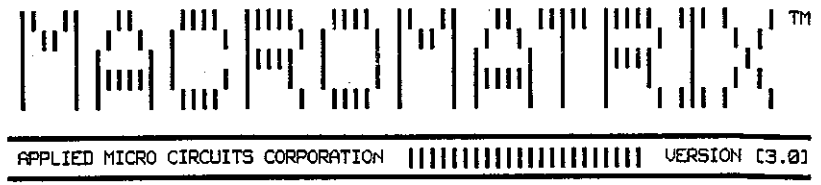


SIFT and SOM_MAKER

FIGURE A10

APNOTE 1.DNIX A25

```
CLASS809> RUN_AMCC
```




```
      1: Part One:   Run DANCE, DRINK, AGIF and ERCs
      2: Part Two:   Run AMCCANN
      3: Part Three: Run SIFT and SOM_MAKER
      4: Part Four:  Run SOM and TCAL
      5: Part Five:  Run AMCCSIMFMT
      6: Part Six:   Run AMCCVRC
      0: Exit Program:

      Please Enter [0 - 6] : >4
      Please Enter SOM Master Control File : >FUNCTION.SING
      Please Enter TCAL Delay File : >FNTMIL.DSY
```

SOM and TCAL
Link For Simulation

FIGURE A11

```
Date:  19 SEP 88 15:46   File:  FUNCTION.SING

/****
*
* DESIGN PATH /USER/CLASS/MUX16   DATE 24 MAY 1988 13:30
*
* COMPANY   ___AMCC__________   CIRCUIT_NAME  __16:1 MUX_
*
* ARRAY    _Q5000 SERIES PO#  ___-_______   REV  ______
*
* DESIGNER _____DEW_________________
*
* What tests does this control file support:  _________
*
* __FUNCTIONAL TESTS - ALL_____________________________
*
* __100 % FAULT GRADE COVERAGE VIA MINIMAL TEST SEQUENCE
*
****/

/***   Configuration section    ****/

$CONFIGURATION

GATE_ACTIVITY_LEVEL := 100;
IMMEDIATE_ACTIVITY_LEVEL := 100;
TIMING_CHECK := 1;

/***  Signal generator section  ****/

$SIGNAL_GENERATORS

@MUX16/3:DAT0  :=  @0:F1,   @40000:F0,   @60000:F1;
@MUX16/3:DAT1  :=  @0:F0,  @460000:F1,  @480000:F0, @1000000:F1, @1020000:F0;
@MUX16/3:DAT2  :=  @0:F0,  @940000:F1,  @960000:F0, @1000000:F1, @1020000:F0;
@MUX16/3:DAT3  :=  @0:F1,  @520000:F0,  @540000:F1;
@MUX16/3:DAT4  :=  @0:F0,  @100000:F1,  @120000:F0, @1000000:F1, @1020000:F0;
@MUX16/3:DAT5  :=  @0:F1,  @400000:F0,  @420000:F1;
@MUX16/3:DAT6  :=  @0:F1,  @880000:F0,  @900000:F1;
@MUX16/3:DAT7  :=  @0:F0,  @580000:F1,  @600000:F0, @1000000:F1, @1020000:F0;
@MUX16/3:DAT8  :=  @0:F0,  @220000:F1,  @240000:F0, @1000000:F1, @1020000:F0;
@MUX16/3:DAT9  :=  @0:F1,  @280000:F0,  @300000:F1;
@MUX16/3:DAT10 :=  @0:F1,  @760000:F0,  @780000:F1;
@MUX16/3:DAT11 :=  @0:F0,  @700000:F1,  @720000:F0, @1000000:F1, @1020000:F0;
@MUX16/3:DAT12 :=  @0:F1,  @160000:F0,  @180000:F1;
@MUX16/3:DAT13 :=  @0:F0,  @340000:F1,  @360000:F0, @1000000:F1, @1020000:F0;
@MUX16/3:DAT14 :=  @0:F0,  @820000:F1,  @840000:F0, @1000000:F1, @1020000:F0;
@MUX16/3:DAT15 :=  @0:F1,  @640000:F0,  @660000:F1;

@MUX16/2:EXTCLK := @0:F0, [10000:F0, 10000:F1]**;

@MUX16/2:EXTRST := @0:F1 , @20000:F0, @1000000:F1, @1020000:F0;

@MUX16/3:SELCT0 := @0:F0, @260000:F1,  @740000:F0, @1000000:F1, @1020000:F0;

@MUX16/3:SELCT1 := @0:F0, @500000:F1,  @980000:F0, @1000000:F1, @1020000:F0;

@MUX16/3:SELCT2 := @0:F0,  @80000:F1,  @200000:F0,
                           @320000:F1,  @440000:F0,
                           @560000:F1,  @680000:F0,
                           @800000:F1,  @920000:F0, @1000000:F1, @1020000:F0;

@MUX16/3:SELCT3 := @0:F0, @140000:F1,  @380000:F0,
                           @620000:F1,  @860000:F0, @1000000:F1, @1020000:F0;
```

FUNCTION.SING: SOM_MCF.SING edited for functional simulation

FIGURE A12

```
/*  SET THERMAL DIODE INPUT STEADY */
@MUX16/4:IN@@1 := @@:F1;

/* ========================================================== */

$OUTPUTS

FILE /USER/CLASS/MUX16/FUNCTION.VLAF <-

/* ---------------------------------------------------- */
/* LIST ALL PRIMARY INPUTS; EXCLUDE THERMAL DIODES,     */
/* MONITOR POINTS AND V8xx MACRO SIGNALS                */
/* ---------------------------------------------------- */

@MUX16/2:EXTCLK, EXTRST,
@MUX16/3:SELCT3, SELCT2, SELCT1, SELCT@,
@MUX16/3:DAT@, DAT1, DAT2, DAT3, DAT4, DAT5, DAT6, DAT7,
@MUX16/3:DAT8, DAT9, DAT1@, DAT11, DAT12, DAT13, DAT14, DAT15,

/* ---------------------------------------------------- */
/* LIST ALL PRIMARY OUTPUTS; EXCLUDE THERMAL DIODES,    */
/* MONITOR POINTS AND V8xx MACRO SIGNALS                */
/* ---------------------------------------------------- */

@MUX16/2:YOUTPT,
@MUX16/4:PARAM;

/* ---------------------------------------------------- */
/* LIST INTERNAL 3-STATE ENABLES, BIDIRECTIONAL         */
/*      ENABLES HERE                                    */
/*   IF ANY                                             */
/* ---------------------------------------------------- */

$END
```

FIGURE A12 CONTINUED

```
APPLIED MICRO CIRCUITS CORPORATION                    VERSION [3.0]

        1: Part One:   Run DANCE, DRINK, AGIF and ERCs

        2: Part Two:   Run AMCCANN

        3: Part Three: Run SIFT and SOM_MAKER

        4: Part Four:  Run SOM and TCAL

        5: Part Five:  Run AMCCSIMFMT

        6: Part Six:   Run AMCCURC

        0: Exit Program:

        Please Enter [0 - 6] : >5
VLAIF Conversion    Rev[1.0]

    Enter VLAIF (input) file name: FUNCTION.VLAF

    Enter SIM (output) file name: FUNCTION.VEC

    Choose from menu -

       1 : VLAIF to SIM FORMAT (NO parenthesis).
       2 : VLAIF to SIM FORMAT (with parenthesis).

    Enter choice [1 or 2]: 1

    Do you want DATA seperated in columns [Y / N] ? Y

       Enter Number of DATA per column: 22

    <<< Processing VLAIF Nets  >>>
    <<< Processing VLAIF Vectors  >>>
    >>>  Time ZERO (0) not output from VLAIF file.
    >>>  (103) lines of Vectors output.

    >>> AMCCSIMFMT conversion completed with NO error(s).
```

AMCCSIMFMT

FIGURE A13

APNOTE 1.DNIX A29

```
Date:  27 AUG 86 12:45    File:  SIMFMTFN.Ø1

1***CIRCUIT IDENTIFICATION =

              EESSSSDDDDDDDDDDDDDDD YP
              XXEEEEAAAAAAAAAAAAAAA OA
              TTLLLLTTTTTTTTTTTTTTT UR
              CRCCCCØ123456789111111 TA
              LSTTTT          Ø12345 PM
              KT321Ø                 T

       TIME

9999          ØIØØØØIØØIØIIØØIIØIØØI ØI
19999         IIØØØØIØØIØIIØØIIØIØØI ØI
29999         ØØØØØØIØØIØIIØØIIØIØØI ØI
39999         IØØØØØIØØIØIIØØIIØIØØI II
49999         ØØØØØØØØØIØIIØØIIØIØØI II
59999         IØØØØØØØØIØIIØØIIØIØØI ØI
69999         ØØØØØØIØØIØIIØØIIØIØØI ØI
79999         IØØØØØIØØIØIIØØIIØIØØI II
89999         ØØØIØØIØØIØIIØØIIØIØØI II
99999         IØØIØØIØØIØIIØØIIØIØØI ØI
1Ø9999        ØØØIØØIØØIIIIØØIIØIØØI ØI
119999        IØØIØØIØØIIIIØØIIØIØØI II
129999        ØØØIØØIØØIØIIØØIIØIØØI II
139999        IØØIØØIØØIØIIØØIIØIØØI ØI
149999        ØØIIØØIØØIØIIØØIIØIØØI ØI
159999        IØIIØØIØØIØIIØØIIØIØØI II
169999        ØØIIØØIØØIØIIØØIIØØØØI II
179999        IØIIØØIØØIØIIØØIIØØØØI ØI
189999        ØØIIØØIØØIØIIØØIIØIØØI ØI
199999        IØIIØØIØØIØIIØØIIØIØØI II
2Ø9999        ØØIØØØIØØIØIIØØIIØIØØI II
219999        IØIØØØIØØIØIIØØIIØIØØI ØI
229999        ØØIØØØIØØIØIIØIIIØIØØI ØI
239999        IØIØØØIØØIØIIØIIIØIØØI II
249999        ØØIØØØIØØIØIIØØIIØIØØI II
259999        IØIØØØIØØIØIIØØIIØIØØI ØI
269999        ØØIØØIIØØIØIIØØIIØIØØI ØI
279999        IØIØØIIØØIØIIØØIIØIØØI II
289999        ØØIØØIIØØIØIIØØØIØIØØI II
299999        IØIØØIIØØIØIIØØØIØIØØI ØI
3Ø9999        ØØIØØIIØØIØIIØØIIØIØØI ØI
319999        IØIØØIIØØIØIIØØIIØIØØI II
329999        ØØIIØIIØØIØIIØØIIØIØØI II
339999        IØIIØIIØØIØIIØØIIØIØØI ØI
349999        ØØIIØIIØØIØIIØØIIØIIØI ØI
359999        IØIIØIIØØIØIIØØIIØIIØI II
369999        ØØIIØIIØØIØIIØØIIØIØØI II
379999        IØIIØIIØØIØIIØØIIØIØØI ØI
389999        ØØØIØIIØØIØIIØØIIØIØØI ØI
399999        IØØIØIIØØIØIIØØIIØIØØI II
4Ø9999        ØØØIØIIØØIØØIØØIIØIØØI II
419999        IØØIØIIØØIØØIØØIIØIØØI ØI
429999        ØØØIØIIØØIØIIØØIIØIØØI ØI
439999        IØØIØIIØØIØIIØØIIØIØØI II
449999        ØØØØØIIØØIØIIØØIIØIØØI II
459999        IØØØØIIØØIØIIØØIIØIØØI ØI
469999        ØØØØØIIIØIØIIØØIIØIØØI ØI
479999        IØØØØIIIØIØIIØØIIØIØØI II
489999        ØØØØØIIØØIØIIØØIIØIØØI II
499999        IØØØØIIØØIØIIØØIIØIØØI ØI
5Ø9999        ØØØØIIIØØIØIIØØIIØIØØI ØI
519999        IØØØIIIØØIØIIØØIIØIØØI II
```

FUNCTION.VEC

FIGURE A14

```
529999      0000111000011001101001  11
539999      1000111000011001101001  01
549999      0000111001011001101001  01
559999      1000111001011001101001  11
569999      0001111001011001101001  11
579999      1001111001011001101001  01
589999      0001111001011101101001  01
599999      1001111001011101101001  11
609999      0001111001011001101001  11
619999      1001111001011001101001  01
629999      0011111001011001101001  01
639999      1011111001011001101001  11
649999      0011111001011001101000  11
659999      1011111001011001101000  01
669999      0011111001011001101001  01
679999      1011111001011001101001  11
689999      0010111001011001101001  11
699999      1010111001011001101001  01
709999      0010111001011001111001  01
719999      1010111001011001111001  11
729999      0010111001011001101001  11
739999      1010111001011001101001  01
749999      0010101001011001101001  01
759999      1010101001011001101001  11
769999      0010101001011001001001  11
779999      1010101001011001001001  01
789999      0010101001011001101001  01
799999      1010101001011001101001  11
809999      0011110100101001101001  11
819999      1011110100101001101001  01
829999      0011110100101001101011  01
839999      1011110100101001101011  11
849999      0011110100101001101001  11
859999      1011110100101001101001  01
869999      0001101001011001101001  01
879999      1001101001011001101001  11
889999      0001101001010001101001  11
899999      1001101001010001101001  01
909999      0001101001011001101001  01
919999      1001101001011001101001  11
929999      0000101001011001101001  11
939999      1000101001011001101001  01
949999      0000101011011001101001  01
959999      1000101011011001101001  11
969999      0000101001011001101001  11
979999      1000101001011001101001  01
989999      0000000100101100110100l  01
999999      1000000100101100110100l  11
1009999     01111111111111111111111  01
1019999     11111111111111111111111  00
1029999     0000000100101100110100l  01
```

FIGURE A14 CONTINUED

```
CLASS809> RUN_AMCC

                                                                    TM
APPLIED MICRO CIRCUITS CORPORATION                    VERSION [3.0]

       1: Part One:   Run DANCE, DRINK, AGIF and ERCs

       2: Part Two:   Run AMCCANN

       3: Part Three: Run SIFT and SOM_MAKER

       4: Part Four:  Run SOM and TCAL

       5: Part Five:  Run AMCCSIMFMT

       6: Part Six:   Run AMCCVRC

       0: Exit Program:

       Please Enter [0 - 6] : >6
AMCCVRC VERSION  3.00

 Enter the SDI file name (input) >  ERC/CIRCUIT.SDI

 Enter the AMCCSIM file name (input) > FUNCTION.VEC



   What type of check do you want to do?
     0) Quit
     1) Race conditions
     2) Simultaneously Switching Outputs
     3) Unknown signals
     4) Signal Toggle check
     5) Required Signal check
     6) Differential Input check
     7) Vector Length check
     9) All but Race (Tests 2 to 7)
    10) All the above (Tests 1 to 7)
    11) Change error limit
   Enter choice (0..11) >10

 Enter the signal analysis file (input)>SIGNAL.DAT


 >>> Creating working files


 ---------- Race CHECK ----------

 >>> phase 1 - phase 2 - phase 3 - phase 4 - phase 5 - phase 6
```

FIGURE A15

AMCCVRC

APNOTE 1.DNIX A32

```
Enter choice (0..11) >10

Enter the signal analysis file (Input)>SIGNAL.DAT

>>> Creating working files

---------- Race CHECK ----------

>>> phase 1 - phase 2 - phase 3 - phase 4 - phase 5 - phase 6

---------- SSO CHECK ----------

>>> phase 1 - phase 2 - phase 3 - phase 4

---------- Unknown signal CHECK ----------

>>> phase 1 - phase 2 - phase 3 - phase 4

---------- Signal Toggle Check ----------

>>> phase 1 - phase 2 - phase 3 - phase 4

---------- Required Signal Check ----------

>>> phase 1 - phase 2 - phase 3 - phase 4

---------- DIFFIP CHECK ----------

>>> phase 1 - phase 2 - phase 3 - phase 4

---------- Vector Length Check ----------

>>> phase 1

   What type of check do you want to do?
     0) Quit
     1) Race conditions
     2) Simultaneously Switching Outputs
     3) Unknown signals
     4) Signal Toggle check
     5) Required Signal check
     6) Differential Input check
     7) Vector Length check
     9) All but Race (Tests 2 to 7)
    10) All the above (Tests 1 to 7)
    11) Change error limit
   Enter choice (0..11) >0
```

FIGURE A15 CONTINUED

SIGNAL ANALYSIS FILE

```
        Date:  19 SEP 88 14:31    File:  SIGNAL.DAT
        EXTCLK + EXCEPT!
```

```
Date:  19 SEP 88 10:13    File:  AMCCVRC.LST


************************************************************
*          Race Condition Checker                          *
*          VERSION  2.90                                   *
************************************************************


   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5000
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


   No errors found.



************************************************************
*          Simultaneously Switching Output Checker         *
*          VERSION  2.90                                   *
************************************************************


   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5000
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


   No errors found.


************************************************************
*          Unknown Signal State Checker                    *
*          VERSION  2.90                                   *
************************************************************


   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5000
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


   No errors found.
```

AMCCVRC.LST

FIGURE A16

```
*************************************************************
*          Differential Input Checker                       *
*          VERSION  2.9Ø                                    *
*************************************************************

   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5ØØØ
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


 The following signals are differential:


   No errors found.


*************************************************************
*          REQUIRED SIGNAL CHECK                            *
*          VERSION  2.9Ø                                    *
*************************************************************

   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5ØØØ
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL




   No errors found.


*************************************************************
*          Signal Toggle Check                              *
*          VERSION  2.9Ø                                    *
*************************************************************

   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5ØØØ
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


   No errors found.
```

FIGURE A16 CONTINUED

```
**********************************************************
*          Vector Length Check                           *
*          VERSION  3.ØØ                                 *
**********************************************************

   Path Name /USER/CLASS/MUX16
   Product Name MUX16
   Circuit family Q5ØØØ
   Circuit technology P
   Date 19 SEP 1988
   Time 14:25
   Product Grade MIL


   No errors found.
```

```
**********************************************************
*          VRC report summary                            *
*          VERSION  3.ØØ                                 *
**********************************************************

    Path Name /USER/CLASS/MUX16
    Product Name MUX16
    Circuit family Q5ØØØ
    Circuit technology P
    Date 19 SEP 1988
    Time 14:25
    Product Grade MIL


Test number  1  Had   Ø  Errors
Test number  2  Had   Ø  Errors
Test number  3  Had   Ø  Errors
Test number  4  Had   Ø  Errors
Test number  5  Had   Ø  Errors
Test number  6  Had   Ø  Errors
Test number  7  Had   Ø  Errors
```

FIGURE A16 CONTINUED

```
Date:  30 AUG 86 12:49   File:  SIMFMTAS.01

1***CIRCUIT IDENTIFICATION =

                EESSSSDDDDDDDDDDDDDDDD YP
                XXEEEEAAAAAAAAAAAAAAAA OA
                TTLLLLTTTTTTTTTTTTTTTT UR
                CRCCCC0123456789111111 TA
                LSTTTT           012345 PM
                KT3210                  T

        TIME

499             0100001001011001101001 01
999             1100001001011001101001 01
1499            0000001001011001101001 01
1999            1000001001011001101001 01
2499            0000000001011001101001 11
2999            1000000001011001101001 01
3499            0000001001011001101001 01
3999            1000001001011001101001 01
4499            0001001001011001101001 11
4999            1001001001011001101001 01
5499            0001001001111001101001 01
5999            1001001001111001101001 01
6499            0001001001011001101001 11
6999            1001001001011001101001 01
7499            0011001001011001101001 01
7999            1011001001011001101001 01
8499            0011001001011001100001 11
8999            1011001001011001100001 01
9499            0011001001011001101001 01
9999            1011001001011001101001 01
10499           0010001001011001101001 11
10999           1010001001011001101001 01
11499           0010001001011011101001 01
11999           1010001001011011101001 01
12499           0010001001011001101001 11
12999           1010001001011001101001 01
13499           0010011001011001101001 01
13999           1010011001011001101001 01
14499           0010011001011000101001 11
14999           1010011001011000101001 01
15499           0010011001011001101001 01
15999           1010011001011001101001 01
16499           0011011001011001101001 11
16999           1011011001011001101001 01
17499           0011011001011001101101 01
17999           1011011001011001101101 01
18499           0011011001011001101001 11
18999           1011011001011001101001 01
19499           0001011001011001101001 01
19999           1001011001011001101001 01
20499           0001011001001001101001 11
20999           1001011001001001101001 01
21499           0001011001011001101001 01
21999           1001011001011001101001 01
22499           0000011001011001101001 11
22999           1000011001011001101001 01
23499           0000011101011001101001 01
23999           1000011101011001101001 01
24499           0000011001011001101001 11
24999           1000011001011001101001 01
25499           0000111001011001101001 01
25999           1000111001011001101001 01
```

SAMPLED AT-SPEED

FIGURE A17

```
26499       0000111100001100110100111
26999       1000111100001100110100101
27499       0000111001101100110100101
27999       1000111001101100110100101
28499       0001111001101100110100111
28999       1001111001101100110100101
29499       0001111001101110110100101
29999       1001111001101110110100101
30499       0001111001101100110100111
30999       1001111001101100110100101
31499       0011111001101100110100101
31999       1011111001101100110100101
32499       0011111001101100110100011
32999       1011111001101100110100001
33499       0011111001101100110100101
33999       1011111001101100110100101
34499       0010111001101100110100111
34999       1010111001101100110100101
35499       0010111001101100111100101
35999       1010111001101100111100101
36499       0010111001101100110100111
36999       1010111001101100110100101
37499       0010101001101100110100101
37999       1010101001101100110100101
38499       0010101001101100100100111
38999       1010101001101100100100101
39499       0010101001101100110100101
39999       1010101001101100110100101
40499       0011101001101100110100111
40999       1011101001101100110100101
41499       0011101001101100110101111
41999       1011101001101100110101111
42499       0011101001101100110100111
42999       1011101001101100110100101
43499       0001101001101100110100101
43999       1001101001101100110100101
44499       0001101001010001101000111
44999       1001101001010001101000101
45499       0001101001011001101000101
45999       1001101001011001101000101
46499       0000101001011001101000111
46999       1000101001011001101000101
47499       0000101011011001101000101
47999       1000101011011001101000101
48499       0000101001011001101000111
48999       1000101001011001101000101
49499       0000001001011001101000101
49999       1000001001011001101000101
```

FIGURE A17 CONTINUED

```
Date:  19 SEP 88 15:48    File:  ATSPEED_POC.SING

/****
*
* DESIGN PATH /USER/CLASS/MUX16    DATE 12 FEB 1986 13:30
*
* COMPANY  ___AMCC__________    CIRCUIT_NAME  __16:1 MUX_
*
* ARRAY    _Q5000 SERIES PO#  ___-_______    REV  ______
*
* DESIGNER _____DEW_____________________
*
* What tests does this control file support:  _________
*
* __ATSPEED    TESTS - ALL PATHS _____________________
*      70/30 CLOCK
****/

/***   Configuration section    ****/

$CONFIGURATION

GATE_ACTIVITY_LEVEL := 100;
IMMEDIATE_ACTIVITY_LEVEL := 100;
TIMING_CHECK := 1;

/***  Signal generator section  ****/

$SIGNAL_GENERATORS

@MUX16/3:DAT0  :=  @0:F1,   @2000:F0,   @3000:F1;
@MUX16/3:DAT1  :=  @0:F0,   @23000:F1,  @24000:F0;
@MUX16/3:DAT2  :=  @0:F0,   @47000:F1,  @48000:F0;
@MUX16/3:DAT3  :=  @0:F1,   @26000:F0,  @27000:F1;
@MUX16/3:DAT4  :=  @0:F0,   @5000:F1,   @6000:F0;
@MUX16/3:DAT5  :=  @0:F1,   @20000:F0,  @21000:F1;
@MUX16/3:DAT6  :=  @0:F1,   @44000:F0,  @45000:F1;
@MUX16/3:DAT7  :=  @0:F0,   @29000:F1,  @30000:F0;
@MUX16/3:DAT8  :=  @0:F0,   @11000:F1,  @12000:F0;
@MUX16/3:DAT9  :=  @0:F1,   @14000:F0,  @15000:F1;
@MUX16/3:DAT10 :=  @0:F1,   @38000:F0,  @39000:F1;
@MUX16/3:DAT11 :=  @0:F0,   @35000:F1,  @36000:F0;
@MUX16/3:DAT12 :=  @0:F1,   @8000:F0,   @9000:F1;
@MUX16/3:DAT13 :=  @0:F0,   @17000:F1,  @18000:F0;
@MUX16/3:DAT14 :=  @0:F0,   @41000:F1,  @42000:F0;
@MUX16/3:DAT15 :=  @0:F1,   @32000:F0,  @33000:F1;

@MUX16/2:EXTCLK := @0:F0, [700:F0, 300:F1]**;

@MUX16/2:EXTRST := @0:F1 , @1000:F0;

@MUX16/3:SELCT0 := @0:F0, @13000:F1,  @37000:F0;

@MUX16/3:SELCT1 := @0:F0, @25000:F1,  @49000:F0;

@MUX16/3:SELCT2 := @0:F0,  @4000:F1,  @17000:F0,
                           @16000:F1,  @22000:F0,
                           @28000:F1,  @34300:F0,
                           @40000:F1,  @46000:F0;

@MUX16/3:SELCT3 := @0:F0,  @7000:F1,  @19000:F0,
                           @31000:F1,  @43000:F0;

@MUX16/4:IN001 := @0:F1;

/* ================================================== */

$OUTPUTS
PRINT_ON_CHANGE

FILE /USER/CLASS/MUX16/ATSPEED.VLAF <-
@MUX16/2:EXTCLK, EXTRST,

@MUX16/3:SELCT3, SELCT2, SELCT1, SELCT0,

@MUX16/3:DAT0, DAT1, DAT2, DAT3, DAT4, DAT5, DAT6, DAT7,
@MUX16/3:DAT8, DAT9, DAT10, DAT11, DAT12, DAT13, DAT14, DAT15,

@MUX16/2:YOUTPT,
@MUX16/4:PARAM;

$END
```

FIGURE A18

SOM_MCF.SING edited for AT-SPEED PRINT-ON-CHANGE

```
Date:  30 AUG 86 13:06    File:  POCFMTAS.01

1***CIRCUIT IDENTIFICATION =

                EESSSSDDDDDDDDDDDDDDD YP
                XXEEEEAAAAAAAAAAAAAAA OA
                TTLLLLTTTTTTTTTTTTTTT UR
                CRCCCC0123456789111111 TA
                LSTTTT          012345 PM
                KT3210                 T

        TIME

700             11000001001011001101001 01
1000            00000001001011001101001 01
1700            10000001001011001101001 01
2000            00000000001011001101001 01
2063            00000000001011001101001 11
2700            10000000001011001101001 11
3000            00000001001011001101001 11
3018            00000001001011001101001 01
3700            10000001001011001101001 01
4000            00010010010110011101001 01
4063            00010010010110011101001 11
4700            10010010010110011101001 11
5000            00010010011110011101001 11
5018            00010010011110011101001 01
5700            10010010011110011101001 01
6000            00010010010110011101001 01
6063            00010010010110011101001 11
6700            10010010010110011101001 11
7000            00110010010110011101001 11
7018            00110010010110011101001 01
7700            10110010010110011101001 01
8000            00110010010110011100001 01
8063            00110010010110011100001 11
8700            10110010010110011100001 11
9000            00110010010110011101001 11
9018            00110010010110011101001 01
9700            10110010010110011101001 01
10000           00100010010110011101001 01
10063           00100010010110011101001 11
10700           10100010010110011101001 11
11000           00100010010110111101001 11
11018           00100010010110111101001 01
11700           10100010010!10111101001 01
12000           00100010010110011101001 01
12063           00100010010110011101001 11
12700           10100010010110011101001 11
13000           00100110010110011101001 11
13018           00100110010110011101001 01
13700           10100110010110011101001 01
14000           00100110010110000101001 01
14063           00100110010110000101001 11
14700           10100110010110000101001 11
15000           00100110010110011101001 11
15018           00100110010110011101001 01
15700           10100110010110011101001 01
16000           00110110010110011101001 01
16063           00110110010110011101001 11
16700           10110110010110011101001 11
17000           00110110010110011101101 11
17018           00110110010110011101101 01
17700           10110110010110011101101 01
18000           00110110010110011101001 01
```

PRINT-ON-CHANGE

AT-SPEED

FIGURE A19

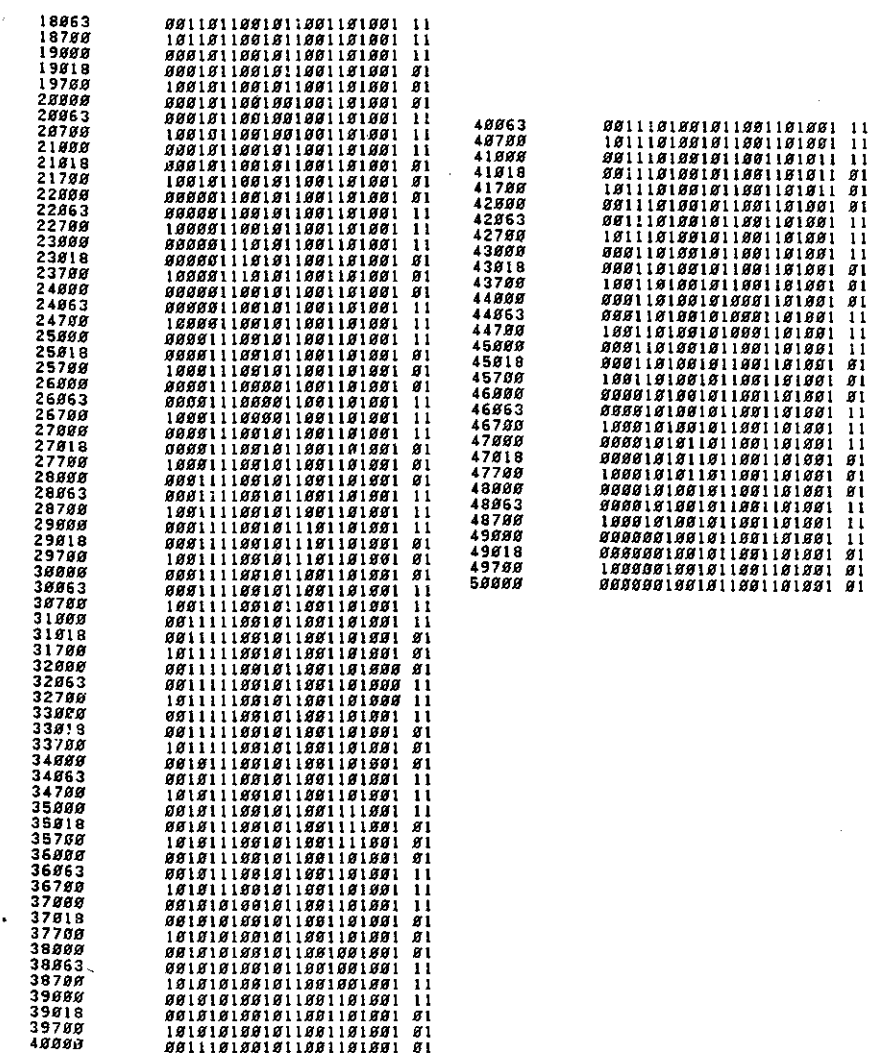


FIGURE A19 CONTINUED

```
Date:  19 SEP 88 14:48   File:  PARAMETER.SING

/****
*
* DESIGN PATH /USER/CLASS/MUX16   DATE 24 MAY 1988 13:30
*
* COMPANY  ___AMCC_____________   CIRCUIT_NAME  __16:1 MUX_
*
* ARRAY    _Q5000 SERIES PO#  ____-________   REV  _______
*
* DESIGNER _____DEW____________________
*
* What tests does this control file support:  _________
*
* __PARAMETRIC TESTS - ALL_____________________________
*
****/

/***   Configuration section    ****/

$CONFIGURATION

GATE_ACTIVITY_LEVEL := 100;
IMMEDIATE_ACTIVITY_LEVEL := 100;
TIMING_CHECK := 1;

/***  Signal generator section  ****/

$SIGNAL_GENERATORS

@MUX16/3:DAT0  :=  @0:F1,   @100000:F0,   @200000:F1;
@MUX16/3:DAT1  :=  @0:F1,   @300000:F0,   @400000:F1;
@MUX16/3:DAT2  :=  @0:F1,   @500000:F0,   @600000:F1;
@MUX16/3:DAT3  :=  @0:F1,   @700000:F0,   @800000:F1;
@MUX16/3:DAT4  :=  @0:F1,   @900000:F0,  @1000000:F1;
@MUX16/3:DAT5  :=  @0:F1,  @1100000:F0,  @1200000:F1;
@MUX16/3:DAT6  :=  @0:F1,  @1300000:F0,  @1400000:F1;
@MUX16/3:DAT7  :=  @0:F1,  @1500000:F0,  @1600000:F1;
@MUX16/3:DAT8  :=  @0:F1,  @1700000:F0,  @1800000:F1;
@MUX16/3:DAT9  :=  @0:F1,  @1900000:F0,  @2000000:F1;
@MUX16/3:DAT10 :=  @0:F1,  @2100000:F0,  @2200000:F1;
@MUX16/3:DAT11 :=  @0:F1,  @2300000:F0,  @2400000:F1;
@MUX16/3:DAT12 :=  @0:F1,  @2500000:F0,  @2600000:F1;
@MUX16/3:DAT13 :=  @0:F1,  @2700000:F0,  @2800000:F1;
@MUX16/3:DAT14 :=  @0:F1,  @2900000:F0,  @3000000:F1;
@MUX16/3:DAT15 :=  @0:F1,  @3100000:F0,  @3200000:F1;

@MUX16/2:EXTCLK := @0:F1, @3300000:F0,  @3400000:F1;

@MUX16/2:EXTRST := @0:F1, @3500000:F0,  @3600000:F1;

@MUX16/3:SELCT0 := @0:F1, @3700000:F0,  @3800000:F1;

@MUX16/3:SELCT1 := @0:F1, @3900000:F0,  @4000000:F1;

@MUX16/3:SELCT2 := @0:F1, @4100000:F0,  @4200000:F1;

@MUX16/3:SELCT3 := @0:F1, @4300000:F0,  @4400000:F1;

@MUX16/4:IN001 := @0:F1;

/* ============================================================ */
```

SOM_MCF.SING edited for Parametric Vectors

FIGURE A20

```
$OUTPUTS

FILE /USER/CLASS/MUX16/FUNCTION.VLAF <-

/* ------------------------------------------------- */
/* LIST ALL PRIMARY INPUTS; EXCLUDE THERMAL DIODES,  */
/* MONITOR POINTS AND VBxx MACRO SIGNALS             */
/* ------------------------------------------------- */

@MUX16/2:EXTCLK, EXTRST,
@MUX16/3:SELCT3, SELCT2, SELCT1, SELCTØ,
@MUX16/3:DATØ, DAT1, DAT2, DAT3, DAT4, DAT5, DAT6, DAT7,
@MUX16/3:DAT8, DAT9, DAT1Ø, DAT11, DAT12, DAT13, DAT14, DAT15,

/* ------------------------------------------------- */
/* LIST ALL PRIMARY OUTPUTS; EXCLUDE THERMAL DIODES, */
/* MONITOR POINTS AND VBxx MACRO SIGNALS             */
/* ------------------------------------------------- */

@MUX16/2:YOUTPT,
@MUX16/4:PARAM;

/* ------------------------------------------------- */
/* LIST INTERNAL 3-STATE ENABLES AND BIDIRECTIONAL   */
/*   ENABLES HERE                                    */
/*   IF ANY                                          */
/* ------------------------------------------------- */

$END
```

FIGURE A20 CONTINUED

```
Date:  26 AUG 86 11:54    File:  SIMFMTPR.Ø1

1***CIRCUIT IDENTIFICATION =

                EESSSSDDDDDDDDDDDDDDD YP
                XXEEEEAAAAAAAAAAAAAAA OA
                TTLLLLTTTTTTTTTTTTTTT UR
                CRCCCCØ123456789111111 TA
                LSTTTT           Ø12345 PM
                KT321Ø                 T

        TIME

9999            111111111111111111111  ØØ
19999           111111Ø1111111111111111 Ø1
29999           111111111111111111111  ØØ
39999           111111Ø1111111111111111 Ø1
49999           111111111111111111111  ØØ
59999           111111110111111111111  Ø1
69999           111111111111111111111  ØØ
79999           111111111Ø1111111111111 Ø1
89999           111111111111111111111  ØØ
99999           111111111Ø1111111111111 Ø1
1Ø9999          111111111111111111111  ØØ
119999          111111111Ø1111111111111 Ø1
129999          111111111111111111111  ØØ
139999          111111111111Ø1111111111 Ø1
149999          111111111111111111111  ØØ
159999          111111111111Ø1111111111 Ø1
169999          111111111111111111111  ØØ
179999          111111111111Ø1111111111 Ø1
189999          111111111111111111111  ØØ
199999          111111111111111Ø111111 Ø1
2Ø9999          111111111111111111111  ØØ
219999          111111111111111Ø111111 Ø1
229999          111111111111111111111  ØØ
239999          111111111111111Ø11111 Ø1
249999          111111111111111111111  ØØ
259999          111111111111111Ø1111 Ø1
269999          111111111111111111111  ØØ
279999          111111111111111Ø1111 Ø1
289999          111111111111111111111  ØØ
299999          111111111111111111Ø1 Ø1
3Ø9999          111111111111111111111  ØØ
319999          111111111111111111111Ø Ø1
329999          111111111111111111111  ØØ
339999          Ø1111111111111111111111 Ø1
349999          111111111111111111111  ØØ
359999          1Ø1111111111111111111111 Ø1
369999          111111111111111111111  ØØ
379999          111111Ø1111111111111111 Ø1
389999          111111111111111111111  ØØ
399999          111110111111111111111111 Ø1
4Ø9999          111111111111111111111  ØØ
419999          1110111111111111111111 Ø1
429999          111111111111111111111  ØØ
439999          11Ø1111111111111111111 Ø1
449999          111111111111111111111  ØØ
```

Parametric Vectors

(Sampled only)

FIGURE A21