Section 8:

MacroMatrix Guide

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INTRODUCTION

The AMCC Design Validation Document includes the design checks that must be made prior to submitting a design to AMCC for the final design review. A design validation review is required for all designs. The checks must be completed by the designer for all designs done with the aid of an engineering workstation (EWS), either the DAISY, MENTOR or VALID Systems EWS, or done with any VAX/VMS system which is used to provide a LASAR 6 netlist.

For AMCC-Implemented designs, AMCC implementation engineering is responsible for the checks.

The AMCC design validation software, part of the MacroMatrix package and also known as the Engineering Rules Checks (ERC) software, performs many of these checks on a captured design netlist and creates an output file that lists the flagged errors and supplies valuable design documentation. In many cases, the process of reviewing the ERC output and redesigning to remove errors flagged will increase the probability of a buildable, testable, successful circuit. AMCC recommends that the designer review the design validation document prior to starting a design.

Hardcopy ERC reports and the written resolution of any outstanding errors or warnings are required documentation for any design submission.

AVAILABILITY

ERC sofware is available for the DAISY, MENTOR and VALID engineering workstations where it is system-resident.

ERC software is available for LASAR Version 6 netlist designs using a VAX/VMS system.

SCHEMATIC REQUIREMENTS

The ERC software requires that the schematic contain one chip macro and that the required parameters for that chip macro be supplied in accordance with the workstation and netlist procedures.

All EWS schematics must follow the rules and conventions as defined in Section 3, EWS Schematic Rules and Conventions.

AMCC GENERIC INTERFACE FORMAT

A special file called the AMCC Generic Interface Format file (AGIF) is used to transfer a design from any approved EWS to the VAX for ERC support, LASAR 6 simulation development, test program support, LASAR 6 fault-grading, and layout. This file is created by AMCC MacroMatrix support software on the individual workstations and is called **CIRCUIT.SDI**. The EWS-VAX interface software is unique to each workstation, converting that particular netlist format into the AGIF netlist format.

The AGIF netlist and the macro library parameter file together are used as source data to the ERC software.

During AGIF netlist generation, error messages are generated both on the screen and written to the error file on the workstation. These errors are documented here along with the probable cause of the error.

If error conditions have occurred during the AGIF netlist generation, any software operating upon the AGIF netlist (AMCCERC, AMCCANN, AMCCSIMFMT, AMCCVRC) will not run correctly.

Contact AMCC if you are unable to debug and run without errors.

ENGINEERING RULES CHECKS SUMMARY

- FAN-OUT - (ALL)

Verifies that macro fan-out limits are not exceeded. Counts any pin with a fan-in greater than 1 correctly. Provides a fan-out table listing all signal, their fan-out limits, the derating used, if any, and their fan-out load. Checks for excessive loading over a derated fan-out limit.

- HOOK-UP CHECK (MACRO PIN HOOK-UP) - (BIPOLAR, BiCMOS interface)

Checks to make sure that pins which must be connected are "hooked-up" to a valid signal. (Macro pins that must be driven by another macro cannot be grounded.) This check is combined with the unused pins check.

- INTERNAL PIN COUNT - (ALL) Counts all routable internal macro pins on a design and returns the total per page and overall total from the design. Counts unconnected pins under the assumption that they should have been connected somewhere. Does NOT count grounded (BIPOLAR) connections for BIPOLAR. Does NOT count terminated macro pins since these are not routed. Provides an error message when the internal pin count exceeds array limits for an acceptable array (RISKY, VERY RISKY, UNACCEPTABLE).

- MACRO OCCURRENCE AND POWER DISSIPATION TABLE (BIPOLAR)
  MACRO OCCURRENCE AND INTERFACE
  POWER DISSIPATION TABLES (BiCMOS; Q20000 Series)

Gives the user a macro usage and macro current table, and computes the worst-case power dissipation based on typical-case assumptions as to the power supply and ECL termination, and duty cycle. For the Q3500 and Q5000 Series, computes the correct worst-case current multiplier based on internal cell utilization. The power dissipation table applies to the AMCC SPEC.

Computes the internal current used for Bipolar arrays and verifies that the internal current is not excessive for the array.

The BiCMOS form of the report provides a list of macros and space for switching frequency to support customer computation. The Q20000 form provides a complete table with power computation for the interface macros and a second macro occurrence table for the internal macros. At present, the designer must compute the AC power for all Q20000 arrays and for the internal macro power dissipation portion of the BiCMOS arrays.

- PIN CLASS - (ALL)
- WIRE-OR - (BIPOLAR)

Verifies that all pins for a given net are compatible. Signal class parameters are used to enforce pin restrictions. The driving macro pin signal class is checked against all driven pin signal classes. Currently does NOT check to see if a PO (output PAD) pin is connected to internal macro pins, grounded or terminated. Currently does NOT check to see if a PI (input PAD) is driven by an internal pin, grounded or terminated. (Future ERC)

Validates that all component wire-ORs are connected correctly and that the wire-OR is correctly used. Wire-OR checks are also part of other ERCs (such as fan-out).

- POPULATION - (ALL)

Determines internal and interface cell population for a given design, provides a table of usage, and gives the internal cell utilization percentage, used in determining routability and issues a warning if the cell utilization is excessive. Provides a count of the cells used by type and the limits for the array and flags violations.

Includes a total array pad count check and a count of power and ground.

- POPULATION STATISTICS - (ALL)

Expands the detail of the population report to call out 3-state enable drivers that carry a ground connection (such as OT59), internal 3-state drivers without ground, thermal diodes, AC monitor points and VBxx macros.

• SIMULTANEOUSLY SWITCHING OUTPUTS
Simultaneously switching outputs are counted if they are tagged on the schematics by the designer via the SWGROUP parameter. Checks that the number of added power and ground pins are adequate based on the number of simultaneously switching outputs and the array and I/O mode. Issues a warning if less than worst-case placement maximums would require and an error if less than the best-case placement.

• TECHNOLOGY - (BIPOLAR, BiCMOS)
• ECL 10K/100K - (BIPOLAR, BiCMOS)
Validates that all components used are consistent with the specified array, I/O mode and ECL type as specified by the chip macro selected.

• VALIDNAMES - (ALL) Checks some of the more common naming errors in support of those checks provided by the individual work-stations or netlist software. Checks for the use of keywords that could interfere with support software (e.g., INPUT, OUTPUT). Checks duplicate naming. Checks for name length for the type (instance or signal). Checks that the first character is alpha or numeric. Checks that no special characters were used.

• VTI CHECK
Computes the number of VTI threshold generator loads and states them for those arrays which require a check. Indicates if the loading is excessive for the array. (This check only applies to Q700 Series Arrays.)

• UNUSED MACRO PINS - (ALL)
Checks a design for dangling pins (pins which are not connected, not grounded and not terminated).

ERC REPORT HEADER

The following information is printed out on page one of the ERC report. This information is used to identify the circuit, the system it is being executed on and the version of the software to allow faster debug and support of problems encountered during its use.

PRODUCT_NAME	Defined by the user; chip macro parameter; code-name
DEVICE_NUMBER	Defined by the user; chip macro parameter; device number
PRODUCT_GRADE	Defined by the user; chip macro parameter; MIL or COM
CIRCUIT_FAMILY	Chip macro parameter; series identification
ARRAY_TYPE	Chip macro parameter; specific array in that series
CIRCUIT_TECHNOLOGY	Chip macro parameter; T, E, M , P
ECL_LEVEL	Chip macro parameter; ECL 10K or ECL 100K
POWER_SUPPLY	Defined by the user; optional chip macro parameter; 5VREF, STD4 or STD5
MACRO_NAME	Chip macro name parameter
EWS_LIBRARY	Software parameter
EWS_LIBRARY_REV	Software parameter
MAC_PARM_FAMILY	Software parameter; array series
MPF_VERSION	Software parameter
EWS_TYPE	Software parameter; EWS station
EWS_DATE	Software parameter; date of run
EWS_TIME	Software parameter; time of run
EWS_PATH_NAME	Software parameter; network node and directory ID
NETLISTER_VERSION	Software parameter
SDI_VERSION	Software parameter
MPF_INTERFACE_VERSION	Software parameter

The ERCs will generate an error message if required parameters are missing from the submitted circuit.

```
**************************************************************
*          AMCC Schematic Data Interface                     *
*          Revision [1.0]                                    *
**************************************************************
```

Netlister version number =	708
SDI version number =	2.6
Netlist generation date =	9 JUN 1986
Netlist generation time =	13:3
Engineering workstation type =	DAISY/DNIX
Engineering workstation path name =	/USER/CLASS/ERRORS
Product Name =	PRODUCT_NAME <-----
Product Number =	DEVICE_NUMBER <-----
Product Grade =	PRODUCT_GRADE <-----
EWS Library =	Q3500
EWS Library Rev =	705
Macro Parameter family =	Q3500
The ARRAY type =	Q2400S
Chip Macro Name =	Q2400SECL10K
Circuit Family =	Q3500
Circuit Technology =	E
ECL Level =	10K

<---- indicates defaulted parameters
Parameters for the chip macros should be defined
by the user.

```
************************************************************
*          AMCC Schematic Data Interface                   *
*          Revision [1.Ø]                                  *
************************************************************

   Netlister version number =              7Ø8
   SDI version number =                    2.1Ø
   Netlist generation date =                7 OCT 1988
   Netlist generation time =               1Ø:39
   Engineering workstation type =          DAISY/DNIX
   Engineering workstation path name =     /USER/CLASS/Q532REG
   Product Name =                          Q5REG32
   Product Number =                        XXXX
   Product Grade =                         MIL
   EWS Library =                           Q5ØØØ
   EWS Library Rev =                       8Ø9
   Macro Parameter family =                Q5ØØØ
   The ARRAY type =                        Q35ØØT
   Chip Macro Name =                       Q35ØØTMIX1ØK
   Circuit Family =                        Q5ØØØ
   Circuit Technology =                    M
   ECL Level =                             1ØK
   Power Supply =                          STD5
```

GENERIC PARAMETERS

Refer to the EWS-Specific Installation document, Volume II, Section 7, for instructions on how to define a parameter for a given EWS system.

CIRCUIT_FAMILY, ARRAY_TYPE

The following AMCC arrays are supported by the MacroMatrix software:

CIRCUIT_FAMILY parameter	ARRAY_TYPE parameter	
Q5000	Q5000T	
	Q3500T	
	QM1600T	
	Q1300T	
Q3500	Q3500S	
	Q2400S	
	QM1600S	
	Q1300S	
Q14000	Q14000B	*
	Q9100B	
	Q6000B	*
	Q2100B	
Q20000	Q20160/ELA88000	*
	Q20080/ELA85000	*
	Q20020/ELA83000	*
	Q20010/ELA81000	*

* These arrays are not yet released

This information is carried in the chip macro that is placed on the schematic drawings. Placement of the chip macro is page-independent to the software. AMCC requires that the chip macro be placed on page one.

TECHNOLOGY

The TECHNOLOGY of a design is also part of the chip macro. The technology of a circuit is defined as the I/O mode and there are four modes recognized for Bipolar and BiCMOS arrays at this time:

Value:	Description
T	for 100% TTL circuits; uses TTL I/O interface macros
E	for 100% ECL circuits; uses ECL I/O interface macros uses standard-reference ECL 10K or 100K macros regardless of the power supply (which may be either -5.2V (ECL 10K INPUT), -4.5V (ECL 100K INPUT) or +5V (EITHER ECL.10K OR ECL 100K INPUT)). For the Q20000 Series, applies to dual supply ECL (DECL).
M	for mixed TTL and ECL interface circuits using two power supplies, either +5V and -5.2V (ECL 10K) or +5V and -4.5V (ECL 100K). Uses the STD REF ECL macros and the TTLMIX macros.
P	for mixed TTL and ECL interface circuits using one power supply (usually +5V). Uses the +5V REF ECL macros if defined for the array. Uses TTL macros.

The technology parameter of macros is the same with the addition of:

C	for CMOS interface - may be placed on BiCMOS arrays

PRODUCT_NAME

The AMCC-assigned array code name assigned by AMCC must be on all media, files and schematics for design submission. To attach this name to the chip macro, define the PRODUCT_NAME parameter for the chip macro using the code name string as its value. This parameter is optional; the ERC software will execute without it. However, AMCC requires that it be used for schematics upon design submission.

DEVICE_NUMBER

The device number, the number assigned by AMCC when a circuit is booked, must appear on the schematics and associated documentation. To define the number, attach the DEVICE_NUMBER parameter to the chip macro and define the identifying string as its value. This parameter is optional; the ERC sotware will execute without it. However, AMCC requires that it be used for schematics upon design submission.

PRODUCT_GRADE

The worst-case-mode is supplied by attaching a PRODUCT _GRADE parameter to the chip macro. The parameter is attached to the chip macro symbol and MIL or COM defined as its value. This paameter is optional; the ERC software will assume MIL as its value. However, AMCC requires that it be used for schematics and files upon design submission.

POWER_SUPPLY - 100% ECL, BIPOLAR, BiCMOS
- ECL/TTLMIX BIPOLAR, BiCMOS

The power supply used in a 100% ECL design could be -5.2V, -4.5V or +5V. The chip macros carry a generic -5.2V (ECL 10K) or -4.5V (ECL 100K) label, which documents the default value.

To define the actual power supply used in a 100% ECL circuit, attach the POWER_SUPPLY parameter to the chip macro and define STD4 (for -4.5V), STD5 (for -5.2V) or 5VREF (+5V) as its value. The POWER_SUPPLY parameter may not have 5VREF as an allowed value for the Q20000 Series.

This parameter is optional but AMCC recommends its use where the power supplies are non-standard.

The power supply used in a dual-power supply ECL/TTL mixed mode design may also be altered from the default values.

- For an ECL 10K design (MIX10K is in the chip macro name), the default is -5.2V and may be set to -4.5V by assigning a value of STD4 to POWER_SUPPLY.

- For an ECL 100K design (MIX100K is in the chip macro name), the default is -4.5V and may be set to -5.2V by assigning a value of STD5 to POWER_SUPPLY.

ALLOWED POWER_SUPPLY PARAMETER VALUES

CHIP MACRO	5VREF* +5V	STD5 -5.2V	STD4 -4.5V
QxxxxECL10K	x		x
QxxxxMIX10K			x
QxxxxECL100K	x	x	
QxxxxMIX100K		x	

No other chip macros carry the power_supply parameter.

* 5VREF is not allowed for the Q20000 Series.

DELAY_PATH
MIND MAXD

The net DELAY_PATH parameter and MIND and MAXD parameters are available.

The DELAY_PATH parameter is assigned to each net in a path by attaching it to each wire-net. The value supplied is a string which is the user-defined path name. This should not be confused with the user-defined net signal name. This parameter and its use are optional.

The MIND and MAXD parameters need to be attached to only one net in the path defined by the DELAY_PATH parameter above. The values given for each are the minimum (MIND) and maximum (MAXD) metal delay allowed for the path given in picoseconds. A path may be defined as one net in size. These parameters are optional; neither, either or both may be used.

FAN-OUT DERATING - FOD

The FAN-OUT_DERATING net parameter, FOD, must be assigned to all nets in a clock path and may be used with any path the designer wishes to derate.

The assigned parameter value can be a two-digit number, 1 through 99, and represents a percentage for the the ERC software to use to derate the fan-out load limit of the macro pin driving the net. The parameter is usually assigned values for 20% and 40% fan-out load derating for clock path or other distortion-sensitive nets. The resulting fan-out load is computed using truncation.

Refer to Volume I, Section 4 of the appropriate Design Manual for the operating speed-clock derating required for any given array.

The ERC software will check to see that loads on a derated line do not exceed the derated fan-out load limit.

If no FOD parameter is assigned to a net, the ERC fan-out check is made using the specified macro fan-out load limit for the pin driving the net.

STATIC LOAD - FAN-OUT LOAD CHANGE (Bipolar Only)

When an unused internal (non-primary) macro input pin has a hook-up restriction which prevents it from being allowed to float (cannot be tied to global ground), then it must be forced to a logical one or a logical zero.

- For the Q5000 and Q3500 array series, special static load drivers (GT87) are available for this purpose. They have a fan-out load limit specifed at 32 loads. Refer to Vol I, Section 6 for documentation on these macros.

- For the Q700 Series arrays, use a standard-option OR or NOR gate for this purpose and document the ERC fan-out load error message received.

SWGROUP

SIMULTANEOUSLY_SWITCHING_OUTPUT: The SWGROUP macro parameter allows the user to define groups consisting of simultaneously switching output macros and the added power and ground macros that are assigned to the individual groups. This allows a report to be made of the switching groups on the array and a check to be made for extra power and ground requirements.

AMCC requires the use of this parameter to allow checking for added power and ground, and for proper completion of the I/O list for design submission.

Values assigned to the macro parameter are names and follow AMCC naming conventions.

BIPOLAR; BiCMOS PARAMETERS

ECL_LEVEL

The input ECL_LEVEL (ECL 10K or ECL 100K) of a design is defined by the chip macro selection. The chip macro will also select the default poweer supplies.

- For the Q3500 Series, the chip macro also defines the allowed output ECL_TYPE.

- The Q14000 and Q5000 Series arrays may mix ECL 10K and ECL 100K output macros on any circuit.

- The Q700 Series arrays do not support ECL 100K.

COMPONENT FAN-OUT CHECK

• FAN-OUT - (ALL) Verifies that specified macro fan-out load limits are not exceeded. Through the use of the "FOD" fan-out derating parameter, this check will verify that derated fan-out load limts are not exceeded. This check will generate an error message for each fan-out error encountered.

INTRODUCTION

The purpose of the fan-out ERC is to verify that a macro is not driving a load larger than the fan-out load limit of that macro. For a macro with a derated fan-out load limit, it will verify that the macro is not driving a load larger than the derated load limit.

FAN-OUT LOAD LIMITS

Macro output pin fan-out load limits are documented in Volume I, Section 6 of the appropriate Bipolar or BiCMOS design manual. The ERC will generate an error message if the specified fan-out load limit is exceeded and no fan-out derating parameter has been used.

WHEN FAN-OUT LOAD LIMITS SHOULD BE DERATED

There are specific conditions under which the specified fan-out load limit should be reduced:

- Any macro driving a differentially-driven 100% TTL unbuffered output macro should have its fan-out load limit reduced by 20%.
- Any macro in a critical path or a distortion-sensitive path should have its fan-out load limit reduced by 20% or 40% depending on the intended speed of operation. Refer to Volume I, Section 4 of the appropriate Design Manual for the rules applicable to the given array.

HOW TO SPECIFY FAN-OUT DERATING - FOD

The designer indicates that a derated fan-out load limit is to be used by attaching the net parameter FOD and defining as its value a 2-digit number that is the per centage that the specified fan-out limit is to derated by. If no FOD parameter is attached to a net, then the specified macro fan-out load limit is used in the ERC check.

Macro load limit before derating:	FOD Parameter value:	New load limit used in fan-out check
9	20	7
15	20	12
9	40	5
15	40	9

The fan-out check will truncate to the lowest whole number.

FAN-IN VALUES DIFFERENT FROM ONE

The fan-out load check correctly handles the case where a macro input pin represents more than one load to the driving macro. The macro documentation should always be referenced whenever there is a question on an input pin's fan-in value.

BIDIRECTIONAL PIN FAN-OUT LOAD CHECK

In the case of a bidirectional pin, the output is checked for fan-out violations (not counting its own fan-in), and the fan-in is counted when being driven by another output.

FAN-OUT LOADING TABLE

A fan-out table is written which contains the component instance name, the macro name, the signal, the load limit against which the check is made (the specified fan-out load limit if not derated or the new, derated limit), the actual load, the % derating used (if any), and the page number.

There is no indication made in the table as to error. Error messages are listed in a separate section above the table.

ERROR REPORTS

A description of error messages follows. Where a signal is to be identified, there is a universal identification printout which follows the specific error message.

ERROR500: FAN-OUT LOAD LIMIT EXCEEDED ON:

Informs the user that the allowable fan-out load limit has been exceeded for the output pin driving the net. If the net has a derating parameter attached, the check is made against the derated load limit.

ERROR501: FAN-OUT LOAD LIMIT IS MISSING FOR THIS MACRO

Informs the user that there is a missing parameter for the pin driving the net. Contact AMCC when this error occurs.

ERROR502: FAN-IN LOAD IS MISSING FOR THIS MACRO

Informs the user that there is a missing parameter for the pin driven by the net. Contact AMCC when this error occurs.

ERROR503: NO OUTPUT PIN ON THIS NET

The net has destination pin or pins but no macro output pin drives it. Not generated for primary input nets.

INFORMATION ONLY:

Number of errors found = n

If errors are found, this statement will inform the designer. There is a limit of 25 on the number of messages printed.

No errors have been found

The circuit has no errors detected by this part of the MacroMatrix software.

```
*************************************************************
*          FAN-OUT CHECK ERC                                *
*          REVISION 1.1                                     *
*************************************************************


   Path Name /USER/CLASS/ERRORS
   Product Name PRODUCT_NAME
   Circuit family Q3500
   Circuit technology E
   Date 9 JUN 1986
   Time 13:3
   Product Grade PRODUCT_GRADE


ERROR503: NO OUTPUT PIN ON THIS NET
          Driving Component=1C11 Macro=FF19
          Signal=XSIG15
          Page= 2
ERROR500: FAN_OUT LOAD LIMIT EXCEEDED ON  :
          SIGNAL= 3S5
          PIN=Y    COMPONENT=ECLANY   MACRO=IE85     LIMIT=8     PAGE=4
          PIN=Y    COMPONENT=111111   MACRO=IE85     LIMIT=8     PAGE=4
          PIN=A    COMPONENT=ECL100   MACRO=OK73   LOADING=1     PAGE=4
          PIN=A    COMPONENT=ECL10    MACRO=OE73   LOADING=1     PAGE=4
ERROR503: NO OUTPUT PIN ON THIS NET
          Driving Component=4C4 Macro=IEGND
          Signal=XSIG5
          Page= 5
   Number of errors found = 4
```

FAN-OUT LOADING TABLE FORMAT:

COMPONENT	MACRO NAME	SIGNAL	LIMIT	LOAD	% DERATING	PAGE
0C10	IT01	0S13	9	1		1
W001	WIREOR2	0S14	9	0		1
0C11	GT01	0S17	9	1		1
0C11	GT01	0S18	9	1		1
0C14	IT01	0S20	5	1	40	1
0C5	WIREOR3	0S9	9	1		1
AMCC01	IT01	12W	9	1		1
0C7	IT01	12_34	9	7		1
V0002	VT00	1S10	999	1		2
V0003	IE85	1S11	8	2		2
2C3	IT01H	2S7	7	1	20	3
2C1	GT03	2S8	7	3	20	3
CHIP00	Q3500STT	4S1	999	0		5
2C2	GT10	FTOUT1	9	0		3
S0016	IT12H	SEL3	9	1		8
0C8	IT01	Z0001	9	1		1

% DERATING = amount limit to be reduced by, typially
20 for 20% or 40 for 40% derating

MACRO PIN HOOK-UP CHECK

• PIN HOOKUP - (ALL) Checks to make sure that pins which must be connected are "hooked-up" to a valid signal. Checks that bipolar macros are not clipped and BiCMOS internal macros are not tied to ground.

• UNUSED PINS - (ALL) Checks a design for "dangling" pins (not connected to a signal, not grounded, not clipped and not terminated).

INTRODUCTION

UNUSED PINS

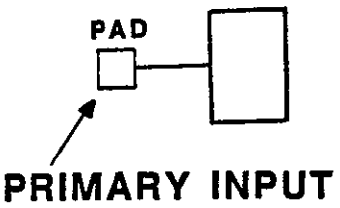
Unused non-primary (macro) input pins:

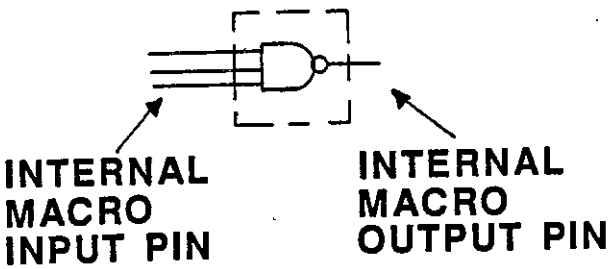
• BiCMOS arrays, internal (core) macros: Unused macro input pins must be clipped to VDD or VSS, never tied to global ground and never terminated. Refer to Section 7, Volume II for instructions on clipping. Clipped pins are not counted in the internal pin count check.

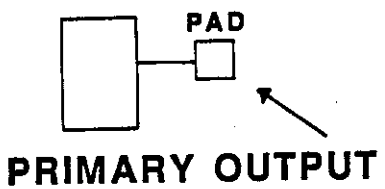
• Bipolar arrays, any macro; BiCMOS arrays, interface (I/O) macros: Unless restricted by a hook-up requirement, unused macro input pins must be tied to global ground on the schematic, never clipped and never terminated. They float in the physical circuit. Refer to Section 7, Volume II for instructions on connecting to a global ground. They are not counted in the internal pin count check.

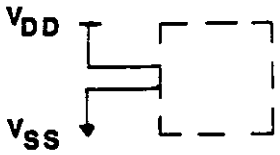
Unused non-primary (macro) output pins:

Unused macro output pins must be terminated (tied to ZTERM). Terminated output pins are not counted in the internal pin count check. Terminated outputs may have a reduced current drain which will be considered during layout. Refer to powered-down outputs in Volume I, Section 5. Arrays which feature powered-down outputs are the Q5000 and Q3500 Series.

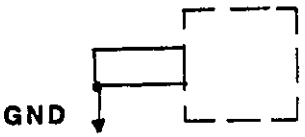

PAD
PRIMARY INPUT


INTERNAL
MACRO
INPUT PIN
INTERNAL
MACRO
OUTPUT PIN

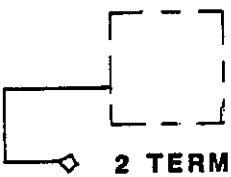

PAD
PRIMARY OUTPUT



INPUT PINS "CLIPPED"

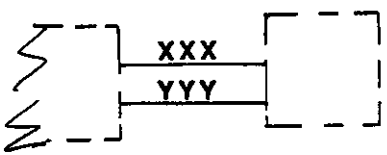


INPUT PINS GROUNDED



ALWAYS ILLEGAL!

INPUT PINS TERMINATED



INPUT PINS DRIVEN

NOTE: SYMBOLS VARY AMONG EWS LIBRARIES

HOOK-UP REQUIREMENTS

Bipolar arrays: Interface macros on BiCMOS arrays: For electrical reasons, certain macro pins may not be tied to global ground since this is a float.

- There are pins which must be connected to a signal (e.g., the macro documentation will contain a note such as: D MUST BE DRIVEN BY A MACRO).

- There are groups of macro input pins that require that one of their number be connected, offering the designer a choice (e.g., the macro documentation will contain a note such as: EITHER A, B, OR C MUST BE DRIVEN BY A MACRO).

- There are also groups of pins on macros where each pin must be connected to a valid signal (e.g., the macro documentation will contain a note such as: S1, EN EACH MUST BE DRIVEN BY A MACRO).

For those arrays which provide one, use a static driver (GT87) to drive these pins high or low as required. For those arrays with no static driver, use a simple OR/NOR gate at lowest available power and document the ERC fan-out error message.

Care must still be taken not to ground the inputs to AND/NAND gates. Hook-up code violations will not detect all mis-uses of macro control lines - only those that would case electrical difficulty. The designer must ensure that the proper macro is selected and that the macro is properly used to implement the desired logic.

Care must also be taken in connecting the PAD of input and output macros. No PAD from an output macro may be taken back inside the array since the signal is at external interface levels. No internal signal may drive the PAD of an input macro. This applies to bidirectional macros as well. These errors may not detected by the ERC software.

ERROR REPORTS

\ description of errors follows. All error messages give the component name and pin name information in sufficient detail to allow location within the schematic set.

ERROR425: UNUSED INPUT PIN

Informs the user that a unused macro input pin was found. Either an internal macro input pin or a primary input pin was not connected to a named wire, terminated (connected to ZTERM), connected to ground, or clipped. The pin is not connected to anything and the assumption is made that it should be connected.

ERROR426: UNUSED OUTPUT PIN

Informs the user that a unused macro output pin was found. Either an internal macro output pin, a primary output pin, or a primary bidirectional output pin was not connected to a named wire, terminated, tied to ground or clipped. The pin is not connected to anything and the assumption is made that it should be connected.

ERROR427: INPUT PIN ILLEGALLY GROUNDED, TERMINATED
OR UNCONNECTED
One of the following pins must be driven by
a macro:

Hook-up code violation. Informs the user that a pin was grounded (tied to global GROUND) and it should not have been. This error applies to a Bipolar array macro: the pin should have been driven by another macro or one of a set of pins to which this pin belongs should have been driven. The error list will be the list of all pins on that component which have the same hook-up code.

ERROR433: HOOKUP PARAMETER NOT FOUND FOR THIS PIN

One of the pins is missing parameter information. Contact AMCC when this error occurs.

ERROR434: NET HAS ONLY ONE PIN

A net exists which has one only one pin (incomplete net). Single pin nets where a terminator drives an input, or ground, VDD or VSS is connected to an output, are detected and reported. Single pin nets where an input pin is tied to ground, VDD or VSS, or an output pin is tied to a terminator, are not reported (these are legal).

ERROR437: OUTPUT PIN ILLEGALLY CLIPPED OR GROUNDED

Informs the user that a macro output pin has been tied to VSS or VDD (clipped). No macro output pin may be clipped.

Informs the user that a macro output pin has been illegally tied to global GROUND. No macro output pin may be grounded.

ERROR438: INPUT PIN ILLEGALLY CLIPPED, GROUNDED, TERMINATED.

Informs that user that an internal macro input pin is tied to the ZTERM net (terminated). No macro input pin may be terminated.

Informs the user that an internal macro input pin was tied to global GROUND for a BiCMOS array. The pins on these macros cannot be grounded, they must either be used or clipped.

Informs the user that a bipolar array internal macro input pin has been illegally tied to VSS or VDD. Bipolar internal macro input pins cannot be clipped.

INFORMATION ONLY:

Number of errors found = n

If errors are found, this statement will inform the designer. There is a limit of 25 on the number of messages printed.

No errors have been found

The circuit has no errors detected by this part of the MacroMatrix software.

```
************************************************************
*          PIN HOOKUP & UNUSED PINS CHECK ERC              *
*          REVISION 1.0                                    *
************************************************************


   Path Name /USER/CLASS/ERRORS
   Product Name PRODUCT_NAME
   Circuit family Q3500
   Circuit technology E
   Date 9 JUN 1986
   Time 13:3
   Product Grade PRODUCT_GRADE


ERROR434: NET HAS ONLY ONE PIN
          Component=W001 Macro=WIREOR2 Pin=Z
          Signal=XSIG30
          Page= 1
ERROR438: INPUT PIN ILLEGALLY CLIPPED, GROUNDED, OR TERMINATED
          Component=0C10 Macro=IT01 Pin=A
          Page= 1
ERROR437: OUTPUT PIN ILLEGALLY CLIPPED OR GROUNDED
          Component=1C11 Macro=FF19 Pin=QN
          Signal=GND
          Page= 1
ERROR425: UNUSED INPUT PIN
          Component=0C10 Macro=IT01 Pin=A
          Page= 1
ERROR427: INPUT PIN IS ILLEGALLY GROUNDED
          Component=0C15 Macro=IT01
          Page= 1
          One of the following pins must be driven by a macro:
          A
ERROR LIMIT EXCEEDED.

   Number of errors found = 43
```

```
*************************************************************
*          PIN HOOKUP & UNUSED PINS CHECK ERC               *
*          VERSION  2.8Ø                                    *
*************************************************************

   Path Name /USER/CLASS/QUICK
   Product Name PRODUCT_NAME
   Circuit family Q5ØØØ
   Circuit technology M
   Date 18 OCT 1988
   Time 16:2Ø
   Product Grade PRODUCT_GRADE


ERROR434: NET HAS ONLY ONE PIN
          Component=1ØC7 Macro=FF1C Pin=Q
          Signal=XSIG11
          Page= 11
                    .
                    .
                    .


ERROR434: NET HAS ONLY ONE PIN
          Component=11C8 Macro=UE5Ø Pin=Y
          Signal=XSIG33
          Page= 12
ERROR434: NET HAS ONLY ONE PIN
          Component=11C11 Macro=OT3Ø Pin=PO
          Signal=XSIG13
          Page= 12
ERROR434: NET HAS ONLY ONE PIN
          Component=12C1Ø Macro=IE89D Pin=Y2
          Signal=XSIG23
          Page= 13
ERROR434: NET HAS ONLY ONE PIN
          Component=12C1 Macro=OT63 Pin=A
          Signal=XSIG33
          Page= 13
ERROR434: NET HAS ONLY ONE PIN
          Component=12C1 Macro=OT63 Pin=B
          Signal=XSIG34
          Page= 13
ERROR434: NET HAS ONLY ONE PIN
          Component=12C2 Macro=OT57 Pin=A
          Signal=XSIG35
          Page= 13
ERROR434: NET HAS ONLY ONE PIN
          Component=12C3 Macro=OT63 Pin=A
          Signal=XSIG37
          Page= 13
ERROR434: NET HAS ONLY ONE PIN
          Component=12C3 Macro=OT63 Pin=B
          Signal=XSIG38
          Page= 13
ERROR434: NET HAS ONLY ONE PIN
          Component=12C5 Macro=IE9Ø Pin=Y
          Signal=XSIG41
          Page= 13
ERROR434: NET HAS ONLY ONE PIN
          Component=12C5 Macro=IE9Ø Pin=YN
          Signal=XSIG42
          Page= 13
ERROR434: NET HAS ONLY ONE PIN
          Component=17C6 Macro=IE25 Pin=Y
          Signal=XSIG14
          Page= 18
ERROR434: NET HAS ONLY ONE PIN
          Component=17C6 Macro=IE25 Pin=YN
          Signal=XSIG15
          Page= 18
ERROR434: NET HAS ONLY ONE PIN
          Component=17CØ Macro=IE99V Pin=Y
          Signal=XSIG18
          Page= 18
ERROR LIMIT EXCEEDED.

   Number of errors found = 2156
```

INTERNAL PIN COUNT

• INTERNAL PIN COUNT - (ALL) Counts all routable internal macro pins on a design and returns the total per page and overall total from the design. Counts unconnected pins under the assumption that they should have been connected somewhere.

INTRODUCTION

The internal pin count ERC counts all connected internal pins on a design that must be routed by the layout software.

Pins which ARE counted are:

- pins that are connected to other internal pins
- pins that are not connected to anything
- internal pin count parameter supplied by the MSI macros (all arrays)
- Q700 threshold generator pins

Pins which are NOT counted are as follows:

- pins that are connected to ground (bipolar arrays, BiCMOS I/O; input pins connected to GLOBAL ground)
- pins that are "clipped" (BiCMOS array core macro input pins connected to V_{DD} and V_{SS})
- terminated outputs
- primary (externally sourced) inputs, including PWR and ground macro inputs (i.e., ITPWR, ITGND, IEVCC)
- primary (external destination) outputs.

The internal pin count report file informs the user of the internal pin count per page and the overall internal pin count for the design.

This ERC provides an error message when the internal pin count exceeds array limits for an acceptable array (RISKY, VERY RISKY, UNACCEPTABLE).

ERRORS AND WARNINGS

ERROR350: TOTAL INTERNAL PIN COUNT EXCEEDS ROUTABLE LIMITS
This circuit cannot proceed to layout.

The number of pins that must be routed is over the fatal limit for the array. The array cannot be routed. The circuit should be re-evaluated to see what internal pin reductions could be made before proceeding. Pin reductions can be achieved by changing simple macros to more complex, cell efficient macros and by performing logical minimization if it has not already been done. Optional functions (the so-called engineering wish-list) should be reviewed for possible deletion.

ERROR351: TOTAL INTERNAL PIN COUNT EXCEEDS THE LIMIT FOR THIS ARRAY
This circuit is considered to be extremely risky
This circuit will probably fail in layout

The number of internal pins that must be routed is over the specified limit for the array but less than the fatal limit. There is a remote possibility that the array could successfully route but it is more likely that it will fail.

WARNING352: TOTAL INTERNAL PIN COUNT EXCEEDS LIMIT FOR THIS ARRAY
This circuit is considered risky and may fail in layout.

The number of internal pins that must be routed is over the specified limit for the array but less than the probably-fail limit. The array may still successfully route but there is a possibility that it may not.

ERROR353: MAXIMUM NUMBER OF INTERNAL PINS NOT FOUND

This is a missing parameter for the chip macro. Consult AMCC if this error occurs.

INFORMATION ONLY:

INTERNAL PIN COUNT IS WITHIN BOUNDS
- THIS ARRAY IS ROUTABLE

The array is acceptable for routing. No problems due to the number of internal pin connections is expected.

No errors have been found

```
**********************************************************
*          INTERNAL PIN COUNT ERC                        *
*          VERSION  2.8Ø                                 *
**********************************************************

   Path Name /USER/CLASS/Q532REG
   Product Name Q5REG32
   Circuit family Q5ØØØ
   Circuit technology M
   Date  7 OCT 1988
   Time 1Ø:39
   Product Grade MIL


                CIRCUIT    AVAILABLE
-----------------------------------------
SUM_INT_PINS:      4Ø6         247Ø
-----------------------------------------

Internal pin count is within bounds.
This array is routable.


   No errors found.
```

```
*************************************************************
*          INTERNAL PIN COUNT ERC                           *
*          VERSION  2.8Ø                                    *
*************************************************************

   Path Name /USER/CLASS/QUICK
   Product Name PRODUCT_NAME
   Circuit family Q5ØØØ
   Circuit technology M
   Date 18 OCT 1988
   Time 16:2Ø
   Product Grade PRODUCT_GRADE


                CIRCUIT    AVAILABLE
-----------------------------------------
SUM_INT_PINS:      3ØØ3        9Ø6
-----------------------------------------

ERROR35Ø: TOTAL INTERNAL PIN COUNT EXCEEDS ROUTABLE LIMITS
          This circuit cannot proceed to layout.


   Number of errors found = 1
```

MACRO OCCURRENCE and POWER DISSIPATION TABLE - BIPOLAR; BiCMOS

- MACRO OCCURRENCE - Provides the designer with a macro usage tally, a summation of the maximum worst-case internal current, detection if the current used exceeds the maximum internal current specification for the array, and provides a filled-in report on the total power dissipated by the entire circuit for all bipolar arrays.

- Provides a macro list and power computation for the interface macros (BiCMOS) or all macros (Q20000) & provides a macro list and workspace for internal power computation.

INTRODUCTION

BiCMOS (Interface)/BIPOLAR (total) POWER COMPUTATION

The macro occurrence and power dissipation table displays macro occurrence information (macro name, number of occurrences), internal current dissipation (I_{CC} and I_{EE}) and total worst-case power dissipation for the circuit.

- The SPECS section informs the user of the typical current dissipation for each individual occurrence of a macro (I_{CC} and/or I_{EE}) and the TOTALS section gives the total current dissipation as summed for all occurrences of that macro. The current values for a single occurrence of a macro are the typical values specified in the appropriate macro documentation.

- All current is considered to be I_{CC} in a 100% TTL circuit or in any circuit designated as +5V REF ECL or +5V REF ECL/TTL mixed. I_{CC} current is multiplied by the absolute value of the V_{CC} supply.

- All current is considered to be I_{EE} in a 100% ECL circuit designated as standard reference ECL. I_{EE} current is multiplied by the absolute value of the V_{EE} supply.

- In a dual power supply circuit, the individual I_{CC} and I_{EE} currents, if both are specified for a macro, are maintained.

• For 3-state and bidirectional macros, the maximum typical current is used, regardless of the macro state. No state-dependent adjustment is made.

• TOTAL TYPICAL MACRO CURRENT. This section totals up all I_{CC} and I_{EE} currents and places the totals in the appropriate columns.

sum of I_{EE}
sum of I_{CC}MACROS
MACROS

• TOTAL TYPICAL POWERED-DOWN CURRENT. This sections totals all powered down macro outputs currents and places the totals in the appropriate columns. Both interface macros and internal macros may have output pins that are wire-ORable. These pins are powered-down when terminated (connected to the ZTERM net). For the value of the current saved by terminating a specific macro output refer to Volume I, Section 5 of the Design Manual for the specific array series.

sum of I_{EE}
sum of I_{CC}powered-down I_{OEF}
powered-down I_{OEF}

• TOTAL TYPICAL OVERHEAD CURRENT. This section adds in the typical overhead current drain to the design. The number here depends upon the chip family, and the technology. (For the Q700 and Q1500 Series arrays, it is also a function of the total number of TTL inputs.) The overhead current is specified in Volume I, Section 5 of the appropriate Design Manual.

I_{EE}
I_{CC}overhead
overhead

The ERCs will use the maximum typical overhead current values when run pre-layout. When CIRCUIT.PKG is in the calling directory (location varies by EWS), the programmable overhead current values will be used.

• TOTAL TYPICAL CURRENT. This section adds the overhead current with the total macro currents in the I_{CC} and I_{EE} columns, subtracts the powered down currents, if any, and writes the new totals. These are the TYPICAL I_{CC} and I_{EE} currents.

• WCCM - WORST-CASE CURRENT MULTIPLIER. This multiplier may be different for MILITARY and COMMERCIAL circuits depending on the array series. The worst-case current multiplier is specified in Volume I, Section 5 of the appropriate Design Manual. **NOTE: For arrays where this multiplier varies with internal cell utilization, the ERCs will compute the correct multiplier to be used.** Refer to Volume I, Section 5 for the worst-case current multiplier for the array series.

• TOTAL MAX CURRENT. This multiplies the overall total of I_{EE} and of I_{CC} (sum of all macros plus the overhead current) by WCCM and places the result of each operation in the respective column.

$$I_{EE_{WC}} = (\text{sum of } I_{EE_{MACROS}} + I_{EE_{OVERHEAD}} - I_{EE_{powered\text{-}down}}) * WCCM$$

$$I_{CC_{WC}} = (\text{sum of } I_{CC_{MACROS}} + I_{CC_{OVERHEAD}} - I_{CC_{powered\text{-}down}}) * WCCM$$

• WORST CASE POWER DISSIPATION. The worst-case voltage is multiplied times the worst-case current to obtain the worst-case power products. The worst-case voltage used is based on the circuit parameters. The following is the table for default power supplies. The worst-case voltage depends on the value assigned to the POWER_SUPPLY parameter, if it was defined. (This parameter is optional.)

		WORST_CASE_MODE:					
			MIL			COM	
TECHNOLOGY:	ECL TYPE:		V_{CC}	V_{EE}		V_{CC}	V_{EE}
T	none		5.5	0		5.25	0
E	ECL 10K		0	5.7		0	5.46
E	ECL 100K		0	4.8		0	4.7
M	ECL 10K		5.5	5.7		5.25	5.46
M	ECL 100K		5.5	4.8		5.25	4.7
P	ECL 10K		5.5	0		5.25	0
P	ECL 100K		5.5	0		5.25	0

$$P_{EE_{WC}} = V_{EE_{WC}} * I_{EE_{WC}}$$
$$P_{CC_{WC}} = V_{CC_{WC}} * I_{CC_{WC}}$$

• ECL OUTPUT POWER DISSIPATION. For ECL outputs only, the termination current value is multiplied by 1.3V (average voltage level) and the number of ECL outputs, assuming a 50% duty cycle. The power computation must be adjusted by the designer (manually) if a non-standard termination is used or if the duty cycle is significantly different.

For ECL 10K/100K:

TERMINATION	CURRENT
25 ohm	28.0mA
50 ohm	14.0mA
100 ohm	7.0mA
200 ohm	3.5mA

• TOTAL POWER DISSIPATION. The worst-case power dissipation products are added along with any ECL output power dissipation to form the total worst-case power. Use this total when evaluating a package and proposed environmental conditions for the circuit. For Bipolar arrays, use this number, or the adjusted number where manual computations are required, to compute the junction temperature of the array for the given, specified, operating environment and conditions (e.g., heat sink, if any; air flow).

• ADJUSTMENTS

• Different ECL termination. In this case, the current is computed as $0.7 * V_T / R$. For a termination voltage of -2V, this reduces to 1.3V/R. Compute the current and use in the ECL static power dissipation equation. Adjust the power supply shown in the standard equation if it is different (worst-case values).

• State-dependent power computations. For 2-state outputs, calculate I_{CC} and I_{EE} as an even average (50% high - 50% low) between the two states. For 3-state outputs, assume 500% disabled high-impedance (Z state), 25% enabled-high output mode and 25% enabled-low output mode. Adjust the values for the macros affected and recompute the total power dissipation.

• Programmable overhead current (BiCMOS Q14000B, Q6000B). If placement has been performed, then an adjustment can be made to the overhead current based on the ECL inputs and outputs nad their locations within the quadrants. Values will be computed by the pre-layout software and made available in CIRCUIT.PKG. A manual computation can be performed once placement is known but this is not recommended.

MAXIMUM INTERNAL CURRENT CHECK - BIPOLAR ARRAYS ONLY

The internal logic macro current sums are computed as a subtotal but not listed until the end of the table. Internal logic macros are those residing on L or B cells.

The internal logic macro subtotals for I_{CC} and I_{EE} are added, adjusted for the powered-down internal macro outputs, multiplied by the worst-case current multiplier, WCCM, and compared to the specification for the array. Refer to Volume I, Section 5 of the appropriate Design Manual.

Both the computed worst-case internal current for the circuit and the maximum internal current specified for the array are printed out at the end of the power dissipation computation.

An error message is generated if the maximum internal current specification is exceeded. A warning message is generated if the current is 80% of the specified limit or higher since further checking during layout will be more restrictive. (There are row and half-row maximum current specifications that must be honored during layout.)

Power can be reduced by changing macro options or by selecting lower current drain macros where high fan-out drive is not required. Power can also be reduced by performing logic minimization.

If an array has no internal current limit, the specified limit is set at 9999mA, an invalid number. The Q700 and the BiCMOS arrays have no internal current limits.

BiCMOS/Bipolar MACRO OCCURRENCE TABLE
- Bipolar (Q20000 Series); BiCMOS (INTERNAL MACROS)

• MACRO OCCURRENCE - (BiCMOS internal macros only; Bipolar - all macros (Q20000 Series) Gives the user a macro usage table for use in power computation.

A table displaying macro occurrence information will be generated by the ERC program. There is no restriction with respect to the occurrence frequency of a given macro. The power dissipation of macros are not treated in this table nor is the current recorded.

The following table is produced as a work-sheet for power computation. The table of basic cells is used for bipolar and BiCMOS. The Table of I/O and I cells is used for bipolar.

INTERNAL MACROS:

• For the BiCMOS Q14000 Series, the internal macro report and worksheet form is:

BiCMOS/Bipolar POWER COMPUTATION WORKSHEET

TABLE OF BASIC CELLS

Macro Name	# of Occurrences	Switching Frequency
...	...	<customer supplies>
...	...	<customer supplies>

The designer fills in the switching frequency for each macro name (these are the AMCC macro names, not instance names). If macros with the same name switch at different frequencies, then add additional pages and indicate the correct number of macros in each entry made for the same macro name.

FOR THE Q20000: All macros (interface and internal) are listed.

FOR THE Q14000: Only internal macros are listed.

BiCMOS (Internal)/Q20000 (total) POWER COMPUTATION

Internal Power Estimate Computation

Use the appropriate equation to compute the contribution to power dissipation attributable to the internal macros. Refer to Volume I, Section 5.

For BiCMOS, add the result of this step to the power dissipation computed by the MacroMatrix ERC software for the interface macros to find the total power dissipation for the BiCMOS array. Use this new total when computing junction temperature.

For Q20000 Bipolar, add the result of this step to the power dissipation computed by the MacroMatrix software for all macros in the array. All Q20000 macros have an AC and DC power dissipation.

ERRORS AND WARNINGS

A description of the errors and warnings follows:

ERROR375: INTERNAL WORST-CASE CURRENT EXCEEDS
THAT SPECIFIED FOR THIS ARRAY

The internal worst-case current dissipation, computed by forming the sum of the current dissipated by any internal logic macros (macros placed on L or B cells) and multipling by the worst-case current multiplier, 1.4, exceeds the maximum internal current specification for the array. Refer to the series macro documentation.

WARNING376: INTERNAL WORST-CASE CURRENT IS HIGH
- CIRCUIT MAY FAIL IN LAYOUT

The internal worst-case current dissipation is within 80% of the maximum internal current specification for the array. Since there are row and half row maximum current specifications which must be honored during layout, the circuit may fail in layout. Efforts should be made to reduce power consumption if this warning is received. This check applies to Bipolar arrays.

INFORMATION:

WORST-CASE INTERNAL CURRENT IS: (circuit)
MAXIMUM INTERNAL CURRENT SPECIFICATION IS: (spec)

These messages appear at the end of the macro occurrence table.

No errors have been found

No errors were encountered by this portion of the MacroMatrix ERC software.

```
**********************************************************
*          MACRO OCCURRENCE AND POWER DISSIPATION        *
*          VERSION  3.ØØ                                 *
**********************************************************
```

BAD

Path Name /USER/CLASS/QUICK
Product Name PRODUCT_NAME
Circuit family Q5ØØØ
Circuit technology M
Date 18 OCT 1988
Time 16:2Ø
Product Grade PRODUCT_GRADE

WORST-CASE INTERNAL CURRENT: 1310.46 mA
MAXIMUM INTERNAL CURRENT SPECIFICATION IS: 405.ØØ mA

ERROR375: INTERNAL WORST_CASE CURRENT EXCEEDS
THAT SPECIFIED FOR THIS ARRAY
Invalid product grade, MIL will be used.

Number of errors found = 1

MACRO NAME	# USED	SPECS ICC mA	SPECS IEE mA	TOTALS ICC mA	TOTALS IEE mA
ADØ5	1	Ø.ØØ	1.62	Ø.ØØ	1.62
ADØ5H	1	Ø.ØØ	2.52	Ø.ØØ	2.52
ADØ5L	1	Ø.ØØ	1.26	Ø.ØØ	1.26
ADDØØ	6	Ø.ØØ	12.51	Ø.ØØ	75.Ø6
ADDØØH	1	Ø.ØØ	18.35	Ø.ØØ	18.36
ADDØØL	1	Ø.ØØ	1Ø.35	Ø.ØØ	1Ø.35
ADDØ2	6	Ø.ØØ	12.97	Ø.ØØ	77.22
ADDØ2H	1	Ø.ØØ	18.72	Ø.ØØ	18.72
ADDØ2L	1	Ø.ØØ	1Ø.53	Ø.ØØ	1Ø.53
CMPØØ	1	Ø.ØØ	12.51	Ø.ØØ	12.51
CMPØØH	1	Ø.ØØ	16.34	Ø.ØØ	16.34
	1	Ø.ØØ	1Ø.71	Ø.ØØ	1Ø.71
		Ø.ØØ	5.5Ø	Ø.ØØ	11.ØØ
			2.5Ø	Ø.ØØ	5

	ICC mA	IEE mA
TOTAL TYPICAL MACRO CURRENT mA	95.74	1143.37
TOTAL TYPICAL POWERED DOWN CURRENT mA	Ø.ØØ	7.Ø2
TOTAL TYPICAL OVERHEAD CURRENT mA	14.ØØ	136.ØØ
TOTAL TYPICAL CURRENT mA	1Ø9.74	1272.35
TOTAL MAX CURRENT mA (TYP CURRENT TIMES 1.4Ø) =	153.64	1781.29
WORST CASE POWER DISSIPATION		
VCC (5.5)V X (153.636)mA/1ØØØ	Ø.84 WATTS	
VEE (5.72)V X (1781.29)mA/1ØØØ	1Ø.19 WATTS	
ECL OUTPUT POWER DISSIPATION		
(28.Ø)mA X 1.3V X (1)outputs/1ØØØ	Ø.Ø4 WATTS	
(14.Ø)mA X 1.3V X (25)outputs/1ØØØ	Ø.46 WATTS	
TOTAL POWER DISSIPATION	11.53 WATTS	

```
**********************************************************
*          MACRO OCCURRENCE AND POWER DISSIPATION        *
*          VERSION  2.9Ø                                 *
**********************************************************
```

GOOD

Path Name /USER/CLASS/Q532REG
Product Name Q5REG32
Circuit family Q5ØØØ
Circuit technology M
Date 7 OCT 1988
Time 1Ø:39
Product Grade MIL

WORST-CASE INTERNAL CURRENT: 139.45 mA
MAXIMUM INTERNAL CURRENT SPECIFICATION IS: 843.ØØ mA

No errors found.

MACRO NAME	# USED	SPECS ICC mA	SPECS IEE mA	TOTALS ICC mA	TOTALS IEE mA
FF13H	32	Ø.ØØ	2.75	Ø.ØØ	88.ØØ
GTØ1L	1	Ø.ØØ	1.Ø3	Ø.ØØ	1.Ø3
GT11	2	Ø.ØØ	1.15	Ø.ØØ	2.3Ø
GT14H	1	Ø.ØØ	1.62	Ø.ØØ	1.62
GT28H	2	Ø.ØØ	1.84	Ø.ØØ	3.68
GT55D	2	Ø.ØØ	3.96	Ø.ØØ	7.92
GT6ØL	5	Ø.ØØ	1.2Ø	Ø.ØØ	6.3Ø
GT99	2	Ø.ØØ	Ø.ØØ	Ø.ØØ	Ø.ØØ
IE85	1	Ø.ØØ	Ø.ØØ	Ø.ØØ	Ø.ØØ
IE9Ø	1	Ø.ØØ	1.35	Ø.ØØ	1.35
IE93	4Ø	Ø.ØØ	1.35	Ø.ØØ	54.ØØ
ITGND	1	Ø.ØØ	Ø.ØØ	Ø.ØØ	Ø.ØØ
ITPWR	4	Ø.ØØ	Ø.ØØ	Ø.ØØ	Ø.ØØ
OE81	1	Ø.ØØ	5.58	Ø.ØØ	5.58
OE87	4	Ø.ØØ	Ø.ØØ	Ø.ØØ	Ø.ØØ
OT59H	4	3.87	Ø.34	15.48	1.36
OT61H	32	4.14	Ø.34	132.48	1Ø.88
OT63H	32	4.86	Ø.34	155.52	1Ø.88

	ICC mA	IEE mA
TOTAL TYP MACRO CURRENT mA	3Ø3.48	194.9Ø
TOTAL TYPICAL POWERED DOWN CURRENT mA	Ø.ØØ	13.Ø5
TOTAL TYP OVERHEAD CURRENT mA	14.ØØ	174.ØØ
TOTAL TYP CURRENT mA	317.48	355.85
TOTAL MAX CURRENT mA (TYP CURRENT TIMES 1.4Ø) =	444.47	498.19
WORST CASE POWER DISSIPATION		
VCC (5.5)V X (444.472)mA/1ØØØ	2.44 WATTS	
VEE (5.72)V X (498.19)mA/1ØØØ	2.85 WATTS	
ECL OUTPUT POWER DISSIPATION		
(14.Ø)mA X 1.3V X (1)outputs/1ØØØ	Ø.Ø2 WATTS	
TOTAL POWER DISSIPATION	5.31 WATTS	

PIN CLASS (SIGNAL VALUE; PIN RESTRICTION) CHECK
BIPOLAR, BiCMOS
INCLUDES BIPOLAR WIRE-OR CHECK

PIN CLASS - WIRE-OR CHECK

• PIN CLASS - (ALL) Verifies that all pins for a given net are compatible. Signal class parameters are used to enforce pin restrictions. The driving macro pin signal class is checked against all driven pin signal classes. Supports the pin-hook-up check to complete interconnect checks for the circuit.

• WIRE-OR - (BIPOLAR) For a wire-OR, checks that ALL driving macro pin signal classes are identical. Wire-OR violations are detected by either the pin-class ERC, by the pin hook-up ERC or by the fan-out ERC.

INTRODUCTION

PIN CLASS

The pin-class ERC ensures that all pins in a particular net are of the same class or set of allowable classes (when a range is allowed) and that no wire-OR (WIREOR2, WIREOR3, WIREOR4) is improperly connected.

Each signal (net) is traversed to make sure that all pin class parameters of all macros in the net (driving macros and driven macros) are equivalent.

PIN RESTRICTIONS

An asterisk is used on a non-primary macro input pin to indicate:

- high fan-in (not equal to one)
- an input pin-restriction (macro must be driven by a specific macro or one of a set of macros).

An asterisk is used on a non-primary macro output pin to indicate:

- an output pin restriction. The macro output pin:
  - cannot be wire-ORed
  - must drive a specific macro or set of macros.

All of these restrictions are documented in Volume II, Section 6 of the appropriate Design Manual via comments listed with the individual macros.

PIN CLASS (SIGNAL VALUE; PIN RESTRICTION) CHECK
BIPOLAR, BiCMOS
INCLUDES BIPOLAR WIRE-OR CHECK

WIRE-ORS

There is no stated limit on the number of WIRE-ORs that may be in a circuit. The use of wire-ORs in a bipolar circuit must follow the following rules. There are no wire-ORs allowed in a CMOS or BiCMOS circuit. For parallel-drive in CMOS and BiCMOS, consult AMCC.

- No customer-generated parametric wire-ORs are allowed.
- No wire-OR may exceed four input drives.
  (Only WIREOR2, WIREOR3 or WIREOR4 may appear in a circuit.)
- No unbuffered input macros may drive a wire-OR.
- No pin-restricted macro output pin may drive a wire-OR.
  (E.g., an unbuffered input, certain latches, certain flip/flops, some MSI macros).
- No 3-state enable driver may drive a wire-OR.
- No high-fan-out driver (any macro with D in its name) may be used to drive a wire-OR.
- No macro driving a wire-OR may drive any other load.
  (The loads are placed on the wire-OR component output.)
- No wire-OR may drive another wire-OR. (No cascading.)
- No output from a wire-OR may be terminated.
- No input to a wire-OR macro may be grounded or clipped.
  (hook-up code check)
- Macro options (S, L, P, H) may be mixed in a wire-OR.
  (This is not encouraged since it can lead to designer-errors.)

Wire-OR violations are detected by either the pin-class ERC, by the pin hook-up ERC or by the fan-out ERC.

ERROR REPORTS

A description of errors follows. All error messages give the component name and pin name information in sufficient detail to allow location within the schematic set.

ERROR701: PIN-CLASS VIOLATION - ILLEGAL MACRO DRIVING WIRE-OR

Informs the user that a pin with a pin-class of 1000 or more has been connected to a wire-OR. A pin-class of 1000 or more may not be connected as a wire-OR input. Any macro with a pin-class greater than zero (0) cannot be wire-ORed. This includes any high fan-out driver, any WIREORn macro, any macro with a fan-out load limit of one and all 3-state enable-drivers. Drivers are not marked with an asterisk to show the restriction since the entire class of macros is involved.

Internal wire-ORs are not allowed to drive an external wire-OR. All such outputs are labeled with an asterisk and a notation made in the macro documentation. This is handled by the pin class ERC check.

ERROR702: PIN-CLASS VIOLATION - MISMATCH FOUND

Informs the user that the pin in error is not of the same pin-class as the rest of the pins connected to the net. Refer to Volume II, Section 6 of the appropriate Design Manual to determine pin restrictions for a macro.

ERROR703: PIN-CLASS PARAMETER IS MISSING FOR THIS PIN

Informs the user that the pin is missing a pin parameter. Contact AMCC if you receive this error.

ERROR704: WIRE-OR EXCEEDS FOUR (4) INPUTS

The WIREORn macro encountered is larger than WIREOR4 or a parametric wire-OR encountered is larger than an equivalent component WIREOR4.

ERROR705: ILLEGAL PARAMETRIC WIRE-OR HAS BEEN USED

Parametric wire-ORs cannot appear on schematics.

ERROR706: A MACRO DRIVING A WIRE-OR CAN NOT DRIVE
ANY OTHER LOADS

Any macro which is driving a wire-OR has a fan-out load limit of one (1). All loading must occur on the schematic as if driven by the wire-OR macro.

INFORMATION ONLY:

Number of errors found = n

If errors are found, this statement will inform the designer. There is a limit of 25 on the number of messages printed.

No errors have been found

The circuit has no errors detected by this part of the MacroMatrix software.

```
**************************************************************
*                                                            *
*          PIN CLASS ERC                                     *
*          VERSION  2.7Ø                                     *
*                                                            *
**************************************************************


   Path Name /USER/CLASS/QUICK
   Product Name PRODUCT_NAME
   Circuit family Q5ØØØ
   Circuit technology M
   Date 18 OCT 1988
   Time 16:2Ø
   Product Grade PRODUCT_GRADE


ERROR7Ø5: ILLEGAL PARAMETRIC WIRE-OR HAS BEEN USED
          Driving Component=ØC6 Macro=UT66
          Signal=XSIG14
          Page= 1
ERROR7Ø5: ILLEGAL PARAMETRIC WIRE-OR HAS BEEN USED
          Driving Component=ØC18 Macro=OT63L
          Signal=XSIG9
          Page= 1

   Number of errors found = 2
```

```
**************************************************************
*          PIN CLASS ERC                                     *
*          VERSION  2.7Ø                                     *
**************************************************************

   Path Name /USER/CLASS/Q532REG
   Product Name Q5REG32
   Circuit family Q5ØØØ
   Circuit technology M
   Date  7 OCT 1988
   Time 1Ø:39
   Product Grade MIL


   No errors found.
```

Section 8-8, Pin Priority Check, has been deleted.

• POPULATION - (ALL) Determines cell population and macro type population for a given design. Prints a matrix of that used and that available and generates a printed error message when array resources have been exceeded. Issues warnings when a design has exceeded certain design guidelines.

• VTI CHECK - (Q700 Bipolar Logic Array Series) Computes the number of VTI threshold generator loads and states them. Indicates if the loading is excessive for the array. VTI loads are listed in the macro documentation.

INTRODUCTION

The population ERC computes the cell count of the circuit design as captured, compares it to the specific array selected by the chip macro, and generates a population and cell usage report. Cell population is computed for inputs, outputs and bidirectional macros and their cell usage as well as for the internal logic macros, including both single and multiple-cell MSI macros.

Cell count computation is done to 1/2 cell accuracy.

After the total cell counts are extracted for each cell type, the totals are compared to the maximum for each cell type allowed for the array. If an error condition is found, an error message is sent to the report file. One error message is issued for each violation.

Internal cell usage is reported as cell utilization and an error generated if the internal cell utilization exceeds that allowed for the array.

The external pin count and signal pin count are computed and reported. An error message is generated when the signal pin count (all interface signals plus all added power and ground) exceeds that allowed for the given array.

POWER AND GROUND PADS:

Bipolar and BiCMOS arrays provide all of the recommended minimum number of power and ground pins as fixed pad locations. Additional power and ground may be added using ITPWR, ITGND and IEVCC (ECL I/O VCC). The Q700 array design guide should be referenced for M7ExPWR and M7ExGND.

ADDED POWER AND GROUND FOR SIMULTANEOUSLY SWITCHING OUTPUTS

The check for sufficient added power and ground pins to accommodate the simultaneously switching outputs identified by the macro parameter SWGROUP is part of the I/O LIST ERC module. Refer to that section for warning messages.

VTI LOAD LIMIT - Q700 Series

For the Q700 Logic Array Series, the ERC also computes the number of high speed TTL macros used on a particular circuit. There is a limit as to how many TTL inputs can be placed on one of these arrays when high speed macros are used. This is not an I/O I_{CC} limitation but rather a limitation of the TTL input threshold VTI generator.

Standard TTL input macros count as 1 VTI load. High-speed TTL input macros count as 6 loads for the Q700 Series. The maximum number of VTI loads allowed for an array is defined in Appendix A of the appropriate Design Guide.

SAMPLE REPORT

```
*******************************************************
*          POPULATION ERC                             *
*          VERSION 2.80                               *
*******************************************************
```

Path Name /USER/CLASS/MUX16
Product Name MUX16
Circuit family Q5000
Circuit technology P
Date 20 SEP 1988
Time 09:58
Product Grade MIL

	Circuit	Available	
SUM_INPUT:	23.0		PADS
SUM_OUTPUT:	5.0		PADS
SUM_X_TTL_PWR:	3.0		PADS
SUM_X_TTL_GND:	3.0		PADS
SUM_X_ECL_VCC:	3.0		PADS
SUM_TOTAL_I/O	42	160.0	CELLS
SUM_INTERNAL	11	352.0	CELLS
TOTAL ARRAY PADS	61.0	184.0	PADS

Cell utilization is: 2.7%

Total fixed power pins:	12	[pads]
Total fixed ground pins:	12	
Total added power pins:	6	
Total added ground pins:	3	
Total input signals:	23	
Total output signals:	5	
Total bidirectional signals:	0	

No errors found.

SUM_INPUT shows the number of I cells (pads) required where the array has I cells. Where an array has no I cells, it shows the number of cells required by input-only macros. If an MSI input macro uses more than 1 cell, the number of cells required is correctly counted.

SUM_OUTPUT shows the number of O cells (pads) required where the array has O cells. Where an array has none, it shows the number of cells required by output-only macros. If an MSI output macro uses more than 1 cell, the number of cells required is correctly counted. (OE10)

If an array has no limit on I or O cells, then none will appear under "available". If a macro can be placed on more than one cell type, it will not be listed under "CIRCUIT" for any one type. The overall limit will be caught under the total I/O cell count in "SUM_TOTAL_I/O".

SUM_BIDIREC shows the number of cells (pads) required by the bidirectional macros used in the design. Q14000 Series arrays are limited in the number of bidirectional macro cells that may appear on a circuit. If the array has no limit then none will appear under "available".

SUM_X_TTL_PWR shows the number of cells (pads) required by the use of ITPWR (Bipolar; BiCMOS) macros. There is no entry under available for bipolar or BiCMOS arrays.

SUM_X_TTL_GND shows the number of cells (pads) required by the use of ITGND (Bipolar; BiCMOS) macros. There is no entry under available for bipolar or BiCMOS arrays.

SUM_X_ECL_VCC shows the number of cells (pads) required by the addition of added ECL I/O VCC pins, added via the IEVCC macros. There is no entry under available for bipolar or BiCMOS arrays.

"SUM_TOTAL_I/O" counts all I/O cells used. This includes the 3-state enable drivers (INTERNAL) which sit on I/O cells but which do not show up in the external pin count. This includes all input (optional placement), all output, all 3-state drivers, all added ITPWR, IEVCC, ITGND, etc. The sum of the I/O cells available is shown. The number of I/O cells available for the array is shown under "available" for all arrays.

The addition of all I, O and Bidirectional pads will not always total the sum of all I/O cells used due to the internal 3-state enable drivers. Refer to the I/O statistics report.

For bipolar arrays, SUM_LOGIC shows the number of internal L and B cells required by all internal macros. The sum of the internal cells available is shown. For BiCMOS arrays, the SUM_LOGIC term counts the number of basic cells required by all internal macros.

"TOTAL ARRAY PADS" counts all PADs (pads going off-array), including signals, fixed power and ground and added power and ground. The number of power, ground and signals are detailed in comments below the table. If, in the physical circuit, two pads have been tied together to connect to one pin, CONSULT AMCC for simulation requirements.

The cell utilization shows the internal cell utilization due to all macros placed on L and B (bipolar) or basic (BiCMOS) cells. Internal cell utilization coupled with internal pin counts will indicate circuit routability. An error is issued if the internal cell utilization exceeds that recommended for the array.

There is no check at present for H-option and driver macro cell utilization.

Total fixed power pads [pins] shows the count of fixed +5V pads, and the fixed -5.2V or -4.5V ECL VEE pads. Sums the fixed TTLVCC, and, for a +5V only system, the fixed ECLVCC.

Total added power pads [pins] shows the count of added +5V pads. For a +5V only system, includes the added IEVCC.

Total fixed ground pads [pins] counts fixed ground pins. Sums the fixed TTLGND, and, for a -5.2V or -4.5V ECL system, adds the fixed ECLVCC. For a +5V system, adds the fixed ECLVEE.

Total added ground pads [pins] counts the added ITGND and, in a standard reference -5.2V or -4.5V ECL system, the added IEVCC.

Total pads used for signals shows the pad count for the I/O signals. The pad count and the I/O cell count may vary due to 3-state enable drivers. Note: The ERC does not recognize pad to pin alterations (two pads tied together to one signal pin count as two pads.)

ERROR REPORTS

A description of errors follows. All error messages give the component name and pin name information in sufficient detail to allow location within the schematic set.

ERROR300: TOTAL INPUT CELLS USED EXCEEDS THAT ALLOWED
FOR THIS ARRAY BY: .....

More input (I) cells have been used than allowable for the array. This error message is used for both Bipolar, CMOS and BiCMOS arrays.

ERROR301: TOTAL OUTPUT CELLS USED EXCEEDS THAT ALLOWED
FOR THIS ARRAY BY: .....

Q5000T Array: More output (O) cells have been used than allowable for the array. For the Q5000T array, the number of output macros is limited. Since they are placed on I/O cells, this is not detected by the I/O cell count check. This check indicates that more than 120 output macros have been used for the array. The limit is 30 per side and 30 per quadrant and the final check is done during placement. Macros such as OE10 count as 2 cells.

ERROR302: TOTAL I/O CELL USED EXCEEDS THAT ALLOWED
FOR THIS ARRAY BY: .....

More I/O cells have been used than allowable for the array. This message is used for both Bipolar, CMOS and BiCMOS arrays. Input, Output, Bidirectional.

ERROR303: TOTAL INTERFACE CELLS USED EXCEEDS THAT
ALLOWED FOR THIS ARRAY BY: .....

More signal pins have been used (and therefore pads and interface cells) than allowable for this array. This message is used for both Bipolar and BiCMOS arrays. This test means that the total interface macro usage exceeds that allowed, and takes into account the optionally placed cells; whereas the above messages were for specific overuse of cell types by the macros that could only be placed on those cells.

ERROR304: TOTAL INTERNAL CELLS USED EXCEEDS THAT ALLOWED
FOR THIS ARRAY BY: .....

Informs the user of internal function cell (L and B cells) population errors. More function cells have been used than are allowable for the circuit family. All but the ECL output buffers may be placed on L or B cells. B cell population is checked separately. For the Q3500, Q5000 Series arrays, the internal cell check is the same as an L cell population check.

ERROR305: TOTAL B CELLS USED EXCEEDS THAT ALLOWED
FOR THIS ARRAY BY: .....

For bipolar arrays (Q700 Series arrays), informs the user that the number of B cells used in a bipolar design exceeds that available with the array. B cells are required for ECL output buffers. (Q700 Series.)

ERROR308: TOTAL RAM CELLS USED EXCEEDS THAT ALLOWED
FOR THIS ARRAY BY: .....

Informs the user that the number of RAM macros used exceeds the number that may be used with the array. (QM1600S, QM1600T.)

ERROR309: TOTAL BASIC CELLS USED EXCEEDS THAT ALLOWED
FOR THIS ARRAY BY: .....

Informs the user that the number of basic (internal) cells used in a BiCMOS design exceeds the number that may be used for the array.

ERROR310: NO CELL COUNT PARAMETER

Indicates that no cell count or size parameter was found. Contact AMCC if this error occurs.

ERROR311: NO CIRCUIT FAMILY PARAMETER ON THE CHIP MACRO

Informs the user that the chip macro is missing a circuit family parameter. Contact AMCC if this error occurs.

ERROR312: ARRAY NAME PARAMETER NOT FOUND

This should be supplied by the selection of a chip macro and its placement on page one of the schematics. Consult AMCC if the chip macro was selected and this message is generated.

ERROR313: MPF CONTAINS AN ILLEGAL CELL COUNT

Informs the user that the macro parameter file has invalid data, specifically invalid cell count information. Contact AMCC if this error occurs.

ERROR314: VTI LOADING EXCEEDS LIMITS FOR THIS ARRAY BY:
.....

Informs the user that the VTI generator has been overloaded. Either high-speed macros must be replaced by standard option macros wherever possible until the circuit is within array limits. (Q700 Series only.)

ERROR316: TOTAL BIDIRECTIONAL I/O MACROS EXCEEDS THAT ALLOWED FOR THIS ARRAY BY: .....

BiCMOS (Q14000 Series) arrays limit the number of bidirectional I/O macros that may be used. (They must all appear on the LEFT side of the array in placement.) (BiCMOS Arrays.)

WARN317: CELL UTILIZATION EXCEEDS THAT RECOMMENDED FOR THIS ARRAY

Each array has a cell utilization figure which is used to serve as a guideline for the routability of a design. High utilization, high internal pin count and layout restrictions can mean a circuit will have problems. AMCC prefers that the design be kept within the recommended cell utilization limits. Generate when the INTERNAL_CELL _USAGE > CELL_UTILIZATION_LIMIT

ERROR318: TOTAL ECL 10K/100K SERIES CELLS USED EXCEEDS THAT ALLOWED FOR THIS ARRAY BY: .....

Q20000 Series: The number of cells used by ECL 10K and ECL 100K on-chip series terminated output macros and ECL 10K and ECL 100K on-chip series terminated bidirectional macros is limited to 8 per quadrant (placement check limit) or 32 per array (preplacement) for all arrays in the Q20000 Series. An on-chip series terminated macro may also be a Darlington macro.

ERROR319: TOTAL TTL OUTPUT CELLS USED EXCEEDS THAT ALLOWED FOR THIS ARRAY BY:.....

Q20000 Series: The number of cells used by TTL output and bidirectional macros is limited to 16 for the Q20160 array (one side) and to 8 per quadrant (placement check limit) or 32 per array (preplacement) for all other arrays in the Q20000 Series.

ERROR320: TOTAL DARLINGTON OUTPUT CELLS USED EXCEEDS THAT ALLOWED FOR THIS ARRAY BY: .....

Q20000 Series: The number of cells used by Darlington type macros (outputs; bidirectionals) is limited to 8 per quadrant (placement check limit) or 32 per array (preplacement) for all arrays in the Q20000 Series.

ERROR321: THIS MACRO CANNOT BE USED WITH THIS CHIP MACRO

Q14000 Series: If an I/O macro that belongs to the Q6000B or Q14000B sea-of-gates architecture are used on a Q2100B or Q9100B array this error will be generated. It will be generated if the reverse occurs. These two sets of BiCMOS arrays have unique I/O macros. Refer to the macro documentation, Volume I, Section 6.

Q20000 Series: The single-cell 25ohm termination ECL output macros cannot be placed on single power suppy (+5V) circuits. Use the dual cell 25ohm ECL outputs. Refer to Volume I, Section 6.

INFORMATION ONLY:

Number of errors found = n

If errors are found, this statement will inform the designer. There is a limit of 25 on the number of messages printed.

No errors have been found

The circuit has no errors detected by this part of the MacroMatrix software.

```
**********************************************************
*          POPULATION ERC                                *
*          VERSION  2.8Ø                                 *
**********************************************************

   Path Name /USER/CLASS/Q532REG                GOOD
   Product Name Q5REG32
   Circuit family Q5ØØØ
   Circuit technology M
   Date  7 OCT 1988
   Time 1Ø:39
   Product Grade MIL



   No errors found.

                     Circuit   Available
-------------------------------------
SUM_INPUT:             42.Ø              PADS
SUM_OUTPUT:            69.Ø              PADS
SUM_X_TTL_PWR:          4.Ø              PADS
SUM_X_TTL_GND:          5.Ø              PADS
-------------------------------------
SUM_TOTAL_I/O         12Ø.Ø    12Ø.Ø    CELLS
SUM_INTERNAL           43.5    242.Ø    CELLS
-------------------------------------
TOTAL ARRAY PADS      148.Ø    148.Ø    PADS
-------------------------------------

Cell utilization is:                  18.Ø %

Total fixed power pins:                1Ø
Total fixed ground pins:               18
Total added power pins:                 4
Total added ground pins:                5

Total input signals:                   42
Total output signals:                  69
Total bidirectional signals:            Ø
```

```
*************************************************************
*          POPULATION ERC                                   *
*          VERSION  2.8Ø                                    *
*************************************************************
```

BAD

```
   Path Name /USER/CLASS/QUICK
   Product Name PRODUCT_NAME
   Circuit family Q5ØØØ
   Circuit technology M
   Date 18 OCT 1988
   Time 16:2Ø
   Product Grade PRODUCT_GRADE
                    •
                    •
                    •
ERROR225: MORE THAN ONE CHIP MACRO (USING FIRST FOUND)
          Component=13CØ Macro=Q13ØØTTTL
          Page= 14
ERROR225: MORE THAN ONE CHIP MACRO (USING FIRST FOUND)
          Component=16C2 Macro=QM16ØØTECL1ØØK
          Page= 17
ERROR225: MORE THAN ONE CHIP MACRO (USING FIRST FOUND)
          Component=16C3 Macro=QM16ØØTMIX1ØK
          Page= 17
ERROR LIMIT EXCEEDED.

   Number of errors found = 34

                     Circuit   Available
-------------------------------------------
SUM_INPUT:             53.Ø              PADS
SUM_OUTPUT:            43.Ø              PADS
SUM_BIDIR:              6.Ø              PADS
SUM_X_TTL_PWR:          2.Ø              PADS
SUM_X_TTL_GND:          5.Ø              PADS
SUM_X_ECL_GND:          3.Ø              PADS
-------------------------------------------
SUM_TOTAL_I/O         117.Ø      76.Ø   CELLS
SUM_INTERNAL          381.5      84.Ø   CELLS
-------------------------------------------
TOTAL ARRAY PADS      128.Ø      92.Ø   PADS
-------------------------------------------

Cell utilization is:                454.2 %

Total fixed power pins:               8
Total fixed ground pins:              8
Total added power pins:               2
Total added ground pins:              8

Total input signals:                 53
Total output signals:                43
Total bidirectional signals:          6
```

I/O STATISTICS ERC

As a further aid to the designer, an I/O population statistic report has been added to the ERCs. This report will detail by type the interface macros used in a design. It will highlight thermal diode connections, VBxx, AC monitors as well as report on ECL 10K and ECL 100K outputs, bidirectionals and 3-state macros and their drivers.

```
*************************************************************
*          I/O Statistics ERC                               *
*          VERSION  1.40                                    *
*************************************************************

   Path Name /USER/CLASS/QUICK
   Product Name PRODUCT_NAME
   Circuit family Q5000
   Circuit technology M
   Date 18 OCT 1988
   Time 16:20
   Product Grade PRODUCT_GRADE
```

	number of Objects in the circuit	Object type
Inputs		
TTL	13	PAD
ECL	36	PAD
SubTotal	49	PAD
Outputs		
TTL	12	PAD
ECL10K	12	PAD
ECL100K	3	PAD
Thermal Diode Connections	4	PAD
SubTotal	31	PAD
Bidirectionals		
TTL	4	PAD
ECL10K	2	PAD
SubTotal	6	PAD
Tristates		
INTERNAL	4	CELL
SubTotal	4	

```
*************************************************************
*          I/O Statistics ERC                               *
*          VERSION  1.3Ø                                    *
*************************************************************
```

Path Name /USER/CLASS/Q532REG
Product Name Q5REG32
Circuit family Q5ØØØ
Circuit technology M
Date 7 OCT 1988
Time 1Ø:39
Product Grade MIL

	number of Objects in the circuit	Object type
Inputs		
ECL	42	PAD
SubTotal	42	PAD
Outputs		
TTL	64	PAD
ECL1ØK	1	PAD
Thermal Diode Connections	4	PAD
SubTotal	69	PAD
Tristates		
INTERNAL+GROUND	4	CELL
SubTotal	4	

SIGNAL I/O LIST

The AMCCERC SIGNAL I/O LIST CHECK will report warnings and errors in the use of added power and grounds with switching groups to the AMCCERC.LST report if and only if the SWGROUP parameter (or property) was used. AMCCERC will also generate an I/O list called AMCCIO.LST located in the same directory.

The designer must submit AMCCIO.LST as part of the design submission. The list is sorted by signal name and includes all PAD signals, including fixed power and ground.

If the simultaneously switching parameter SWGROUP has been used, the number of simultaneously switching outputs in each group will be counted and recorded by group name for inclusion in AMCCIO.LST.

AMCC requires the the SWGROUP parameter be used on all simultaneously switching outputs and the parameter value MUST be visible on the schematic. The parameter is attached to the output macro. The parameter is also attached to any power and ground macros added to handle the particular switching group.

The switching group report is placed at the end of the I/O list and will correctly include the number of outputs involved in simultaneous switching. OE10, for example, will count as two outputs.

The array documentation in Volume I, Section 2, contains the tables for recommended added power and ground based on I/O mode and the number of simultaneously switching outputs.

The SWITCHING GROUP report also shows the required minimum and maximum added power and grounds required for each group.

- A warning will be issued to the ERC report, AMCCERC.LST, if the number of added power and grounds is less than the possible maximum required (worst-case placement) for the group size but equal to or greater than the required minimum.

- An error will be issued to the ERC report if the number of added power an grounds is less than the computed required minimum (best-case placement).

****
* SIGNAL I/O LIST *
****

The signal I/O list records (one per primary signal or power/ground pin) contain the following:

SIGNAL NAME:

The user-defined name of the primary input, output or bidirectional signal. Fixed power and ground is not listed. Added power and ground are listed as ITPWR, ITGND and ITEVCC. Fixed power and ground are listed as labeled on the chip macros. For example: ECL IO VCC, ECLVCC, ECLVEE, TTLVCC and TTLGND are used for Bipolar arrays.

OE10 requires two entries since it has two pads. Note the two outputs of OE10 count as TWO outputs when computing simultaneous switching group sizes.

INSTANCE NAME

The user-defined macro occurrence name or instance name for the macro to which the signal is connected is listed.

MACRO NAME

The AMCC macro name for the macro to which the signal is connected is listed.

LOGIC LEVEL:

This will be automatically entered to identify the logic level, TTL, CMOS or ECL, and ECL type, ECL 10K or ECL 100K, based on the specific macros chosen. Fixed and added power and grounds will show voltage level (5V, 0V, -4.5V, -5.2V).

I/O TYPE:

This will be automatically entered as I, O or BI for input, output or bidirectional, respectively. Fixed and added power and grounds will appear as P or G respectively.

SWITCH GROUP:

This will be automatically entered, if the designer has used the SWGROUP parameter. The value assigned to a parameter on an individual macro will appear. Values are alphanumeric and follow EWS naming conventions.

DIFF PAIRS (Differential pairs)

This will be automatically entered based on the macros and their use. The paris are marked by lower case (a,b,c) letter pairs.

FAN-IN I_{IL}, I_{IH}

This will be automatically entered for the macros based on the entries in the macro parameter file.

On the last page of the report, the I/O list summary is printed (this is the same summary printed on the population report):

****
* I/O LIST SUMMARY *
****

TOTAL INPUTS: The count of all input signals.

TOTAL OUTPUTS: The count of all output signals.

TOTAL BIDIRECTIONALS: The count of all bidirectional signals.

TOTAL EXTRA POWER: The count of all added power pads. Counts IEVCC if the circuit ECL power supply is +5V.

TOTAL EXTRA GROUND: The count of all added ground pads. Counts IEVCC if the circuit ECL power supply is -5.2V or -4.5V.

TOTAL FIXED POWER: The count of all fixed power pads (+5V and/or -5.2V or -4.5V pins).

TOTAL FIXED GROUND: The count of all fixed ground pads (0V).

Beneath the Signal I/O List report, a summary of the switching groups is printed:

```
*************************
*    SWITCHING GROUPS   *
*************************

SWITCHING GROUP:   SIZE :   TYPE:    PWR:     GND:
-------------------------------------------------------
  value1             ...      ...     ...       ...
  value2             ...      ...     ...       ...
  value3             ...      ...     ...       ...
  value4             ...      ...     ...       ...
          etc.
-------------------------------------------------------
TOTAL # SIMULTANEOUSLY SWITCHING TTL OUTPUTS:  ......
TOTAL # SIMULTANEOUSLY SWITCHING ECL OUTPUTS:  ......
-------------------------------------------------------
```

SWITCHING GROUP:

Under this column the ERC lists the names of the switching groups, assigned via the unique value assigned to the SWGROUP parameter/property. The value is alphameric, following AMCC schematic naming rules for instance names.

SIZE:

Under this column the ERC lists the number of outputs tagged as belonging to each identified group. (If other macros are mistakenly tagged they are not counted.) Extra power and ground macros are recognized as being tagged and as belonging to a specific group but are not counted in the group size. A group may be empty.

TYPE: (ECL/TTL)

Under this column the ERC lists either TTL or ECL. For switching groups with both, there will be two line entries.

ADDED POWER PINS REQUIRED
MIN-MAX / SUPPLIED

Under the min-max column, the ERC lists the minimum number of power pads required assuming best-case placement (even distribution amoung the quadrants) and the maximum number required assuming worst-case placement (done assuming everything is in one quadrant).

Under the supplied column the ERC lists the number of extra power pads added by the designer and tagged as belonging to the switch group. For a TTL group this would be the ITPWR macro count or its equivalent. For a ECL group, this would depend on the power supply mode. For standard ECL, this field will be empty. For +5V ref ECL, this field will be the IEVCC macro count.

ADDED GROUND PINS REQUIRED
MIN-MAX / SUPPLIED

Under the min-max column, the ERC lists the minimum number of ground pads required assuming best-case placement (even distribution amoung the quadrants) and the maximum number required assuming worst-case placement (done assuming everything is in one quadrant).

Under the supplied column the ERC lists the number of extra ground pads added by the designer and tagged as belonging to the switch group. For a TTL group this would be the ITGND macro count or its equivalent. For a ECL group, this would depend on the power supply mode. For standard ECL, this field will be the IEVCC macro count. For +5V REF ECL, this field will be empty.

ERROR REPORTS

A description of errors and warnings follows.

ERROR200: INSUFFICIENT TTL POWER HAS BEEN PROVIDED

DISCONTINUED

ERROR201: INSUFFICIENT TTL GROUND HAS BEEN PROVIDED

DISCONTINUED

WARNING202: INSUFFICIENT TTL POWER HAS BEEN PROVIDED
FOR SWITCHING GROUP: .....
ADDITIONAL TTL POWER MAY BE REQUIRED
DEPENDING ON THE FINAL PLACEMENT

Issued when less then the worst-case placement minimum has been provided for a switching group. Informs the user that additional TTL power macros may be required for an array based on the number of simultaneously switching outputs in a group. Consult with AMCC Application Engineering.

WARNING203: INSUFFICIENT TTL GROUND HAS BEEN PROVIDED
FOR SWITCHING GROUP: .....
ADDITIONAL TTL GROUND MAY BE REQUIRED
DEPENDING ON THE FINAL PLACEMENT

Issued when less then the worst-case placement minimum has been provided for a switching group. Informs the user that additional TTL ground macros may be required for an array based on the number of simultaneously switching outputs in a group. Consult with AMCC Applications Engineering.

WARNING204: INSUFFICIENT ECL VCC HAS BEEN PROVIDED
FOR SWITCHING GROUP: .....
ADDITIONAL ECL VCC MAY BE REQUIRED
DEPENDING ON THE FINAL PLACEMENT

Issued when less then the worst-case placement minimum has been provided for a switching group. Informs the user that additional ECL VCC macros may be required for an array based on the number of simultaneously switching outputs in a group. Consult with AMCC Applications Engineering.

ERROR205: INSUFFICIENT ECL VCC HAS BEEN PROVIDED
FOR SWITCHING GROUP: .....

Issued when less then the best-case placement minimum has been provided for a switching group. Informs the user that additional ECL VCC macros are required for an array based on the number of simultaneously switching outputs in a group. Add IEVCC macros for the switching group.

ERROR206: INSUFFICIENT TTL POWER HAS BEEN PROVIDED
FOR SWITCHING GROUP: .....

Issued when less then the best-case placement minimum has been provided for a switching group. Informs the user that additional TTL power macros are required for an array based on the number of simultaneously switching outputs in a group. Add ITPWR macros for the switching group..

ERROR207: INSUFFICIENT TTL GROUND HAS BEEN PROVIDED
FOR SWITCHING GROUP: .....

Issued when less then the best-case placement minimum has been provided for a switching group. Informs the user that additional TTL ground macros are required for an array based on the number of simultaneously switching outputs in a group. Add ITGND macros for the switching group.

INFORMATION ONLY:

Number of errors found = n

If errors are found, this statement will inform the designer.

No errors have been found

The circuit has no errors detected by this part of the MacroMatrix software.

```
**************************************************
*                                                *
*        SIGNAL I/O LIST                         *
*        REVISION 1.0                            *
*                                                *
**************************************************


    Path Name /USER/CLASS/Q532REG
    Product Name Q5REG32
    Circuit family Q5000
    Circuit technology M
    Date 7 OCT 1988
    Time 10:39
    Product Grade MIL


WARNING202: INSUFFICIENT TTL POWER HAS BEEN PROVIDED FOR SWITCH GRP AAA
            ADDITIONAL TTL POWER MAY BE REQUIRED DEPENDING
            ON THE FINAL PLACEMENT
WARNING203: INSUFFICIENT TTL GROUND HAS BEEN PROVIDED FOR SWITCH GRP AAA
            ADDITIONAL TTL GROUND MAY BE REQUIRED DEPENDING
            ON THE FINAL PLACEMENT

    No errors found.
```

AMCCERC.LST REPORT

```
*********************************
* I/O LIST SUMMARY              *
*********************************

Total fixed power pins:                10
Total fixed ground pins:               18
Total added power pins:                 4
Total added ground pins:                5

Total input signals:                   42
Total output signals:                  69
Total bidirectional signals:            0


*********************************
* SWITCHING GROUPS              *
*********************************

                    !      !            ! ADDED POWER PINS     ! ADDED GROUND PINS
SWITCHING GROUP     !      !    TYPE    ! REQUIRED             ! REQUIRED
NAME                ! SIZE ! (ECL/TTL) ! MIN--MAX / SUPPLIED  ! MIN--MAX / SUPPLIED
--------------------------------------------------------------------------------
AAA                   64       TTL          4 -  7 /    4          4 -  7 /    5
--------------------------------------------------------------------------------
TOTAL # SIMULTANEOUSLY SWITCHING TTL OUTPUTS: 64
TOTAL # SIMULTANEOUSLY SWITCHING ECL OUTPUTS:  0
-----------------------------------------------------
```

```
**************************************************************
*          SIGNAL I/O LIST                                   *
*          REVISION  3.20                                    *
**************************************************************

   Path Name /USER/CLASS/Q532REG
   Product Name Q5REG32
   Circuit family Q5000
   Circuit technology M
   Date  7 OCT 1988
   Time 10:39
   Product Grade MIL


*********************************
* SIGNAL I/O LIST               *
*********************************
```

ITEM #	SIGNAL NAME	INSTANCE NAME	MACRO NAME	LOGIC LEVEL	I/O TYPE	SWITCH GROUP	DIFF PAIRS	FAN-IN IIL(uA)	FAN-IN IIH(uA)
1	DI00	EI0007	IE93	ECL	I			0.00	0.00
2	DI01	EI0008	IE93	ECL	I			0.00	0.00
3	DI02	EI0009	IE93	ECL	I			0.00	0.00
4	DI03	EI0010	IE93	ECL	I			0.00	0.00
5	DI04	EI0011	IE93	ECL	I			0.00	0.00
6	DI05	EI0012	IE93	ECL	I			0.00	0.00
7	DI06	EI0013	IE93	ECL	I			0.00	0.00
8	DI07	EI0014	IE93	ECL	I			0.00	0.00
9	DI08	EI0015	IE93	ECL	I			0.00	0.00
10	DI09	EI0016	IE93	ECL	I			0.00	0.00
11	DI10	EI0017	IE93	ECL	I			0.00	0.00
12	DI11	EI0018	IE93	ECL	I			0.00	0.00
13	DI12	EI0019	IE93	ECL	I			0.00	0.00
14	DI13	EI0020	IE93	ECL	I			0.00	0.00
15	DI14	EI0021	IE93	ECL	I			0.00	0.00
16	DI15	EI0022	IE93	ECL	I			0.00	0.00
17	DI16	EI0023	IE93	ECL	I			0.00	0.00
18	DI17	EI0024	IE93	ECL	I			0.00	0.00
19	DI18	EI0025	IE93	ECL	I			0.00	0.00
20	DI19	EI0026	IE93	ECL	I			0.00	0.00
21	DI20	EI0027	IE93	ECL	I			0.00	0.00
22	DI21	EI0028	IE93	ECL	I			0.00	0.00
23	DI22	EI0029	IE93	ECL	I			0.00	0.00
24	DI23	EI0030	IE93	ECL	I			0.00	0.00
25	DI24	EI0031	IE93	ECL	I			0.00	0.00
26	DI25	EI0032	IE93	ECL	I			0.00	0.00
27	DI26	EI0033	IE93	ECL	I			0.00	0.00

65	!ENA	!IE003	!IE93	! ECL	! I	!	!	!	!	! Ø.ØØ	!	Ø.ØØ !
66	!ENB	!IE004	!IE93	! ECL	! I	!	!	!	!	! Ø.ØØ	!	Ø.ØØ !
67	!ENC	!IE005	!IE93	! ECL	! I	!	!	!	!	! Ø.ØØ	!	Ø.ØØ !
68	!EXTCAN	!IE001	!IE85	! ECL	! I	!	!	! a	!	! Ø.ØØ	!	Ø.ØØ !
69	!EXTCKA	!IE000	!IE90	! ECL	! I	!	!	! a	!	! Ø.ØØ	!	Ø.ØØ !
70	!EXTRST	!IE002	!IE93	! ECL	! I	!	!	!	!	! Ø.ØØ	!	Ø.ØØ !
71	!PARAM	!EO11ØØ	!OE81	! ECL1ØK	! O	!	!	!	!	!	!	!
72	!TDOØØ	!TOØØØ1	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
73	!TDOØ1	!TOØØØ3	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
74	!TDOØ2	!TOØØØ5	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
75	!TDOØ3	!TOØØØ7	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
76	!TDOØ4	!TOØØØ9	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
77	!TDOØ5	!TOØØ11	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
78	!TDOØ6	!TOØØ13	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
79	!TDOØ7	!TOØØ15	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
8Ø	!TDOØ8	!TOØØ17	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
81	!TDOØ9	!TOØØ19	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
82	!TDO1Ø	!TOØØ21	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
83	!TDO11	!TOØØ23	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
84	!TDO12	!TOØØ25	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
85	!TDO13	!TOØØ27	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
86	!TDO14	!TOØØ29	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
87	!TDO15	!TOØØ31	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
88	!TDO16	!TOØØ33	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
89	!TDO17	!TOØØ35	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
9Ø	!TDO18	!TOØØ37	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
91	!TDO19	!TOØØ39	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
92	!TDO2Ø	!TOØØ41	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
93	!TDO21	!TOØØ43	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
94	!TDO22	!TOØØ45	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
95	!TDO23	!TOØØ47	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
96	!TDO24	!TOØØ49	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
97	!TDO25	!TOØØ51	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
98	!TDO26	!TOØØ53	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
99	!TDO27	!TOØØ55	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
1ØØ	!TDO28	!TOØØ57	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
1Ø1	!TDO29	!TOØØ59	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
1Ø2	!TDO3Ø	!TOØØ61	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
1Ø3	!TDO31	!TOØØ63	!OT63H	! TTL	! O	!AAA	!	!	!	!	!	!
1Ø4	!TDS11Ø1	!TD11Ø1	!OE87	! ECL1ØK	! O	!	!	!	!	!	!	!
1Ø5	!TDS11Ø2	!TD11ØØ	!OE87	! ECL1ØK	! O	!	!	!	!	!	!	!
1Ø6	!TDS11Ø3	!TD11Ø3	!OE87	! ECL1ØK	! O	!	!	!	!	!	!	!
1Ø7	!TDS11Ø4	!TD11Ø2	!OE87	! ECL1ØK	! O	!	!	!	!	!	!	!

108	!TEN1	!IE2006	!IE93	! ECL	! I	!	!	!	! Ø.ØØ	!	Ø.ØØ	!
109	!TEN2	!IE2007	!IE93	! ECL	! I	!	!	!	! Ø.ØØ	!	Ø.ØØ	!
110	!TEN3	!IE2008	!IE93	! ECL	! I	!	!	!	! Ø.ØØ	!	Ø.ØØ	!
111	!TEN4	!IE2009	!IE93	! ECL	! I	!	!	!	! Ø.ØØ	!	Ø.ØØ	!
112	!ITGND	!GND200	!OT59H	! TTL	! G	!AAA	!	!	!	!	!	!
113	!ITGND	!GND201	!OT59H	! TTL	! G	!AAA	!	!	!	!	!	!
114	!ITGND	!GND202	!OT59H	! TTL	! G	!AAA	!	!	!	!	!	!
115	!ITGND	!GND203	!OT59H	! TTL	! G	!AAA	!	!	!	!	!	!
116	!ITGND	!GT0000	!ITGND	! TTL	! G	!AAA	!	!	!	!	!	!
117	!ITPWR	!PT0000	!ITPWR	! TTL	! P	!AAA	!	!	!	!	!	!
118	!ITPWR	!PT0001	!ITPWR	! TTL	! P	!AAA	!	!	!	!	!	!
119	!ITPWR	!PT0002	!ITPWR	! TTL	! P	!AAA	!	!	!	!	!	!
120	!ITPWR	!PT0003	!ITPWR	! TTL	! P	!AAA	!	!	!	!	!	!
121	!ECLIOVCC	!	!	! ØV	! G	!	!	!	!	!	!	!
122	!ECLIOVCC	!	!	! ØV	! G	!	!	!	!	!	!	!
123	!ECLIOVCC	!	!	! ØV	! G	!	!	!	!	!	!	!
124	!ECLIOVCC	!	!	! ØV	! G	!	!	!	!	!	!	!
125	!ECLVCC	!	!	! ØV	! G	!	!	!	!	!	!	!
126	!ECLVCC	!	!	! ØV	! G	!	!	!	!	!	!	!
127	!ECLVCC	!	!	! ØV	! G	!	!	!	!	!	!	!
128	!ECLVCC	!	!	! ØV	! G	!	!	!	!	!	!	!
129	!ECLVCC	!	!	! ØV	! G	!	!	!	!	!	!	!
130	!ECLVCC	!	!	! ØV	! G	!	!	!	!	!	!	!
131	!ECLVEE	!	!	! -5.2V	! P	!	!	!	!	!	!	!
132	!ECLVEE	!	!	! -5.2V	! P	!	!	!	!	!	!	!
133	!ECLVEE	!	!	! -5.2V	! P	!	!	!	!	!	!	!
134	!ECLVEE	!	!	! -5.2V	! P	!	!	!	!	!	!	!
135	!ECLVEE	!	!	! -5.2V	! P	!	!	!	!	!	!	!
136	!ECLVEE	!	!	! -5.2V	! P	!	!	!	!	!	!	!
137	!TTLGND	!	!	! ØV	! G	!	!	!	!	!	!	!
138	!TTLGND	!	!	! ØV	! G	!	!	!	!	!	!	!
139	!TTLGND	!	!	! ØV	! G	!	!	!	!	!	!	!
140	!TTLGND	!	!	! ØV	! G	!	!	!	!	!	!	!
141	!TTLGND	!	!	! ØV	! G	!	!	!	!	!	!	!
142	!TTLGND	!	!	! ØV	! G	!	!	!	!	!	!	!
143	!TTLGND	!	!	! ØV	! G	!	!	!	!	!	!	!
144	!TTLGND	!	!	! ØV	! G	!	!	!	!	!	!	!
145	!TTLVCC	!	!	! 5V	! P	!	!	!	!	!	!	!
146	!TTLVCC	!	!	! 5V	! P	!	!	!	!	!	!	!
147	!TTLVCC	!	!	! 5V	! P	!	!	!	!	!	!	!
148	!TTLVCC	!	!	! 5V	! P	!	!	!	!	!	!	!

TECHNOLOGY CHECK

• TECHNOLOGY - Validates that all components used are consistent with the specified product type and I/O mode as specified by the circuit user-assigned parameters of CIRCUIT_FAMILY and TECHNOLOGY. These parameters are assigned when the user selects a chip macro.

• ECL 10K/100K - Q3500 Series only: Ensures that a design does not mix ECL 10K with ECL 100K, or STD REF ECL with +5V REF ECL.

INTRODUCTION

The technology ERC will check the design for component family and technology mismatches. It is illegal to mix component families and technologies on any circuit.

Each macro in the circuit is checked to see if it is a valid component for the given circuit parameters as defined by the chip macro. This includes the ECL technology.

NO array libraries may be mixed on a circuit, i.e., macros from more than one array series library are not alllowed.

Use of Q14000B/Q6000B I/O on a Q9100B/Q2100B circuit will be detected in the Population Error Check.

The technology ERC also ensures that STD REF ECL 10K and STD REF ECL 100K are not mixed with +5V REF ECL 10K or +5V REF ECL 100K. This part of the check applies to the different Logic Array Series as follows:

Q3500 Series arrays - The Q3500 Series arrays currently do not allow both ECL 10K and ECL 100K to be on the same array. The Q3500 Series array macro library has no distinction for reference voltage for input or output macros.
Checks:

- no ECL 10K I/O macro is mixed with any ECL 100K I/O macro in any one array design.
  (only IEnn and OEnn or OKnn and IEnn are allowed, OEnn and OKnn cannot be mixed)

Q5000 Series arrays - The Q5000 Series arrays allow both ECL 10K and ECL 100K to be on the same array. The Q5000 Series array macro libraries have no distinction for reference voltage for input or output macros. The assumption is made that the chip macro selected will define the ECL type to be assigned to the input macros. The default ECL power supplies are for the input macro ECL type.

Q14000 Series arrays - The Q14000 Series arrays allow both ECL 10K and ECL 100K to be on the same array. The Q14000 Series array macro libraries have no distinction for reference voltage for input or output macros. The assumption is made that the chip macro selected will define the ECL type to be assigned to the input macros. The default ECL power supplies are for the input macro ECL type.

Q20000 Series arrays - The Q20000 Series arrays allow both ECL 10K and ECL 100K to be on the same array. The Q20000 Series array macro libraries have no distinction for reference voltage for input or output macros. The assumption is made that the chip macro selected will define the ECL type to be assigned to the input macros. The default ECL power supplies are for the input macro ECL type.

There are no chip macros of the type "TTL", "TTL10K" or "TTL100K" for the Q20000 Series. There are no +5V REF ECL or +5V REF ECL/TTL mix circuits and no 100% TTL circuits. There are dual power supply "DECL10K" and "DECL100K" chip macros for 100% ECL circuits with two power supplies.

ERROR REPORTS

A description of errors follows:

ERROR325: COMPONENT HAS NO SIGNAL TYPE

Informs the user that the macro has no technology parameter associated with it. Contact AMCC if this error occurs.

ERROR326: TECHNOLOGY (I/O MODE) PARAMETER NOT FOUND

Informs the user that the chip macro does not have a technology. Consult AMCC if this error occurs.

ERROR327: INVALID CIRCUIT TECHNOLOGY

Informs the user that the circuit technology is not an AMCC approved technology. On all EWS, this can happen if the AGIF netlist is hand edited by the designer.

ERROR328: BOTH ECL 10K AND ECL 100K MACROS HAVE BEEN USED

Only one ECL type may be used in any given circuit for the Q3500 Series arrays. (Does not apply to Q20000, Q14000 or Q5000 Series arrays.) Both ECL 10K and ECL 100K macros have been used.

ERROR333: THIS MACRO CAN NOT BE USED IN THIS CIRCUIT TECHNOLOGY

Informs the user that an improper mix of technology types has occurred such as TTLMIX in a TTL circuit, ECL in a TTL circuit, TTL in an ECL/TTL dual power supply circuit, +5V REF ECL in a STD REF ECL circuit, TTL in a 100% ECL circuit, etc.

ERROR334: ARRAY LIBRARY DOES NOT MATCH CIRCUIT FAMILY

Followed by a listing of the incorrect macro, this error message indicates that a macro from another array series has appeared on the schematic. Replaced by population check.

INFORMATION ONLY:

Number of errors found = n

If errors are found, this statement will inform the designer. There is a limit of 25 on the number of messages printed.

No errors have been found

The circuit has no errors detected by this part of the MacroMatrix software.

```
************************************************************
*          CIRCUIT TECHNOLOGY ERC                          *
*          REVISION 1.1                                    *
************************************************************


   Path Name /USER/CLASS/ERRORS
   Product Name PRODUCT_NAME
   Circuit family Q3500
   Circuit technology E
   Date 9 JUN 1986
   Time 13:3
   Product Grade PRODUCT_GRADE


ERROR333: THIS MACRO CAN NOT BE USED IN THIS CIRCUIT
          TECHNOLOGY
          Component may not be used on the
                    following types of circuits: E M
          Component=0C10 Macro=IT01 Pin=PI
          Signal=XSIG31
          Page= 1
ERROR328: BOTH ECL 10K AND ECL 100K MACROS HAVE BEEN USED
          COMPONENT= ECL10    MACRO=OE73   ECL_LEVEL=10K   PAGE=4
          COMPONENT= ECL100   MACRO=OK73   ECL_LEVEL=100K  PAGE=4
          COMPONENT= L0001    MACRO=OE82   ECL_LEVEL=10K   PAGE=7
                    :
   Number of errors found = 11
```

```
**************************************************************
*          CIRCUIT TECHNOLOGY ERC                            *
*          VERSION  2.8Ø                                     *
**************************************************************

   Path Name /USER/CLASS/Q532REG
   Product Name Q5REG32
   Circuit family Q5ØØØ
   Circuit technology M
   Date  7 OCT 1988
   Time 1Ø:39
   Product Grade MIL


   No errors found.
```

VALIDNAMES CHECK

• VALIDNAMES - Checks some of the more blatant naming errors such as duplicate names, names over 8 characters, special characters in names or reserved first-letter. Checks all user-assigned (occurrence) names.

INTRODUCTION

The validnames ERC ensures that user-defined signal and instance names do not conflict with the AMCC naming conventions. This ERC will also flag potential problems with the design interface to AMCC internal software.

Depending on the EWS, some default names ARE longer than eight characters. The ERC program produces a cross-reference report of renamed macros and signals.

It is not a good design practice to use pin names or names that would be easily confused with other notations when selecting a user-defined name. It is a good practice to keep a name meaningful (representative of the function or module).

- All external signals require a name.
- All page-to-page signals require a name.
- All critical path nets require a name.
- All signals connected to the control of a 3-state output (or bidirectional I/O macro) require a name.
- All macros in a flat design must be named.
- Macros in a multi-level (each block unique) structure must be named. (Note: DAISY users call this hierarchy.)
- Macros in the definition pages of a multiple-referenced block must be handled following the EWS system's conventions (Volume II, Section 7). Macros in these instances are renamed by the AMCC netlister. (Note: DAISY users call this nested.)

Different EWS systems have different page-handling and naming conventions. Refer to the appropriate AMCC EWS MacroMatrix Installation and Operations document, Volume II, Section 7, and to AMCC EWS Schematic Rules and Conventions in Volume II, Section 3, of the appropriate Design Manual.

DESIGN METHODOLOGY NOTE:

If all nets in a critical path start with the same letters they will sort together in the Front- and Back-Annotation delay files and this will simplify timing analysis. AMCC recommends this approach.

Checks that are made by the VALIDNAME ERC are as follows:

- Duplicate names - This includes component and signal names as well as AMCC macro names. All macro names, instance names, and net names must be unique.

- Non-alphanumeric characters - A name may begin with and may contain letters or numerals. It may not contain or begin with a special character.

- Name length - Insures that no user defined signal name is greater than 8 characters long and that no user defined instance name is greater than 6 characters long. DESIGN NOTE: For placement, MSI macro names of 4 characters or less are easier to work with but there is no special restriction of MSI instance names.

- Reserved words - Ensures that no user-defined name contains a reserved word:

GRND	INPUT	VDD
MODE	OUTPUT	VSS
GND	ZTERMS	

ERROR REPORTS

A description of errors follows. All error messages except 170 give the component name and pin name information in sufficient detail to allow location within the schematic set.

ERROR170: Duplicate component names in the AGIF file.
Component=.....

Informs the user that the design has duplicate user-defined names on two or more objects. NOTE: THIS IS CAUGHT DURING THE CIRCUIT.SDI GENERATION. THE CIRCUIT.SDI FILE WILL NOT LOAD AND AMCCERC.LST WILL SHOW ERROR170 AND ERROR3. The page number for the duplicate names can be found by searching the CIRCUIT.SDI file. Remove all duplicate names and regenerate thru CIRCUIT.SDI.

ERROR603: USER-DEFINED SIGNAL NAME EXCEEDS 8 CHARACTERS

Informs the user that a user-defined signal name exceeds the 8 character limit. There will be problems with other software packages.

ERROR604: USER-DEFINED INSTANCE NAME EXCEEDS 6 CHARACTERS

Informs the user that a user-defined instance name (a user-defined macro name, or name given to a block, cell, or other non-signal structure) exceeds the 6 character limit. There will be problems with other software packages.

ERROR605: USER-DEFINED NAME EQUALS A RESERVED WORD

Informs the user that a user-defined name duplicates a reserved word. There will be problems with other software packages.

GRND	INPUT	VDD
MODE	OUTPUT	VSS
GND	ZTERM	

ERROR609: USER-DEFINED NAME CONTAINS NON-ALPHANUMERIC CHARACTERS

A name must begin with a letter or a numeral and contain only letters and numerals. No spaces or special characters are allowed. Different EWS systems allow different special characters but the other software that a netlist must interface with does not.

INFORMATION ONLY:

Number of errors found = n

If errors are found, this statement will inform the designer. There is a limit of 25 on the number of messages printed.

No errors have been found

The circuit has no errors detected by this part of the MacroMatrix software.

```
*************************************************************
*          VALID NAME CHECK ERC                             *
*          Revision 2.0                                     *
*************************************************************

   Path Name /USER/CLASS/ERRORS
   Product Name PRODUCT_NAME
   Circuit family Q3500
   Circuit technology E
   Date 9 JUN 1986
   Time 13:3
   Product Grade PRODUCT_GRADE


ERROR604: USER DEFINED INSTANCE NAME EXCEEDS 6 CHARACTERS
          Component=WIREORX Macro=WIREOR3
          Page= 1

   Number of errors found = 1
```

```
*************************************************************
*          VALID NAME CHECK ERC                             *
*          VERSION  2.7Ø                                    *
*************************************************************

   Path Name /USER/CLASS/Q532REG
   Product Name Q5REG32
   Circuit family Q5ØØØ
   Circuit technology M
   Date  7 OCT 1988
   Time 1Ø:39
   Product Grade MIL


   No errors found.
```

RENAMED SIGNAL/COMPONENT CROSS-REFERENCE REPORT

INTRODUCTION

The purpose of the cross-reference report, **AMCCXREF.LST**, is to provide a mapping between the name on the schematic, either macro instance name or a signal name, and the name as it appears in the AGIF netlist. This cross-reference may be particularly useful when debugging ERC errors in a hierarchical schematic.

This report lists the signal or instance names that have been renamed, if any, showing both the original and the new name. A signal or component can be named by the EWS system itself, by the netlister, or by the designer during schematic capture.

The AMCC netlister places **AMCCXREF.LST** in the /ERC subdirectory.

type amccxref.lst

Signal Cross-Reference

NETLIST SIGNAL NAME	ORIGINAL SIGNAL NAME	PAGE NUMBER
0P34	XSIG34	1

Component Cross-Reference

NETLIST COMPONENT NAME	ORIGINAL COMPONENT NAME	PAGE NUMBER
XC0007	XCMP22	1

PrePlacement Component Cross-Reference

PAGE NUMBER	ORIGINAL COMPONENT NAME	NETLIST COMPONENT NAME
1	XCMP22	XC0007

REPORT SUMMARY

At the end of the AMCCERC.LST report a summary of all errors and warnings is printed to provide a quick overview of the status of the design. Any errors must be removed or waived via an approved pre-approval request prior to submission.

```
*************************************************************
*                                                           *
*          ERC report summary                               *
*          VERSION  3.5Ø                                    *
*                                                           *
*************************************************************
```

BAD

```
Path Name /USER/CLASS/QUICK
Product Name PRODUCT_NAME
Circuit family Q5ØØØ
Circuit technology M
Date 18 OCT 1988
Time 16:2Ø
Product Grade PRODUCT_GRADE
```

ERC NAME	! ERRORS	! WARNINGS
Simultaneously Switching Output	Ø	Ø
Population	34	Ø
Valid Name Check	Ø	Ø
Pin Class	2	Ø
Fan-Out	51	Ø
Internal Pin Count	1	Ø
Pin hookup and Unused pins	2156	Ø
Bipolar Macro Occurrence and Power	1	Ø
Circuit Technology	11	Ø

```
*************************************************************
*                                                           *
*          ERC report summary                               *
*          VERSION  3.4Ø                                    *
*                                                           *
*************************************************************
```

GOOD

```
Path Name /USER/CLASS/MUX16
Product Name MUX16
Circuit family Q5ØØØ
Circuit technology P
Date 2Ø SEP 1988
Time  9:58
Product Grade MIL
```

ERC NAME	! ERRORS	! WARNINGS
Simultaneously Switching Output	Ø	Ø
Population	Ø	Ø
Valid Name Check	Ø	Ø
Pin Class	Ø	Ø
Fan-Out	Ø	Ø
Internal Pin Count	Ø	Ø
Pin hookup and Unused pins	Ø	Ø
Bipolar Macro Occurrence and Power	Ø	Ø
Circuit Technology	Ø	Ø

```
**********************************************************
*          ERC report summary                            *
*          VERSION  3.4Ø                                 *
**********************************************************
```

Path Name /USER/CLASS/Q532REG
Product Name Q5REG32
Circuit family Q5ØØØ
Circuit technology M
Date 7 OCT 1988
Time 1Ø:39
Product Grade MIL

Try to Correct

ERC NAME	! ERRORS	! WARNINGS
Simultaneously Switching Output	Ø	2
Population	Ø	Ø
Valid Name Check	Ø	Ø
Pin Class	Ø	Ø
Fan-Out	Ø	Ø
Internal Pin Count	Ø	Ø
Pin hookup and Unused pins	Ø	Ø
Bipolar Macro Occurrence and Power	Ø	Ø
Circuit Technology	Ø	Ø

Each AMCCERC check has a default error limit of 25. All errors will be detected and a total printed for each check but only the first 25 will be printed.

When it is necessary to raise this limit, i.e., during initial debug of a large circuit, the error limit may be raised as follows:

1. Create a text file named PARAMS.ERC

2. The file should contain one line of text setting the limit:

   LIMIT nnn
   where nnn is an integer.

AMCC does not recommend the use of limits above 100 since the limit applies to each check made by the AMCCERC software.

The AMCCERC software can be run on a partial circuit. The DAISY shell script RUN_AMCC will abort on error so the individual steps RUN_DD, RUN_AGIF and RUN_ERC will need to be called. MENTOR and VALID will run the script run_amcc on a partial circuit.

Running on a partial circuit allows consistently repeated errors to be spotted early before they become bad habits. It also makes the task of final debug easier by clearing away errors as they are discovered.