Q5000 Bipolar Array Series (804)

Section 6:

Macro Library

6-1-1 Q5000 TTL MACROS

- FOR TTL INPUT/OUTPUT - +5V POWER SUPPLY CIRCUIT

Q5000 TTL INPUT

page #	name	OPTIONS	cells	description
6-1-3	IT11	S,H	1	INPUT WITH BUFFER, COMPL. OUTPUTS

Q5000 TTL OUTPUT

page #	name	OPTIONS	cells	description
6-1-4	OT30	S,L,H	1	OUTPUT, 3-INPUT OR BUFFER

6-2-1 Q5000 TTLMIX MACROS

- FOR TTL INPUT/OUTPUT IN ECL/TTL MIXED CIRCUITS WITH TWO POWER SUPPLIES (-5.2V, +5V; ECL 10K); (-4.5V, +5V; ECL 100K)

Q5000 TTLMIX INPUT

page #	name	OPTIONS	cells	description
6-2-3	IT40	S	1	INPUT WITH OR/NOR BUFFER
6-2-4	IT45	S	1	UNBUFFERED INPUT
6-2-5	IT58	S,H	1	3-STATE ENABLE-DRIVER (EXTERNAL)

Q5000 TTLMIX OUTPUT

page #	name	OPTIONS	cells	description
6-2-6	OT57	S,L,H	1	3-STATE ENABLE DRIVER (INTERNAL)
6-2-7	OT61	S,L,H	1	OUTPUT, 2-INPUT OR BUFFER
6-2-8	OT63	S,L,H	1	3-STATE OUTPUT - OR GATE

Q5000 TTLMIX BIDIRECTIONAL

page #	name	OPTIONS	cells	description
6-2-9	UT66	S,L,H	1	BIDIR I/O, 2-INPUT OR

6-3-1 Q5000 ECL MACROS

• FOR ECL INPUT/OUTPUT IN ECL, +5V REF ECL,
MIXED ECL/TTL AND MIXED +5V REF ECL/TTL CIRCUITS

Q5000 ECL INPUT

page #		name	OPTIONS	cells	description
6-3-3		IE23D	S	1	BUFFER, SUPER-DRIVER
6-3-4	*	IE25	S	2	DIFFERENTIAL INPUT
6-3-5		IE80	S	1	INPUT WITH OR/NOR BUFFER
6-3-6		IE85	S	1	UNBUFF. INPUT COMPENSATOR
6-3-7		IE86	S	1	PROGRAMMABLE THERMAL DIODE
6-3-8		IE88D	D	1	DIFF. INPUT, COMPL. OUT
6-3-10		IE89D	D	1	DIFF. INPUT, COMPL. OUT
6-3-12		IE90	S	1	DIFF. INPUT, BUF, COMPL.
6-3-13		IE93	S	1	BUFFER, COMPL. OUTPUTS
6-3-14	*	IE99V	V	2	DIFFERENTIAL INPUT - FAST

Q5000 ECL OUTPUT - Oxnn - BUFFERED INTERNALLY

page #		name	OPTIONS	cells	description
OEnn IS FOR ECL 10K, -5.2V OR +5V REF, 50ohm					
OKnn IS FOR ECL 100K, -4.5V OR +5V REF, 50ohm					
6-3-15		OE10	S	2	DIFFERENTIAL ECL OUTPUT
6-3-16		OE13	S	1	2-INPUT OR
6-3-17	*	Ox77	S	1	2:1 MUX (YIN)
6-3-19	*	Ox80	S	1	3-INPUT OR/NOR (YI)
6-3-20	*	Ox81	S	1	3-INPUT OR/NOR (YIN)
6-3-21		OE85	S	1	2-INPUT EXOR/EXNOR (YI)
6-3-22		OE87	S	1	THERMAL DIODE TERMINATION
6-3-23	*	OE97V	V	2	DIFF. ECL OUTPUT - FAST

Q5000 ECL BIDIR

page #	name	OPTIONS	cells	description
6-3-24	UE50	S	1	BIDIR I/O WITH BUFFER

SAMPLE I/O INTERCONNECTIONS:

6-4-1 Q5000 SERIES INTERNAL LOGIC MACROS

ADDERS:

COMPARATORS

CARRY-PROPAGATE GENERATORS

COUNTER MACROS

DECODER MACROS

EXOR/EXNOR-NETWORK MACROS

page #		name	OPTIONS	cells	description
6-4-30		EX00	S,L,H	0.5	3-INPUT OR-EXOR/EXNOR
6-4-32		EX03	S,L,H	1	5-INPUT OR-EXOR
6-4-33	*	EX04	S,L,H	0.5	3-INPUT EXOR/EXNOR
6-4-34		EX20	S,L,H	1	TRIPLE 2-INPUT EXOR
6-4-35		EX24	S,L,H	0.5	4-INPUT EXOR
6-4-36		EX26	S,L,H	1	4-INPUT EXNOR
6-4-37	*	EX27	S,L,H	1	TRIPLE 2-INPUT EXOR
6-4-38	*	EX33	S,L,H	0.5	3-INPUT EXOR/EXNOR
6-4-39		EX50	S,L,H	0.5	2-TERM, 2-INPUT OR TO EXOR/EXNOR
6-4-40		EX58	S,L,H	0.5	DUAL 2-INPUT EXOR
6-4-41	*	EX59	S,L,H	0.5	DUAL 2-INPUT EXOR
6-4-42	*	EX59D	D	0.5	DRIVER 2-INPUT EXOR

FLIP/FLOPS

page #		name	OPTIONS	cells	description
6-4-43		FF13	S,L,H	1	D F/F, AR
6-4-44		FF15	S,L,H	1	D F/F, AR, Q, QN
6-4-45		FF17	S,L,H	1	D F/F, AS, Q, QN
6-4-46		FF18	S,L	0.5	HIGH DENSITY F/F, Y
6-4-47		FF19	S,L	0.5	HIGH DENSITY F/F, YN
6-4-48		FF32	S,L,H	1	2:1 MUX D F/F, AR
6-4-50		FF34	S,L,H	1	D F/F, AS, AR, Q, QN
6-4-51	*	FF35	S,L,H	1	D F/F, AS, AR, Q, QN
6-4-52		FF50	S,L,H	1	3:1 MUX D F/F
6-4-54		FF53	S,L,H	1	3:1 MUX D F/F, AR
6-4-56	*	FF70	S	1	METASTABLE D F/F RISING
6-4-57	*	FF71	S	1	METASTABLE D F/F FALLING
6-4-58	*	FF72	S	1	METASTABLE D F/F RISING,AR
6-4-59	*	FFF05V	V	2	MSI D F/F, AR - FAST

GATES - BASIC LOGIC FUNCTIONS

page #	name	OPTIONS	cells	description
6-4-61	GT00	S,L,H	0.5	4-INPUT OR/NOR
6-4-62	GT01	S,L,H	1	6-4-INPUT OR/NOR
6-4-63	GT10	S,L,H	0.5	DUAL 2-INPUT NOR
6-4-64	GT11	S,L,H	0.5	DUAL 2-INPUT OR
6-4-65	GT12	S,L,H	0.5	2-INPUT NOR, 2-INPUT OR
6-4-66	GT13	S,L,H	0.5	3-INPUT, DUAL OUTPUT OR
6-4-67	GT14	S,L,H	0.5	3-INPUT, DUAL OUTPUT NOR
6-4-68	GT15	S,L,H	1	2-TERM 3-INPUT OR-AND/NAND

GATES - BASIC LOGIC (CONTINUED)

LATCHES

MULTIPLEXOR MACROS

page #	name	OPTIONS	cells	description
6-4-111	MX00	S,L,H	1	2:1 MUX, GTD SEL, CPL
6-4-112	MX01	S,L,H	1	2:1 MUX, GTD SEL, EN
6-4-113	MX03	S,L,H	1	2:1 MUX, GTD SEL, EN, YN
6-4-114 *	MX04	S,L,H	0.5	2:1 MUX, GTD SEL, CPL
6-4-116 *	MX04D	D	0.5	DRIVER MUX
6-4-118	MX07	S,L,H	1	TRIPLE 2:1 MUX, CMN SEL
6-4-120	MX13	S,L,H	0.5	2:1 MUX
6-4-121 *	MX17V	V	1	2:1 MUX - FAST
6-4-123	MX21	S,L,H	1	4:1 MUX
6-4-124	MX22	S,L,H	1	4:1 MUX WITH LOW ENABLE,Y
6-4-126 *	MX25	S,L,H	1	4:1 MUX
6-4-128 *	MX26	S,L,H	1	4:1 MUX; LOW ENABLE

REGISTER

page #	name	OPTIONS	cells	description
6-4-130	REG00	S,L,H	4.5	4-BIT MUX WITH D F/F

WIRE-OR COMPONENT MACROS

page #	name	cells	description
6-5-3	WIREOR2	0	2-INPUT WIRE OR
6-5-3	WIREOR3	0	3-INPUT WIRE OR
6-5-3	WIREOR4	0	4-INPUT WIRE-OR

EXTRA POWER-GROUND MACROS ON I/O CELL

page #	name	cells	description
6-5-4	ITPWR	1	EXTRA VCC - TTL OR TTLMIX
6-5-5	ITGND	1	EXTRA GROUND - TTL OR TTLMIX
6-5-6	IEVCC	1	EXTRA ECL VCC - ECL OR MIX

6-5-7 CHIP MACROS

CHIP MACROS USE NO CELLS

MACRO NAMING CONVENTION- Q5000

THE EXPANSION OF A MACRO NAME IS GIVEN BELOW:

```
aa[a]nnb
 :   : :
 :   : :
 :   : :
 :   : ---- POWER/FANOUT:  S - STANDARD      (9 LOADS)
 :   :                     L - LOW POWER     (4 LOADS)
 :   :                     H - HIGH SPEED    (9 LOADS)
 :   :                     V - VERY FAST (9 or + LOADS)
 :   :                     D - DRIVER      (15/25 LOADS)
 :   :                     (3-STATE DRIVERS - 8 LOADS)
 :   :
 :   ---------- CELL # (00-99)
 --------- CELL TYPE: TWO - THREE LETTERS
                      (THREE LETTERS FOR MSI MACROS)
```

KEY:

```
AD - ADDER
ADD - MSI ADDER
BB - MSI BUILDING BLOCK - AMCC USE ONLY
BI - ECL INPUT BUFFERED LOGIC
CPG - MSI CARRY LOOK-AHEAD GENERATOR
CMP - MSI COMPARATOR
CTR - MSI COUNTER                    ========================
DE - DECODER                          IE  ECL input
EX - EXOR                             OE  ECL 10K OUTPUT
FF - F/F                              OK  ECL 100K OUTPUT
FFF - MSI F/F                         UE  ECL 10K Bidirec.
GT - GENERAL GATES                    UK  ECL 100K Bidirec.
LA - LATCH                            IT  TTL INPUT
MX - MULTIPLEXOR, MUX                 OT  TTL OUTPUT
RAM - QM1600T RAM MACRO               UT  TTL Bidirec.
REG - MSI REGISTER                   ========================
```

FOR TTL I/O MACROS:
00-39 = 100% TTL; OR MIX IN A +5V ONLY CIRCUIT
40-99 = MIX IN A DUAL POWER SUPPLY CIRCUIT

FOR ECL I/O MACROS:
LETTER DESIGNATION FOR ECL 10K AND ECL 100K
ECL MACROS DO NOT VARY WITH I/O MODE

Section 6-1:

TTL Interface

AMCC Q5000 MACRO SUMMARY - TTL LIB (804)
FOR 100% TTL OR ECL/TTL MIXED MODE CIRCUITS;
SINGLE +5V POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

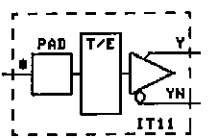
IT11 I/O cell TTL INPUT WITH BUFFER, COMPL. OUTPUTS

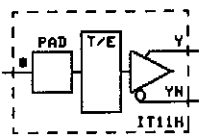
		S	L	H	
Tpd ++	PAD->Y	0.49		0.33	ns
--	PAD->Y	0.33		0.23	ns
Tpd +-	PAD->YN	0.26		0.22	ns
-+	PAD->YN	0.11		0.24	ns
ICC		1.13		1.35	mA I/O
FAN-OUT LOAD LIMIT:		9		9	loads
k-FACTOR	RISING	0.04		0.02	ns/LU
	FALLING	0.04		0.04	ns/LU

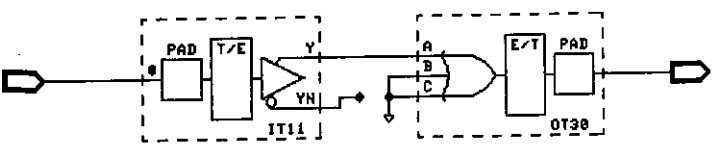
---

* INPUT PAD MUST BE TIED TO TOTEM-POLE TYPE TTL OUTPUTS OR TO A VOLTAGE WITH $V_H < V_{CC} - 0.5$

Y = PAD YN = $\overline{PAD}$







TTL I/O

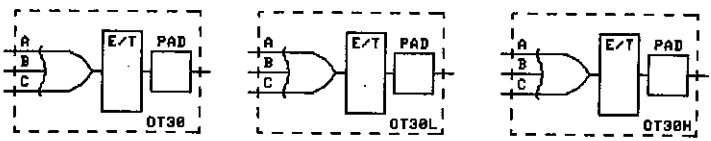
AMCC Q5000 MACRO SUMMARY - TTL LIB (804)
FOR 100% TTL OR ECL/TTL MIXED MODE CIRCUITS;
SINGLE +5V POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

OT30 I/O cell TTL OUTPUT WITH 3-INPUT OR BUFFER

	S	L	H	
Tpd (A,B,C->PAD				
++	4.21	4.23	4.13	ns
--	2.95	3.74	2.45	ns
ICC	2.75	2.30	4.01	mA I/O

A,B,C CAN BE TIED TO GROUND

PAD = A + B + C



Section 6-2:

TTLMIX Interface

AMCC Q5000 MACRO SUMMARY - TTL MIX (804)
FOR TTL I/O IN STD ECL/TTL MIXED MODE CIRCUITS
DUAL POWER SUPPLY: +5V AND -5.2V
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

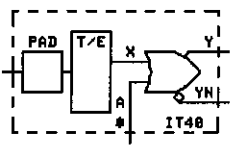
IT40 I/O cell TTL INPUT WITH OR/NOR BUFFER

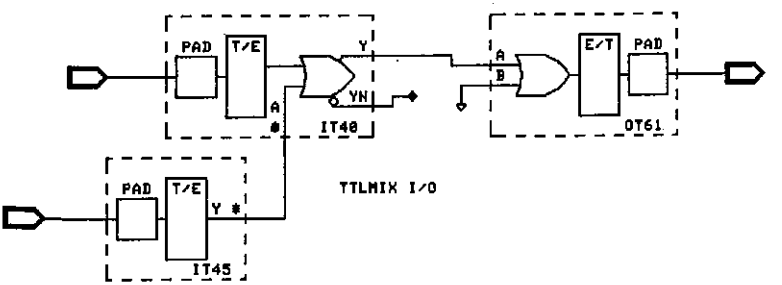
	S	L	H	
Tpd ++A->Y	0.86			ns
Tpd --A->Y	0.39			ns
Tpd ++PAD->Y	1.42			ns
Tpd --PAD->Y	0.78			ns
Tpd +-A->YN	0.56			ns
Tpd -+A->YN	0.63			ns
Tpd +-PAD->YN	1.12			ns
Tpd -+PAD->YN	1.02			ns
ICC	0.50			mA I/O
IEE	1.35			mA CORE
FAN-OUT LOAD LIMIT:	9			loads
k-FACTOR RISING	0.04			ns/LU
FALLING	0.04			ns/LU

---

* A FROM IT45 OR GROUND

$Y = PAD + A \qquad YN = \overline{PAD + A}$





AMCC Q5000 MACRO SUMMARY - TTL MIX (804)
FOR TTL I/O IN STD ECL/TTL MIXED MODE CIRCUITS
DUAL POWER SUPPLY: +5V AND -5.2V
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

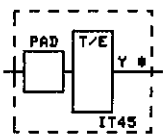
IT45 I/O cell TTL INPUT - UNBUFFERED

	S	L	H	
Tpd ++PAD->Y	0.56			ns
Tpd --PAD->Y	0.39			ns
ICC	0.27			mA CORE
FAN-OUT LOAD LIMIT:	1			loads
k-FACTOR RISING	0.04			ns/LU
FALLING	0.04			ns/LU

---

* Y TO IT40 A INPUT ONLY

Y = PAD



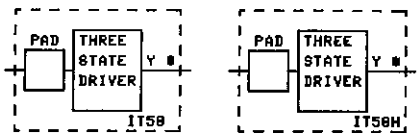
AMCC Q5000 MACRO SUMMARY - TTL MIX (804)
FOR TTL I/O IN STD ECL/TTL MIXED MODE CIRCUITS
DUAL POWER SUPPLY: +5V AND -5.2V
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

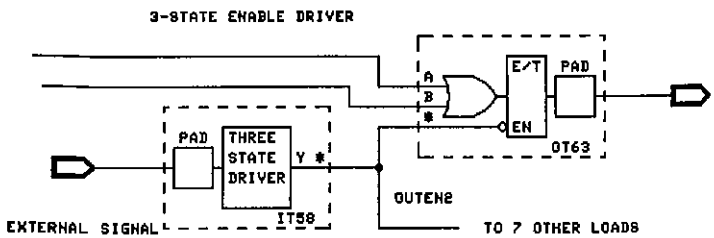
IT58 I/O cell TTL 3-STATE ENABLE-DRIVER (EXTERNAL)

		S	L	H	
Tpd ++PAD->Y		0.67		0.08	ns
Tpd --PAD->Y		0.11		0.02	ns
ICC		0.72		2.70	mA I/O
FAN-OUT LOAD LIMIT:		8		8	loads
k-FACTOR	RISING	0.04		0.02	ns/LU
	FALLING	0.04		0.04	ns/LU

---

* Y TO OUTPUT ENABLE ON TTLMIX 3-STATE OR TTLMIX BIDIRECTIONAL MACROS





AMCC Q5000 MACRO SUMMARY - TTL MIX (804)
FOR TTL I/O IN STD ECL/TTL MIXED MODE CIRCUITS
DUAL POWER SUPPLY: +5V AND -5.2V
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

OT57 I/O cell TTL 3-STATE ENABLE-DRIVER (INTERNAL)

		S	L	H	
Tpd ++A->Y		1.09	2.10	0.46	ns
Tpd --A->Y		1.64	1.64	2.01	ns
ICC HIGH		2.30	2.07	3.87	mA I/O
ICC LOW		1.67	0.99	2.88	mA I/O
IEE		0.23	0.23	0.23	mA CORE
FAN-OUT LOAD LIMIT:		8	8	8	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

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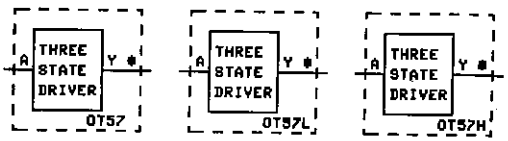
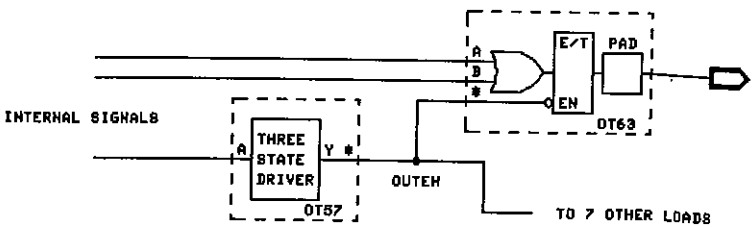
* Y TO OUTPUT ENABLE ON TTLMIX 3-STATE OR TTLMIX BIDIRECTIONAL MACROS
A CAN BE TIED TO GROUND

Y = A





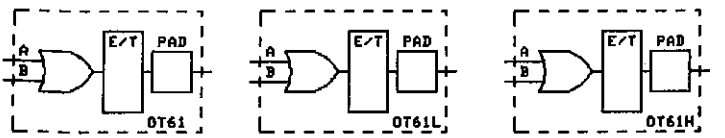
AMCC Q5000 MACRO SUMMARY - TTL MIX (804)
FOR TTL I/O IN STD ECL/TTL MIXED MODE CIRCUITS
DUAL POWER SUPPLY: +5V AND -5.2V
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

OT61 I/O cell TTL OUTPUT WITH 2-INPUT OR BUFFER

		S	L	H	
	(1 INPUT CHANGING)				
Tpd	++A,B->PAD	4.34	4.37	3.73	ns
	--A,B->PAD	2.51	3.41	1.97	ns
	(2 INPUTS CHANGING)				
	++	3.66	4.35	4.29	ns
	--	2.02	3.49	2.59	ns
ICC		2.70	2.25	4.14	mA I/O
IEE		0.23	0.15	0.34	mA CORE

A,B CAN BE TIED TO GROUND

PAD = A + B



AMCC Q5000 MACRO SUMMARY - TTL MIX (804)
FOR TTL I/O IN STD ECL/TTL MIXED MODE CIRCUITS
DUAL POWER SUPPLY: +5V AND -5.2V
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

OT63 I/O cell TTL 3-STATE OUTPUT, 2-INPUT OR, EN

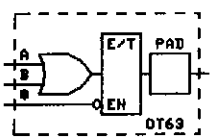
		S	L	H	
Tpd	++(A->PAD)	6.35	6.04	5.07	ns
	--(A->PAD)	2.12	3.06	1.90	ns
Tpd	++(B->PAD)	6.23	5.93	5.03	ns
	--(B->PAD)	2.12	3.07	1.91	ns
Tpd	++(A,B->PAD)	6.20	5.93	5.00	ns
Tpd	(EN->PAD)				
	A+B=0 ZL	4.31	5.31	3.30	ns
	LZ	3.89	4.80	2.92	ns
	A+B=1 ZH	5.21	6.52	4.39	ns
	HZ	1.24	0.80	1.56	ns
ICC		3.24	2.61	4.86	mA I/O
IEE		0.23	0.15	0.34	mA CORE

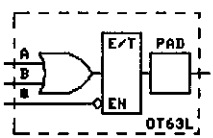
---

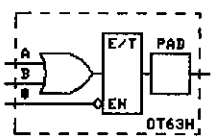
* EN FROM TTLMIX 3-STATE ENABLE DRIVER (INTERNAL OR EXTERNAL)
EN MUST BE DRIVEN BY A MACRO
SIGNAL NAME FOR ENABLE INPUT MUST APPEAR IN THE SIMULATION FORMAT
A,B CAN BE TIED TO GROUND

PAD = (A+B).$\overline{EN}$ (FOR EN LOW);
PAD = HIGH-Z (FOR EN HIGH)

EN	A+B	PAD
0	1	1
0	0	0
1	X	HIGH-Z







AMCC Q5000 MACRO SUMMARY - TTL MIX (804)
FOR TTL I/O IN STD ECL/TTL MIXED MODE CIRCUITS
DUAL POWER SUPPLY: +5V AND -5.2V
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

UT66 I/O cell TTL BIDIRECTIONAL I/O, 2-INPUT OR BUFFER

		S	L	H		
(1 INPUT CHANGING)						
Tpd	++A->PAD	6.01	5.74	5.34	ns	
	--A->PAD	2.38	3.01	1.98	ns	
	++B->PAD	5.96	5.66	5.28	ns	
	--B->PAD	2.37	3.01	1.96	ns	
(2 INPUTS CHANGING)						
Tpd	++A,B->PAD	5.95	5.65	5.27	ns	
	--A,B->PAD	2.43	3.07	2.01	ns	
	++PAD->Y	1.08	1.08	1.08	ns	
	--PAD->Y	1.11	1.11	1.11	ns	
	+-PAD->YN	1.03	1.03	1.03	ns	
	-+PAD->YN	1.51	1.51	1.51	ns	
Tpd	EN->PAD					
	A+B=0 ZL	4.66	4.76	3.37	ns	
	LZ	4.09	4.52	2.94	ns	
	A+B=1 ZH	6.38	6.15	5.12	ns	
	HZ	1.32	1.02	1.59	ns	
ICC		3.74	3.11	5.36	mA	I/O
IEE		1.67	1.67	1.67	mA	CORE
FAN-OUT LOAD LIMIT:		9	4	9	loads	
k-FACTOR	RISING	0.04	0.04	0.04	ns/LU	**
	FALLING	0.04	0.04	0.04	ns/LU	**

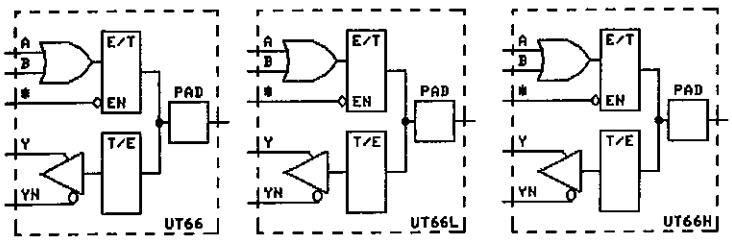
---

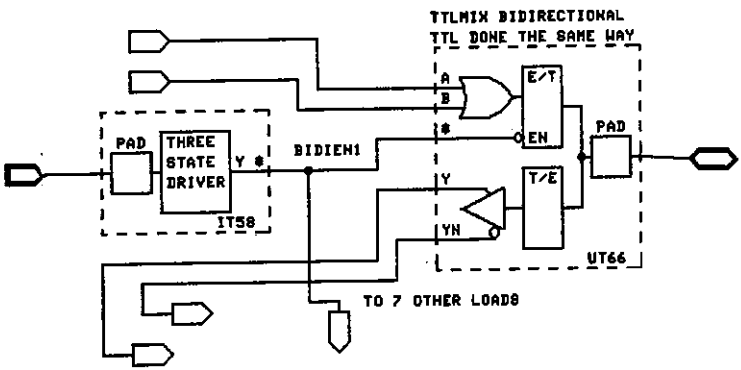
* EN FROM 3-STATE ENABLE DRIVER
  EN MUST BE DRIVEN BY A MACRO
  SIGNAL NAME FOR ENABLE INPUT MUST APPEAR IN
  THE SIMULATION FORMAT
  A,B CAN BE TIED TO GROUND
** The input buffer is always an "S" option hence the constant k-factor

AMCC Q5000 MACRO SUMMARY - TTL MIX (804)
FOR TTL I/O IN STD ECL/TTL MIXED MODE CIRCUITS
DUAL POWER SUPPLY: +5V AND -5.2V
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

UT66 I/O cell TTL BIDIRECTIONAL I/O, 2-INPUT OR BUFFER

EN	A	B	PAD	Y	YN	
0	0	0	0	0	1	OUTPUT
0	X	1	1	1	0	OUTPUT
0	1	X	1	1	0	OUTPUT
1	X	X	1	1	0	INPUT
1	X	X	0	0	1	INPUT





Section 6-3:

ECL Interface

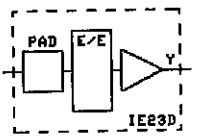
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

IE23D I/O cell ECL BUFFERED INPUT, SUPER-DRIVER

		DRIVER	
Tpd ++	PAD->Y	0.28	ns
--	PAD->Y	0.22	ns
IEE		5.20	mA
FAN-OUT LOAD LIMIT:		25	loads
k-FACTOR	RISING	0.01	ns/LU
	FALLING	0.01	ns/LU

OUTPUT CANNOT BE WIRE-ORED
FAN-OUT LOAD LIMIT IS NOT DERATED

Y = PAD



FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

IE25 2 I/O cells DIFFERENTIAL ECL BUFFERED INPUT

	S	L	H	
Tpd A,AN->Y,YN	0.37			ns
IEE	1.35			mA
FAN-OUT LOAD LIMIT:	9			loads
k-FACTOR RISING	0.040			ns/LU
FALLING	0.040			ns/LU
MAXIMUM FREQUENCY OF OPERATION (fMAX)	360			MHz

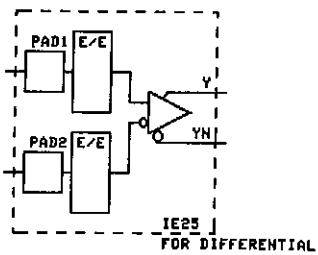
---

* BOTH INPUTS MUST BE USED

Note: Use dual-cell macros such as IE25 for high-speed ECL input up to 360MHz. Use V macros for speeds up to 600MHz.

PAD1 = A PAD2 = AN

PAD1 A	PAD2 AN	Y	YN
0	0	X	X
0	1	0	1
1	0	1	0
1	1	X	X



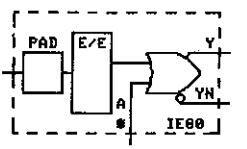
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

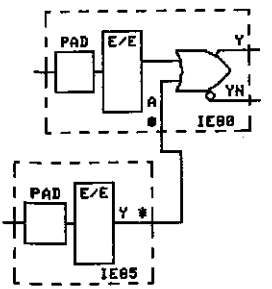
IE80 I/O cell ECL INPUT WITH OR/NOR BUFFER

	S	L	H	
Tpd ++A->Y	0.40			ns
--A->Y	0.31			ns
+-A->YN	0.31			ns
-+A->YN	0.66			ns
++PAD->Y	0.45			ns
--PAD->Y	0.36			ns
+-PAD->YN	0.36			ns
-+PAD->YN	0.71			ns
IEE	1.35			mA
FAN-OUT LOAD LIMIT:	9			loads
k-FACTOR RISING	0.040			ns/LU
FALLING	0.040			ns/LU

* A FROM UNBUFFERED ECL INPUT OR CAN BE TIED TO GROUND

$Y = PAD + A$ $YN = \overline{PAD + A}$





SIMPLE LOGIC PAIR

FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

IE85	I/O cell	ECL INPUT COMPENSATOR			
		S	L	H	
Tpd PAD->Y		0.05			ns
IEE		0.00			mA
FAN-OUT LOAD LIMIT:		8			loads
k-FACTOR	RISING	0.0			ns/LU
	FALLING	0.0			ns/LU

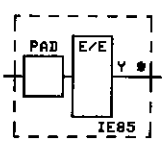
* Y TO BUFFERED-LOGIC MACROS; BUFFERED INPUT MACROS
  Y FAN-OUT LOAD IS NOT DERATED

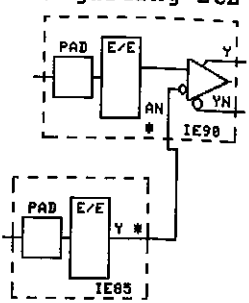
Y = PAD

NOTE: IE85 contains a series resistor between the pad and the transistor base connection of the macro used in a differential pair while the pairing macro does not contain this resistor. Therefore, for high speed applications, it may be necessary to skew the inputs to obtain optimum performance.

Macros IE88D-IE89D are balanced and should be used as a differential pair for high-speed applications. High-speed is defined as anything over 100MHz. THE maximum frequency for the pair is 180MHz with placement considerations. Use dual-cell differentials such as IE25 for speeds up to 360MHz and the V macros such as IE99V for speeds up to 600MHz (Commercial).

Any differential input pair will require external signal adjustment to account for package skew, etc. Refer to the Design Methodology section for rules regarding ECL differential I/O.





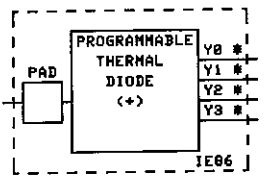
DIFFERENTIAL PAIR

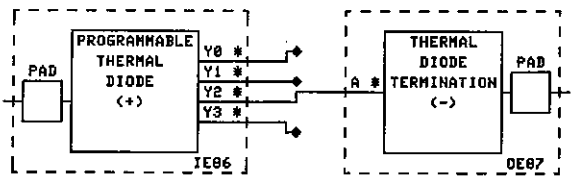
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

IE86 I/O cell PROGRAMMABLE THERMAL DIODE

		S	L	H	
Tpd PAD->Y		0.10			ns
IEE		0.00			mA
FAN-OUT LOAD LIMIT:		8			loads
k-FACTOR	RISING	0.04			ns/LU
	FALLING	0.04			ns/LU

MUST BE USED WITH OE87





THERMAL DIODE

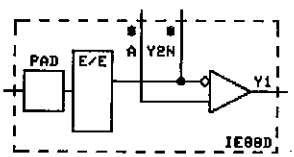
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

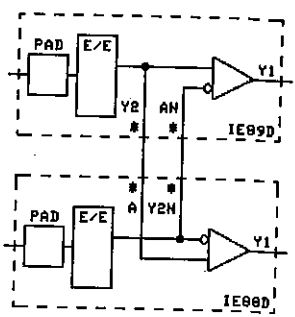
IE88D I/O cell ECL DIFFERENTIAL SUPER DRIVER

		DRIVER	
Tpd	PAD->Y2N	0.05	ns
Tpd -+	PAD->Y1	0.18	ns
+-	PAD->Y1	0.15	ns
Tpd ++	A->Y1	0.13	ns
--	A->Y1	0.10	ns
IEE		4.91	mA
FAN-OUT LOAD LIMIT:	Y1	25	loads
	Y2N	7	loads
k-FACTOR RISING	Y2N	0.00	ns/LU
FALLING	Y2N	0.00	ns/LU
RISING	Y1	0.01	ns/LU
FALLING	Y1	0.01	ns/LU
MAXIMUM FREQUENCY OF OPERATION (fMAX)		180	MHz

---

* A FROM UNBUFFERED ECL INPUT
A CANNOT BE GROUNDED
IE88D AND COMPANION MACRO MUST BE ADJACENT
Y1 TO BUFFERED LOGIC MACROS, BUFFERED INPUT MACROS
Y1,Y2N - FAN-OUT LOAD LIMIT IS NOT DERATED
OUTPUT CANNOT BE WIRE-ORED





DIFFERENTIAL PAIR

FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

IE88D I/O cell ECL DIFFERENTIAL SUPER DRIVER

Note: Use dual-cell macros such as IE25 for high-speed ECL input up to 360MHz. Use V macros for speeds up to 600MHz.

PAD	A	Y1	Y2N
0	0	ILLEGAL (UNKNOWN)	0
0	1	1	0
1	0	0	1
1	1	ILLEGAL (UNKNOWN)	1

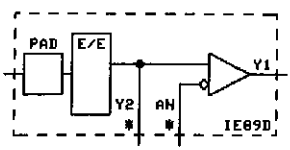
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

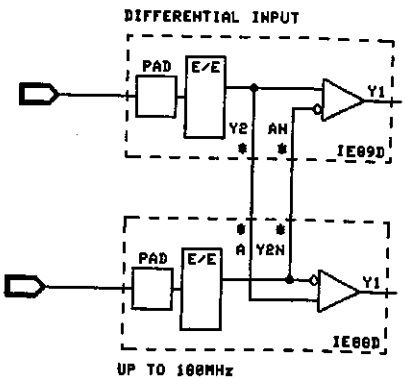
IE89D I/O cell ECL DIFFERENTIAL SUPER DRIVER

		DRIVER	
Tpd	PAD->Y2	0.05	ns
Tpd ++	PAD->Y1	0.18	ns
--	PAD->Y1	0.14	ns
Tpd -+	AN->Y1	0.13	ns
+-	AN->Y1	0.09	ns
IEE		4.91	mA
FAN-OUT LOAD LIMIT:	Y1	25	loads
	Y2	7	loads
k-FACTOR RISING	Y2	0.00	ns/LU
FALLING	Y2	0.00	ns/LU
RISING	Y1	0.01	ns/LU
FALLING	Y1	0.01	ns/LU
MAXIMUM FREQUENCY OF OPERATION (fMAX)		180	MHz

---

* AN FROM UNBUFFERED ECL INPUT
AN CANNOT BE GROUNDED
IE89D AND COMPANION MACRO MUST BE ADJACENT
Y2 TO BUFFERED LOGIC MACROS, BUFFERED INPUT MACROS
Y2,Y1 - FAN-OUT LOAD LIMIT IS NOT DERATED



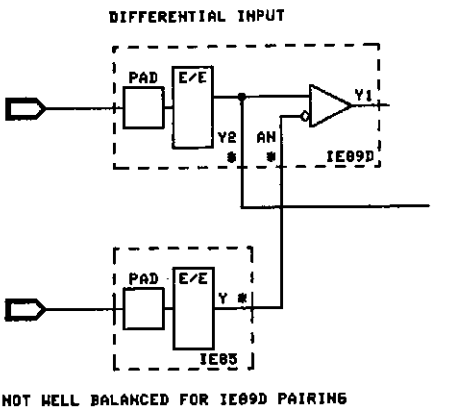


FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

IE89D I/O cell ECL DIFFERENTIAL SUPER DRIVER

Note: Use dual-cell macros such as IE25 for high-speed ECL input up to 360MHz. Use V macros for speeds up to 600MHz.

PAD	AN	Y1	Y2
0	0	ILLEGAL (UNKNOWN)	0
0	1	0	0
1	0	1	1
1	1	ILLEGAL (UNKNOWN)	1



FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

IE90 I/O cell ECL DIFF. INPUT, COMPL. OUTPUTS

	S	L	H	
Tpd ++ PAD->Y	0.22			ns
-- PAD->Y	0.23			ns
Tpd +- PAD->YN	0.23			ns
-+ PAD->YN	0.22			ns
Tpd +- AN->Y	0.18			ns
-+ AN->Y	0.17			ns
Tpd ++ AN->YN	0.17			ns
-- AN->YN	0.18			ns
IEE	1.35			mA
FAN-OUT LOAD LIMIT:	9			loads
k-FACTOR RISING	0.04			ns/LU
FALLING	0.04			ns/LU
MAXIMUM FREQUENCY OF OPERATION (fMAX)	180			MHz

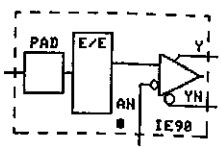
---

* AN FROM UNBUFFERED ECL INPUT
(MUST BE DRIVEN DIFFERENTIALLY)
AN CANNOT BE GROUNDED
IE90 AND COMPANION MACRO SHOULD BE ADJACENT

Note: Use dual-cell macros such as IE25 for high-speed ECL input up to 360MHz. Use V macros for speeds up to 600MHz.

Y = AN.PAD YN = $\overline{AN.PAD}$

PAD	AN	Y	YN
0	0	ILLEGAL	(UNKNOWN)
0	1	0	1
1	0	1	0
1	1	ILLEGAL	(UNKNOWN)

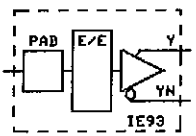


FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

IE93 I/O cell ECL BUFFERED INPUT, COMPL. OUTPUTS

		S	L	H	
Tpd ++	PAD->Y	0.36			ns
--	PAD->Y	0.24			ns
Tpd +-	PAD->YN	0.33			ns
-+	PAD->YN	0.24			ns
IEE		1.35			mA
FAN-OUT LOAD LIMIT:		9			loads
k-FACTOR	RISING	0.040			ns/LU
	FALLING	0.040			ns/LU

Y = PAD YN = $\overline{PAD}$



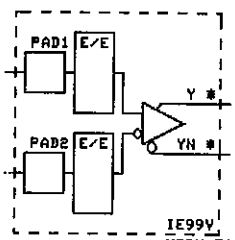
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

IE99V 2 I/O CELLS VERY HI-SPEED, DIFFERENTIAL INPUT ECL, HALF-SWING

	V	
Tpd ++ PAD1,PAD2->Y,YN	0.22	ns
+- PAD1,PAD2->Y,YN	0.22	ns
-+ PAD1,PAD2->Y,YN	0.22	ns
-- PAD1,PAD2->Y,YN	0.22	ns
IEE	2.90	mA
FAN-OUT LOAD LIMIT:	9	loads
k-FACTOR RISING	0.020	ns/LU
FALLING	0.020	ns/LU
MAXIMUM FREQUENCY OF OPERATION (fMAX)	600	MHz COM
	450	MHz MIL

BOTH INPUTS MUST BE USED
PAD1, PAD2 MUST BE DIFFERENTIALLY DRIVEN
*Y,YN OUTPUTS ARE 1/2 SWING (250mV)
*Y,YN MUST DRIVE A DIFFERENTIAL INPUT PAIR
*Y,YN CANNOT BE WIRE-ORED
*Y,YN CANNOT BE POWERED-DOWN

PAD1	PAD2	Y	YN
0	1	0	1
0	0	UND	UND
1	0	1	0
1	1	UND	UND



IE99V
VERY FAST DIFFERENTIAL

FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

OE10 2 I/O cells ECL DIFFERENTIAL DRIVER WITH OR GATE

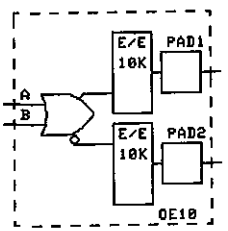
Tpd ++ A,B->PAD1	0.46	ns	
-- A,B->PAD1	0.46	ns	
Tpd +- A,B->PAD2	0.52	ns	
-+ A,B->PAD2	0.42	ns	
IEE	5.13	mA	OE10
MAXIMUM FREQUENCY OF OPERATION (fMAX)	360	MHz	

---

* A,B - AT LEAST ONE MUST BE DRIVEN BY A MACRO

Note: Use dual-cell macros such as OE10 for high-speed ECL output up to 360MHz. Use V macros for speeds up to 600MHz.

PAD1 = A + B PAD2 = $\overline{\overline{A} + \overline{B}}$



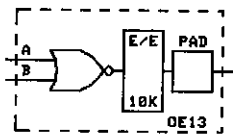
FOR HIGH-SPEED APPLICATIONS

FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

OE13	2 I/O cells	ECL 25 OHM NOR OUTPUT	
Tpd	+- A,B->PAD	0.45	ns
	-+ A,B->PAD	0.77	ns
IEE		13.60	mA

* A,B - AT LEAST ONE MUST BE DRIVEN BY A MACRO

$$PAD = \overline{A + B}$$



FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

Ox77 I/O cell 2:1 MUX ECL 10K OUTPUT

		OE77	OK77 (if different)	
Tpd	++ I0->PAD	0.55		ns
	-- I0->PAD	0.54		ns
Tpd	+- I0->YIN	0.21		ns
	-+ I0->YIN	0.54		ns
Tpd	++ I1->PAD	0.55		ns
	-- I1->PAD	0.58		ns
Tpd	+- I1->YIN	0.21		ns
	-+ I1->YIN	0.60		ns
Tpd	++ S1->PAD	0.67		ns
	-- S1->PAD	0.71		ns
	+- S1->PAD	0.62		ns
	-+ S1->PAD	0.72		ns
Tpd	+- S1->YIN	0.39		ns
	-+ S1->YIN	0.72		ns
	++ S1->YIN	0.62		ns
	-- S1->YIN	0.40		ns
Tpd	++ I0,I1->PAD		0.41	ns
	-- I0,I1->PAD		0.57	ns
Tpd	++ SI->PAD		0.52	ns
	+- SI->PAD		0.57	ns
	-+ SI->PAD		0.58	ns
	-- SI->PAD		0.69	ns
IEE		5.80	4.05	mA

FAN-OUT LOAD LIMIT: YIN 9

k-FACTOR	RISING	YIN	0.040	ns/LU
	FALLING	YIN	0.040	ns/LU

---

* YIN TO INTERNAL LOGIC - FROM OE77 ONLY
  I0, I1, S - EACH MUST BE DRIVEN BY A MACRO

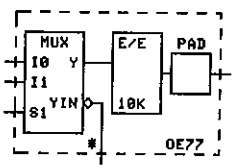
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

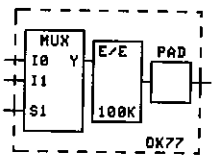
0x77 I/O cell 2:1 MUX ECL 10K OUTPUT

$PAD = I0.\overline{I1}\overline{S} + I1.S1$ $YIN = \overline{\overline{PAD}}$

S	I1	I0	PAD	YIN (YIN ON OE77 ONLY)
0	X	0	0	1
0	X	1	1	0
1	0	X	0	1
1	1	X	1	0
X	0	0	0	1
X	0	1	UNKNOWN	
X	1	0	UNKNOWN	
X	1	1	1	0

OE77: ECL 10K
OK77: ECL 100K





FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

0x80 I/O cell ECL OUTPUT WITH 3-INPUT NOR BUFFER

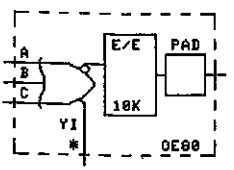
	OE80	0K80	
Tpd +- A,B,C->PAD	0.47		ns
-+ A,B,C->PAD	0.48		ns
Tpd ++ A,B,C->YI	0.44		ns
-- A,B,C->YI	0.17		ns
Tpd +- A,B,C->PAD		0.44	ns
Tpd -+ (separately)		0.42	ns
Tpd +- A,B,C->PAD		0.37	ns
Tpd -+ (together)		0.45	ns
IEE	5.58	5.13	mA
FAN-OUT LOAD LIMIT: YI	9	9	loads
k-FACTOR RISING	0.04	0.04	ns/LU
FALLING	0.04	0.04	ns/LU

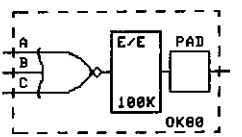
---

* YI TO INTERNAL LOGIC - FROM OE80 ONLY
EITHER A, B OR C MUST BE DRIVEN BY A MACRO

$PAD = \overline{A + B + C} = \bar{A}\,\bar{B}\,\bar{C}$ $\qquad YI = A + B + C$

OE80: ECL 10K
OK80: ECL 100K





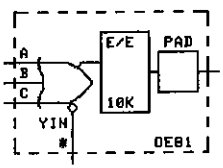
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

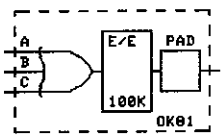
0x81 I/O cell	ECL OUTPUT WITH 3-INPUT OR BUFFER		
	OE81	OK81	
Tpd ++ A,B,C->PAD	0.53	0.34	ns
-- A,B,C->PAD	0.44	0.47	ns
Tpd +- A,B,C->YIN	0.20		ns
-+ A,B,C->YIN	0.41		ns
IEE	5.58	3.83	mA
FAN-OUT LOAD LIMIT: YIN	9	9	loads
k-FACTOR RISING	0.04	0.04	ns/LU
FALLING	0.04	0.04	ns/LU

* YIN TO INTERNAL LOGIC - FROM OE81 ONLY
  EITHER A, B OR C MUST BE DRIVEN BY A MACRO

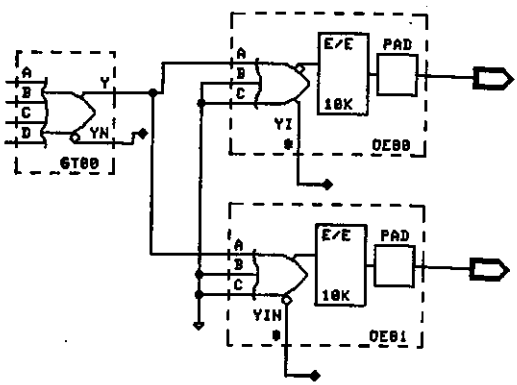
$$PAD = A + B + C \qquad YIN = \overline{A + B + C} = \overline{A}\,\overline{B}\,\overline{C}$$

OE81: ECL 10K
OK81: ECL 100K





DIFFERENTIAL



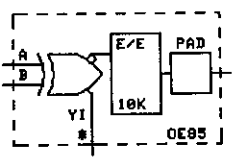
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

OE85	I/O cell	ECL 10K OUTPUT EXNOR	
		S	
Tpd	++ A->YI	0.46	ns
	-- A->YI	0.29	ns
	+- A->YI	0.20	ns
	-+ A->YI	0.66	ns
Tpd	++ B->YI	0.56	ns
	-- B->YI	0.39	ns
	+- B->YI	0.34	ns
	-+ B->YI	0.69	ns
Tpd	++ A->PAD	0.47	ns
	-+ A->PAD	0.65	ns
	++ A->PAD	0.52	ns
	-- A->PAD	0.64	ns
Tpd	+- B->PAD	0.59	ns
	-+ B->PAD	0.72	ns
	++ B->PAD	0.65	ns
	-- B->PAD	0.67	ns
IEE		5.58	mA
FAN-OUT LOAD LIMIT: YI		9	loads
k-FACTOR	RISING	YIN 0.040	ns/LU
	FALLING	YIN 0.040	ns/LU

* YI TO INTERNAL LOGIC - FROM OE85 ONLY
  A, B - EACH MUST BE DRIVEN BY A MACRO

$PAD = \overline{A \oplus B}$ $\qquad$ $YI = A \oplus B$

OE85: ECL 10K
OK85: ECL 100K



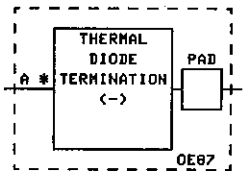
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

OE87 I/O cell PAD MACRO FOR THERMAL DIODE

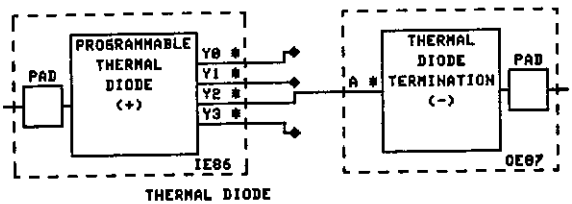
	S	
Tpd A->PAD	0.10	ns
IEE	0.0	mA

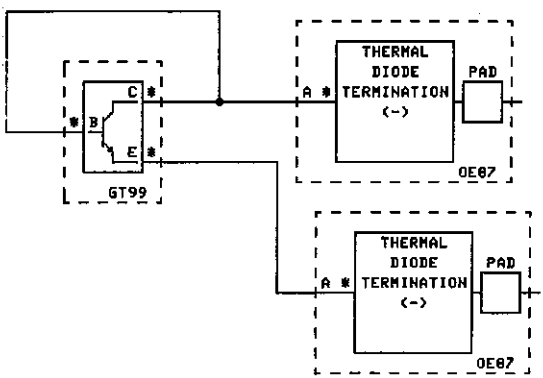
A MUST BE DRIVEN BY THE THERMAL DIODE MACRO
(IE86 or GT99)

OE87: ECL 10K
OK87: ECL 100K



USE WITH IE86 OR GT99





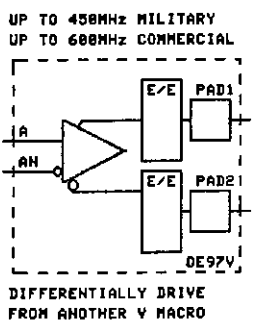
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

OE97V 2 I/O CELLS VERY HI-SPEED DIFFERENTIAL INPUT, DIFFERENTIAL OUTPUT

	V		
Tpd ++ A,AN->PAD1,PAD2	0.34	ns	
+- A,AN->PAD1,PAD2	0.34	ns	
-+ A,AN->PAD1,PAD2	0.34	ns	
-- A,AN->PAD1,PAD2	0.34	ns	
IEE	4.75	mA	OEnn
MAXIMUM FREQUENCY	600	MHz	COM
OF OPERATION	450	MHz	MIL
(fMAX)			

PAD1,PAD2 OUTPUTS ARE 1/2 SWING EXTERNAL ECL
A,AN MUST BE DIFFERENTIALLY DRIVEN FROM ONE MACRO
BOTH INPUTS MUST BE USED

A	AN	PAD1	PAD2	
0	1	0	1	
0	0	UND	UND	ILLEGAL
1	0	1	0	
1	1	UND	UND	ILLEGAL



FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

UE50 I/O cell ECL BIDIRECTIONAL I/O WITH BUFFER

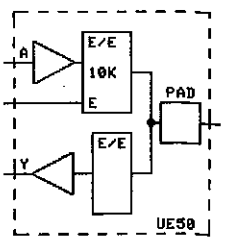
		S	
Tpd	++ A->PAD	0.54	ns
	-- A->PAD	0.59	ns
	-- E->PAD	0.69	ns
	++ E->PAD	0.65	ns
	++ PAD->Y	0.77	ns
	-- PAD->Y	0.50	ns
IEE		5.40	mA
FAN-OUT LOAD LIMIT: Y		9	loads
k-FACTOR	RISING YIN	0.040	ns/LU
	FALLING YIN	0.040	ns/LU

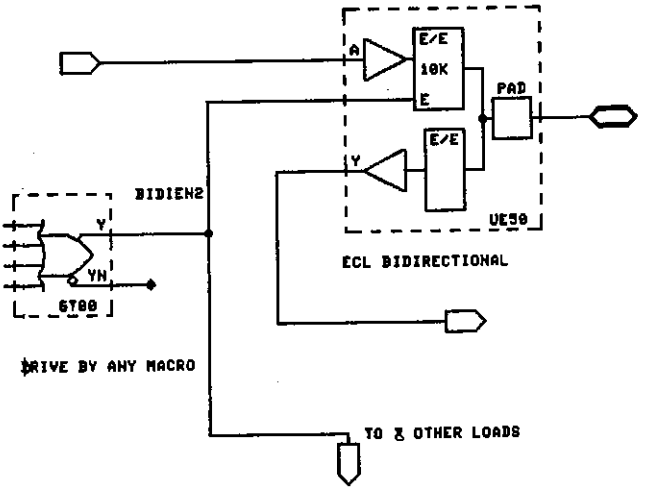
---

* Y TO INTERNAL LOGIC
  ENABLE FROM ANY INTERNAL SIGNAL
  ENABLE SIGNAL NAME MUST APPEAR IN SIMULATION FORMAT
  A, E - EACH MUST BE DRIVEN BY A MACRO

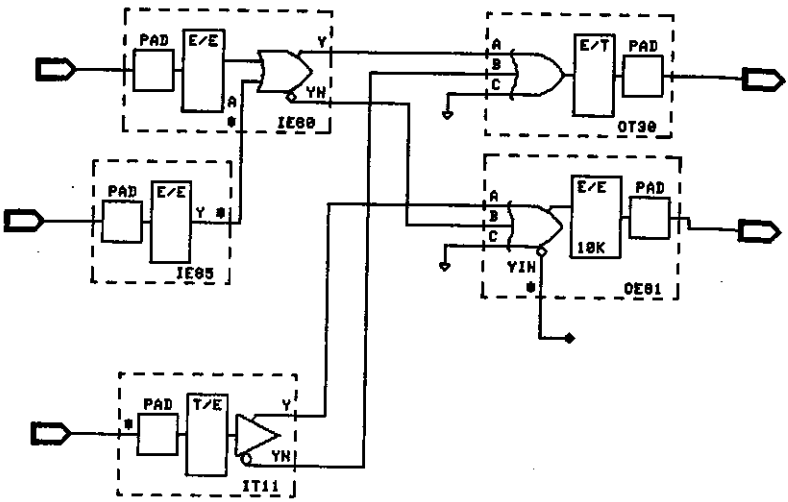
E	A	PAD	Y	
1	0	0	0	OUTPUT MODE
1	1	1	1	OUTPUT MODE
0	X	0	0	INPUT MODE
0	X	1	1	INPUT MODE

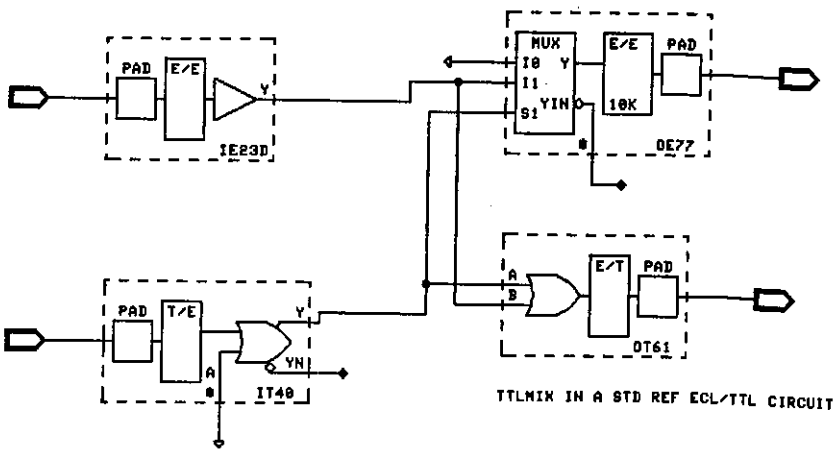
UE50: ECL 10K
UK50: ECL 100K not released




A
E/E
10K
E
PAD
Y
E/E
UE30
ECL BIDIRECTIONAL
BIDIEN2
Y
YN
6T80
DRIVE BY ANY MACRO
TO 8 OTHER LOADS

TTL IN A +5V REF ECL/TTL CIRCUIT





TTLMIX IN A STD REF ECL/TTL CIRCUIT

Section 6-4:

Logic Macros

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL OR +5V REF ECL PATH,
ELSE I = IEE

AD05 L cell 1-BIT FULL ADDER

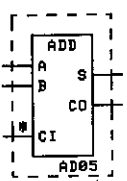
		S	L	H	
Tpd	++ A->S	0.87	0.77	0.57	ns
	+- A->S	1.04	0.83	0.64	ns
	-+ A->S	0.77	0.95	0.54	ns
	-- A->S	0.76	0.82	0.49	ns
Tpd	++ B->S	1.13	1.02	0.74	ns
	+- B->S	1.22	1.01	0.81	ns
	-+ B->S	0.96	1.11	0.63	ns
	-- B->S	0.94	1.01	0.62	ns
Tpd	++ CI->S	1.04	0.89	0.40	ns
	+- CI->S	0.56	0.43	0.34	ns
	-+ CI->S	0.39	0.47	0.25	ns
	-- CI->S	0.43	0.49	0.33	ns
Tpd	++ CI->CO	0.68	0.61	0.39	ns
	-- CI->CO	0.48	0.54	0.33	ns
Tpd	++ A->CO	0.85	0.76	0.51	ns
	-- A->CO	0.73	0.78	0.47	ns
Tpd	++ B->CO	1.06	0.97	0.72	ns
	-- B->CO	0.95	1.00	0.62	ns
I		1.62	1.26	2.52	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

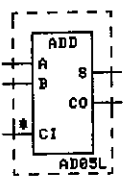
---

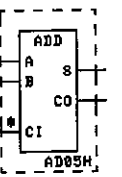
* CI COUNTS AS 2 LOADS; (A,B COUNT AS 1 LOAD EACH)
A,B - EACH MUST BE DRIVEN BY A MACRO

$S = A \oplus B \oplus CI \qquad CO = A\,B + (A \oplus B)\,CI$

A	B	CI	S	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1







⊕ = EXOR

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

ADD00 5 L cells 4-BIT CARRY LOOK-AHEAD ADDER WITH CARRY OUTPUT

		S	L	H	
Tpd	++ Ai,Bi->Si	2.60	2.52	1.58	ns
	-+ Ai,Bi->Si	2.27	2.00	1.48	ns
	+- Ai,Bi->Si	2.54	2.88	1.84	ns
	-- Ai,Bi->Si	2.21	2.36	1.74	ns
Tpd	++ Ai,Bi->CO	2.08	2.20	1.48	ns
	-+ Ai,Bi->CO	1.75	1.68	1.38	ns
	+- Ai,Bi->CO	2.04	2.01	1.20	ns
	-- Ai,Bi->CO	1.71	1.49	1.10	ns
Tpd	++ CI->CO	1.54	1.40	0.81	ns
	-- CI->CO	1.03	1.40	0.78	ns
Tpd	++ CI->Si	1.68	1.53	0.99	ns
	-+ CI->Si	1.45	1.66	1.07	ns
	+- CI->Si	1.43	1.42	0.93	ns
	-- CI->Si	1.20	1.55	1.01	ns
	i= 0,1,2,3				
I		12.51	10.35	18.36	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
INTERCONNECT PINS:		40	40	40	internal
k-FACTOR	RISING	0.040	0.040	0.020	ns/LU
	FALLING	0.040	0.080	0.040	ns/LU

* CI COUNTS AS 5 LOADS
* ALL Ai INPUTS COUNT AS 2 LOADS EACH
  B0, B1, B2, B3 - EACH MUST BE DRIVEN BY A MACRO
* OUTPUT CO CANNOT BE WIRE-ORED

ADD00 is a four-bit semi-fast carry look-ahead adder with carry output designed for use in a ripple-carry configuration. It can be cascaded by attaching the CO output of one stage to the CI input of the next stage. The main advantage of this adder over ADD02 is a hardware savings if speed is not the critical parameter. A 16-bit adder requires 20 L cells.

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

ADD00 5 L cells 4-BIT CARRY LOOK-AHEAD ADDER WITH CARRY OUTPUT

$P0 = A0 \oplus B0$ $S0 = \overline{P0} \oplus \overline{CI}$

$P1 = A1 \oplus B1$ $S1 = \overline{P1} \oplus \overline{CI}$

$P2 = A2 \oplus B2$ $S2 = \overline{P2} \oplus \overline{CI}$

$P3 = A3 \oplus B3$ $S3 = \overline{P3} \oplus \overline{CI}$

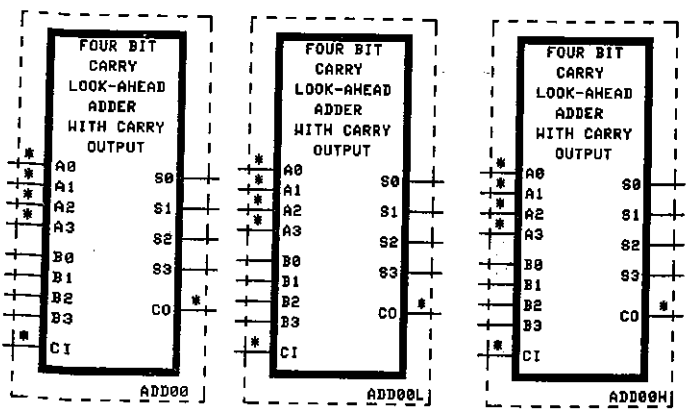
$G0 = A0 \cdot B0$
$G1 = A1 \cdot B1$
$G2 = A2 \cdot B2$
$G3 = A3 \cdot B3$

$$C1 = G0 + (\overline{P0} + \overline{CI})$$

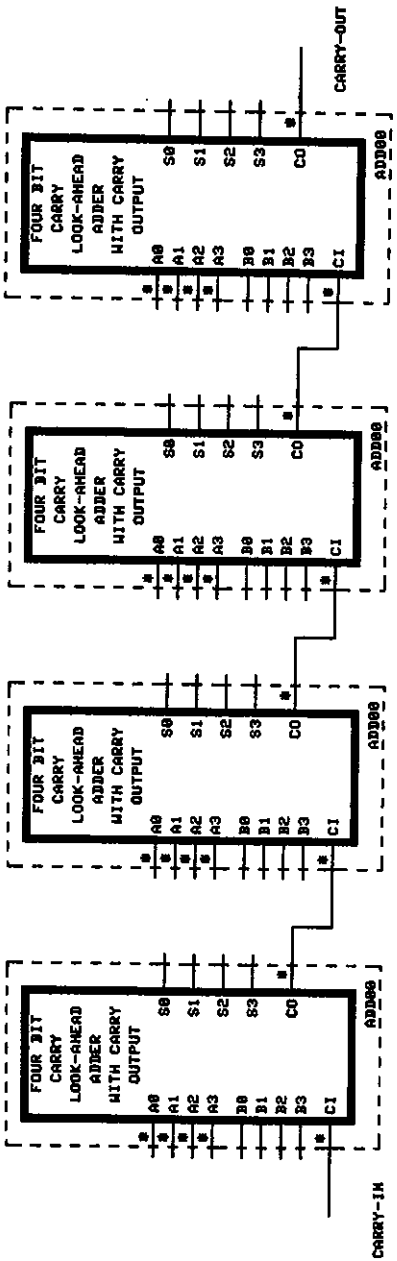
$$C2 = G1 + (\overline{P1} + \overline{G0}) + (\overline{P1} + \overline{P0} + \overline{CI})$$

$$C3 = G2 + (\overline{P2} + \overline{G1}) + (\overline{P2} + \overline{P1} + \overline{G0}) + (\overline{P2} + \overline{P1} + \overline{P0} + \overline{CI})$$

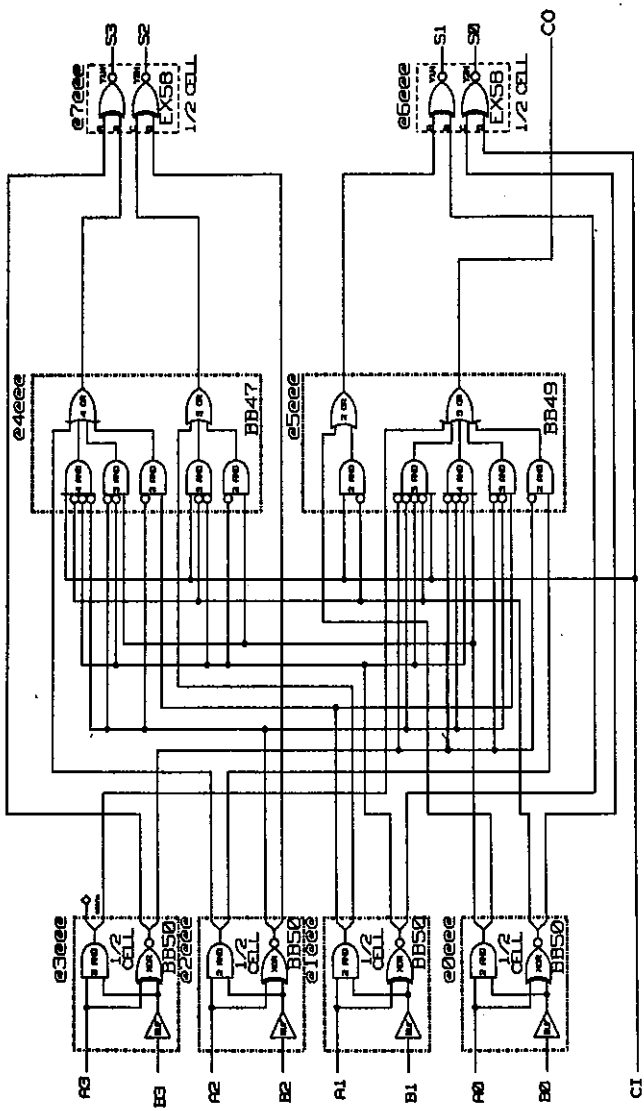
$$C4 = G3 + (\overline{P3} + \overline{G2}) + (\overline{P3} + \overline{P2} + \overline{G1}) + (\overline{P3} + \overline{P2} + \overline{P1} + \overline{G0}) + (\overline{P3} + \overline{P2} + \overline{P1} + \overline{P0} + \overline{CI})$$



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE



16-BIT RIPPLE-CARRY ADDER



PREPLACEMENTS MUST USE THIS CELL ARRANGEMENT:

0	1	7	3	4	5	6	2

AMCC Q5000 MACRO SUMMARY - ADxx (804)

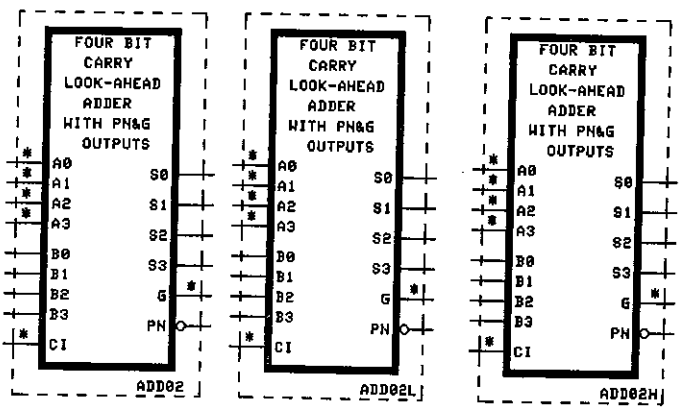
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

ADD02 5 L cells 4-BIT CARRY LOOK-AHEAD ADDER WITH G AND PN OUTPUTS

		S	L	H	
Tpd	ALL Ai,Bi->ALL S	2.56	2.63	2.08	ns
	ALL Ai,Bi->PN	1.90	1.84	1.12	ns
	All Ai,Bi->G	2.17	1.90	1.21	ns
	CI->ALL S	1.47	1.46	0.93	ns
	i= 0,1,2,3				
I		12.87	10.53	18.72	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
INTERCONNECT PINS:		40	40	40	internal
k-FACTOR	RISING	0.040	0.040	0.020	ns/LU
	FALLING	0.040	0.080	0.040	ns/LU

---

* CI COUNTS AS 4 LOADS
* ALL Ai INPUTS COUNT AS 2 LOADS EACH
  B0, B1, B2, B3 - EACH MUST BE DRIVEN BY A MACRO
* OUTPUT G CANNOT BE WIRE-ORED



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

ADD02 5 L cells 4-BIT CARRY LOOK-AHEAD ADDER WITH G AND PN OUTPUTS

The ADD02 is a four-bit fast carry look-ahead adder with negated propagate (PN) and generate (G) outputs. These outputs feed inputs on the carry look-ahead generator (CPG02). CPG02 can handle the PN and G inputs from a total of four ADD02s, allowing the construction of a 16-bit carry-look-ahead adder. It is faster than a 16-bit ripple-carry adder but requires more L cells. A 16-bit carry look-ahead adder requires 24 L cells.

$P0 = A0 \oplus B0$ $\quad S0 = \overline{P0} \oplus \overline{CI}$

$P1 = A1 \oplus B1$ $\quad S1 = \overline{P1} \oplus \overline{CI}$

$P2 = A2 \oplus B2$ $\quad S2 = \overline{P2} \oplus \overline{CI}$

$P3 = A3 \oplus B3$ $\quad S3 = \overline{P3} \oplus \overline{CI}$

$G0 = A0 \cdot B0$

$G1 = A1 \cdot B1$

$G2 = A2 \cdot B2$

$G3 = A3 \cdot B3$

$$C1 = G0 + (\overline{P0} + \overline{CI})$$

$$C2 = G1 + (\overline{P1 + G0}) + (\overline{P1} + \overline{P0} + \overline{CI})$$

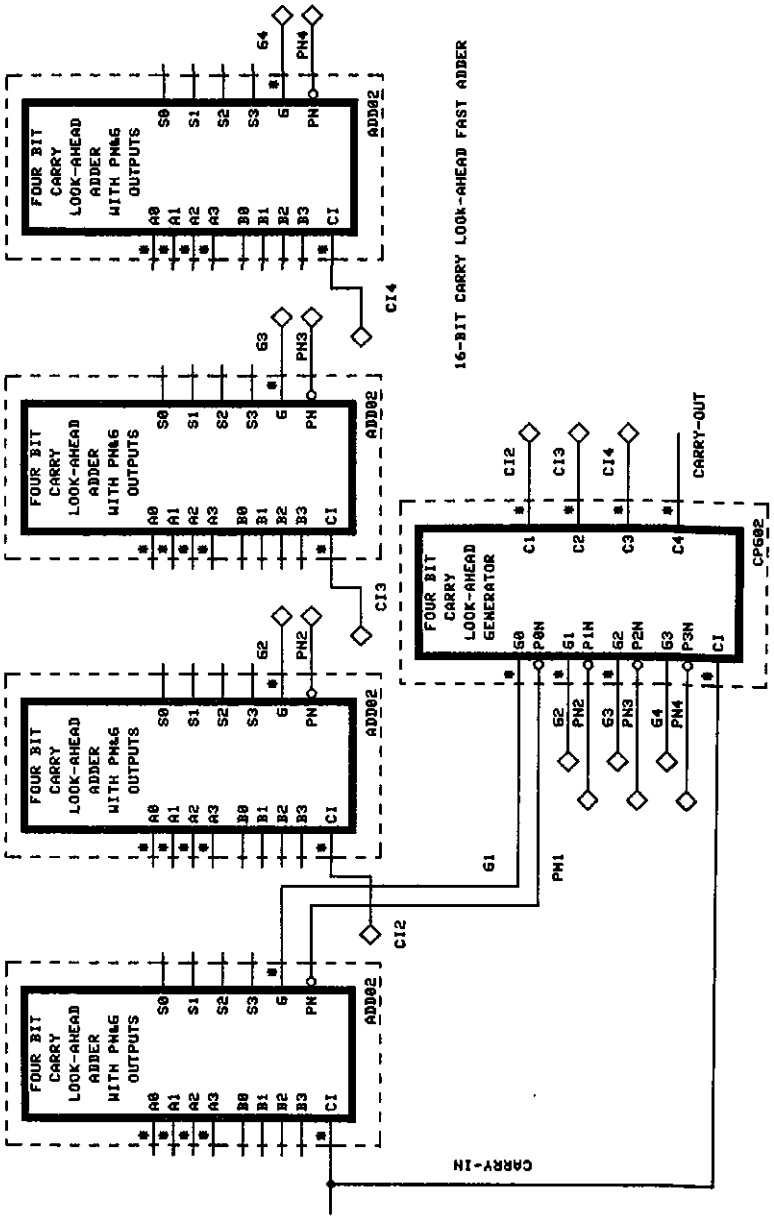
$$C3 = G2 + (\overline{P2 + G1}) + (\overline{P2 + P1 + G0}) + (\overline{P2} + \overline{P1} + \overline{P0} + \overline{CI})$$

$$C4 = G3 + (\overline{P3 + G2}) + (\overline{P3 + P2 + G1}) + (\overline{P3} + \overline{P2} + \overline{P1} + \overline{G0}) + (\overline{P3 + P2 + P1 + P0} + \overline{CI})$$

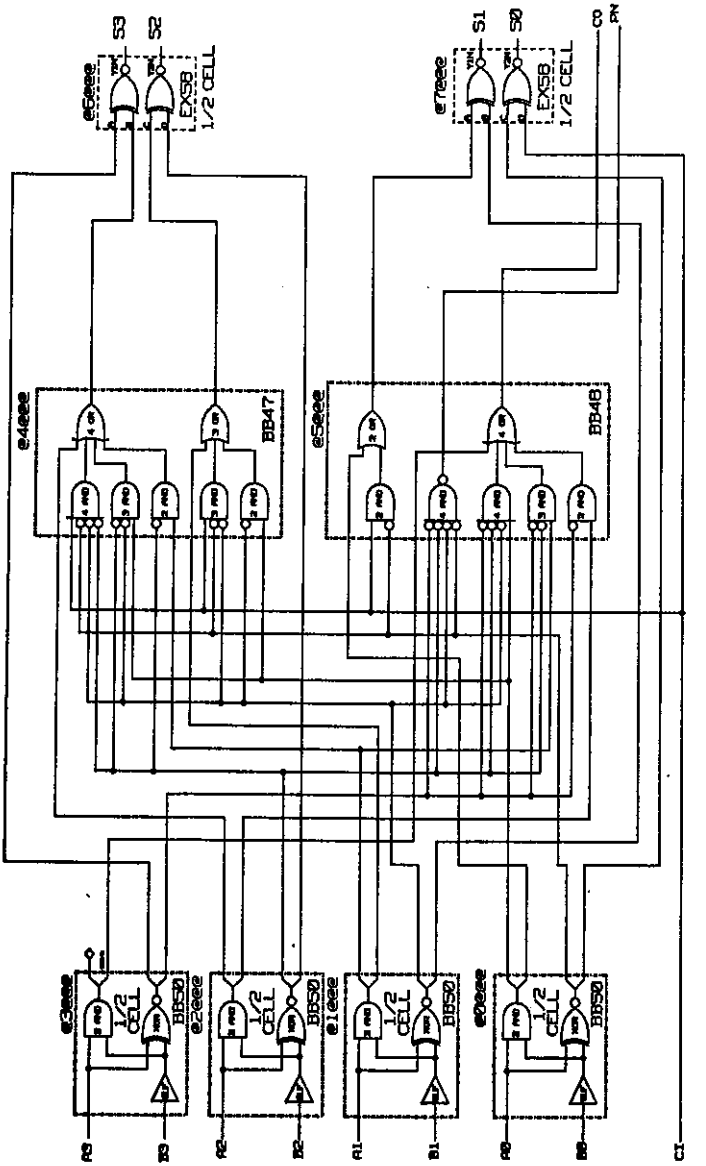
$$G = G3 + (\overline{P3 + G2}) + (\overline{P3 + P2 + G1}) + (\overline{P3} + \overline{P2} + \overline{P1} + \overline{G0})$$

$$PN = \overline{P3} + \overline{P2} + \overline{P1} + \overline{P0}$$

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE



Q5000 ADD02



PREPLACEMENTS MUST USE THIS CELL ARRANGEMENT:

0	1	7	3	4	5	6	2

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

CMP00 4.5 L cells 6-BIT COMPARATOR WITH LOW ENABLE

		S	L	H	
Tpd	++A0-5->AGB	2.83	2.86	1.99	ns
	+-A0-5->AGB	2.48	2.77	1.89	ns
	--A0-5->AGB	2.47	2.61	1.87	ns
	-+A0-5->AGB	2.85	2.77	1.96	ns
Tpd	++B0-5->AGB	2.66	2.68	1.84	ns
	+-B0-5->AGB	2.29	2.42	1.74	ns
	--B0-5->AGB	2.23	2.37	1.69	ns
	-+B0-5->AGB	2.61	2.65	1.81	ns
Tpd	++A0-5->ALB	2.65	2.86	1.92	ns
	+-A0-5->ALB	2.70	2.81	1.91	ns
	--A0-5->ALB	2.72	2.70	1.96	ns
	-+A0-5->ALB	2.64	2.72	1.90	ns
Tpd	++B0-5->ALB	2.46	2.51	1.77	ns
	+-B0-5->ALB	2.53	2.63	1.76	ns
	--B0-5->ALB	2.48	2.60	1.73	ns
	-+B0-5->ALB	2.40	2.46	1.72	ns
Tpd	++A0-5->AEB	1.86	2.15	1.35	ns
	+-A0-5->AEB	1.93	1.88	1.33	ns
	--A0-5->AEB	1.85	1.99	1.33	ns
	-+A0-5->AEB	1.95	1.79	1.30	ns
Tpd	++B0-5->AEB	1.67	1.80	1.20	ns
	+-B0-5->AEB	1.76	1.70	1.18	ns
	--B0-5->AEB	1.61	1.75	1.15	ns
	-+B0-5->AEB	1.71	1.67	1.15	ns
Tpd	+-EN->AGB	0.35	0.39	0.30	ns
	-+EN->AGB	0.49	0.45	0.35	ns
Tpd	+-EN->AEB	0.67	0.72	0.53	ns
	-+EN->AEB	0.67	0.61	0.44	ns
Tpd	+-EN->ALB	0.66	0.70	0.52	ns
	-+EN->ALB	0.68	0.61	0.44	ns
I		12.51	10.71	16.34	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
INTERCONNECT PINS:		17	17	17	internal
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

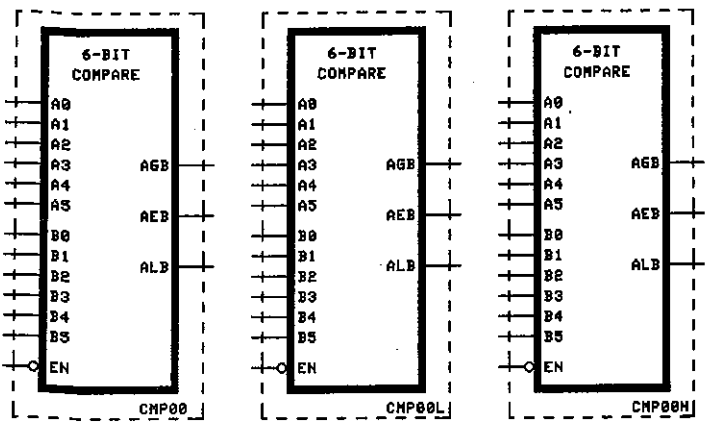
A0,A1,A2,A3,A4,A5,EN - EACH MUST BE DRIVEN BY A MACRO
* A0,A1,A2,A3,A4,A5,B0,B1,B2,B3,B4,B5,EN -
ALL COUNT AS 2 LOADS EACH

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

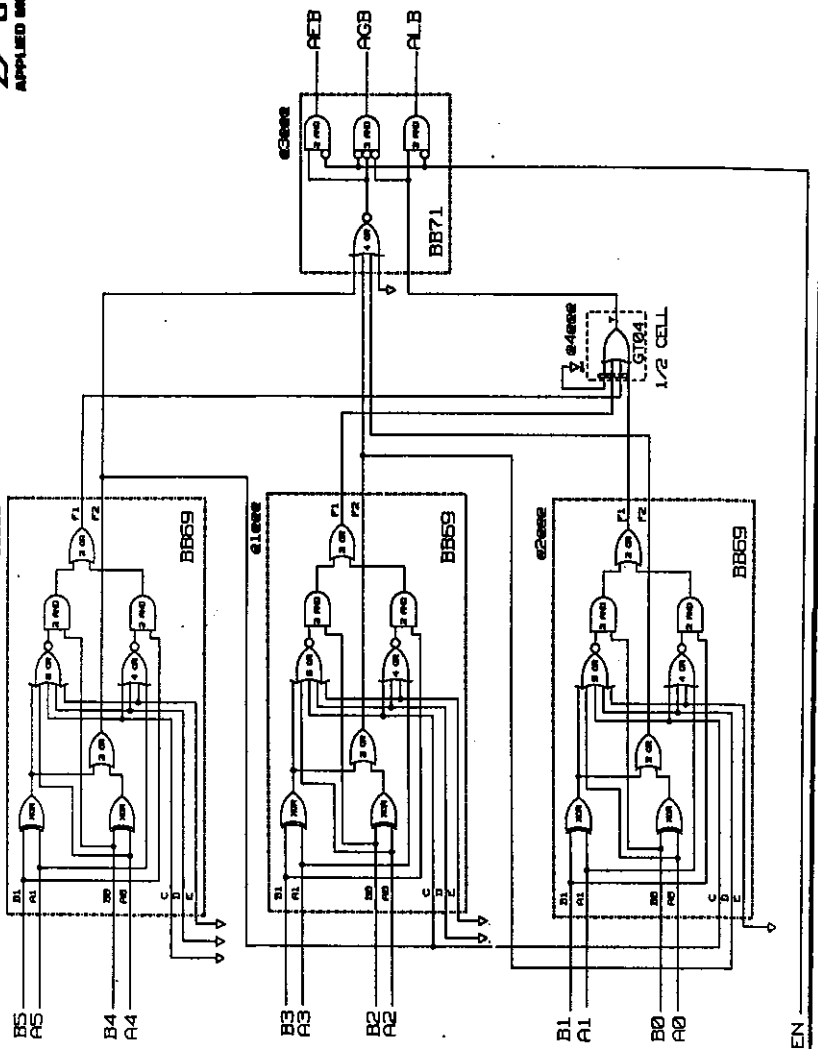
CMP00 4.5 L cells 6-BIT COMPARATOR WITH LOW ENABLE

A 6-bit comparator with A > B, A = B, and A < B outputs and a low enable. Compares the magnitude of two 6-bit or less binary numbers. A high level on the enable line (EN) forces all outputs low.

EN	COMPARE	AGB	AEB	ALB
1	X	0	0	0
0	A>B	1	0	0
0	A=B	0	1	0
0	A<B	0	0	1



Q5000 CMP00



PREPLACEMENTS MUST USE THIS CELL ARRANGEMENT:

4	3	2	1	0

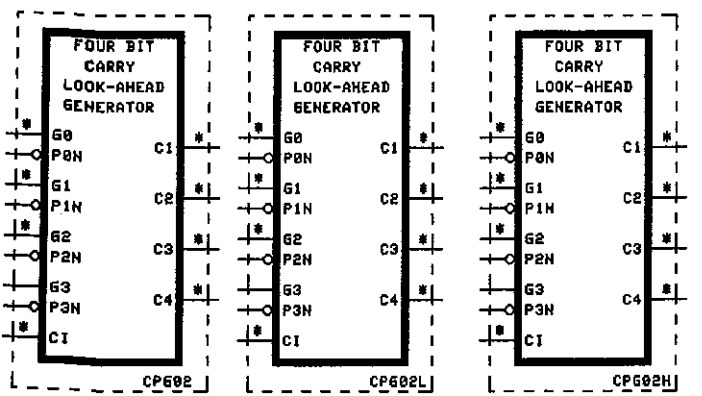
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

CPG02 4 L cells 4-BIT CARRY LOOK-AHEAD GENERATOR

		S	L	H	
Tpd	PiN->Cj	1.33	1.21	0.74	ns
	Gi,Ci->Cj	1.29	1.15	0.65	ns
	i= 0,1,2,3				
	j= 1,2,3,4				
I		5.50	4.78	9.54	mA
FAN-OUT LOAD LIMIT		9	4	9	loads
INTERCONNECT PINS:		21	21	21	internal
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

* G0 COUNTS AS 4 LOADS
* G1 COUNTS AS 3 LOADS
* G2 COUNTS AS 2 LOADS
* CI COUNTS AS 4 LOADS
P0N, P1N, P2N, P3N - EACH MUST BE DRIVEN BY A MACRO
* C1, C2, C3, C4 - THESE OUTPUTS CANNOT BE WIRE-ORED
THESE OUTPUTS CANNOT BE POWERED-DOWN

• FOR USE WITH ADD02



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

CPG02 4 L cells 4-BIT CARRY LOOK-AHEAD GENERATOR

Carry look-ahead generator for use with ADD02. Inputs are negated propagate (PN) and generate (G) from up to four ADD02s, to permit a 16-bit fast addition to be performed. Additional cascading requires the C4 output from this macro to feed the CI input of the next ADD02 stage.

$$C1 = G0 + (\overline{P0N})(CI)$$

$$C2 = G1 + (\overline{P1N})(G0) + (\overline{P1N})(\overline{P0N})(CI)$$

$$C3 = G2 + (\overline{P2N})(G1) + (\overline{P2N})(\overline{P1N})(G0) + (\overline{P2N})(\overline{P1N})(\overline{P0N})(CI)$$

$$C4 = G3 + (\overline{P3N})(G2) + (\overline{P3N})(\overline{P2N})(G1) + (\overline{P3N})(\overline{P2N})(\overline{P1N})(G0) + (\overline{P3N})(\overline{P2N})(\overline{P1N})(\overline{P0N})(CI)$$

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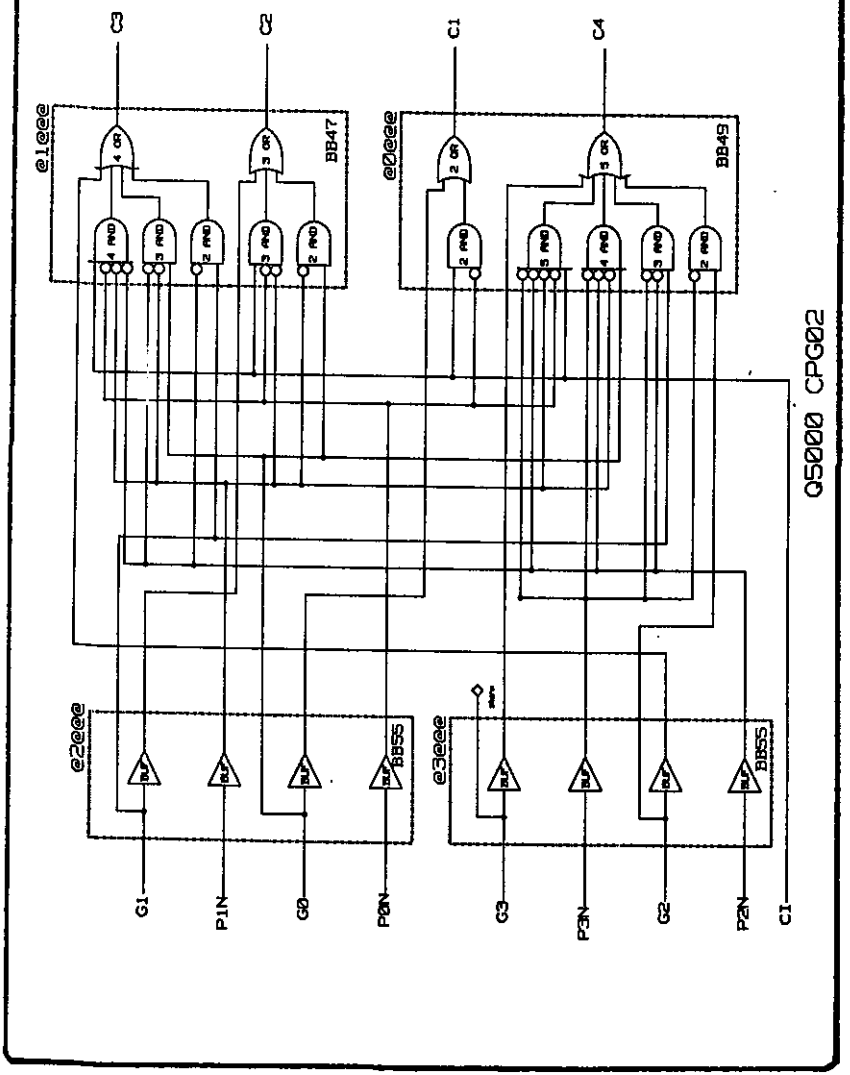
PREPLACEMENTS MUST USE THIS CELL ARRANGEMENT:

2	1	0	3



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

CTR02 6 L cells 4-BIT UP-COUNTER, RISING-EDGE LATCHED, WITH ASYNC. SET, ASYNC. RESET

	S	L	H	
Tpd CLK->ALL QiN	1.83	1.68	1.05	ns
CLK->TC	1.12	1.21	0.80	ns
CLK->TCN	1.26	1.17	0.77	ns
AR->ALL QiN	1.66	1.51	0.84	ns
AS->ALL QiN i= 0,1,2,3	1.12	1.25	0.79	ns
Tsu (PE)	1.93	2.17	1.93	ns min
Th (PE)	-1.21	-2.02	-1.21	ns min
Tsu (CE1,CE2)	4.28	4.09	3.45	ns min
Tsu (CE3,CE4)	4.61	4.39	3.70	ns min
Th (CE1,CE2)	-1.50	-1.41	-0.70	ns min
Th (CE3,CE4)	-1.66	-1.55	-0.82	ns min
Tsu (Di)	2.00	2.00	2.00	ns min
Th (Di)	-0.40	-0.40	0.00	ns min
Trec (AR)	1.40	1.40	1.40	ns min
Trec (AS)	2.50	2.50	2.50	ns min
PW (CLK,AS,AR)	2.86	4.00	1.67	ns min
I	15.79	13.63	20.52	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU
INTERCONNECT PINS:	45	45	45	internal
MAXIMUM FREQUENCY OF OPERATION	145	110	195	MHz COM
(fMAX)	135	105	185	MHz MIL

RISING EDGE TRIGGERED
PE,AR,AS,CLK - EACH MUST BE DRIVEN BY A MACRO
CE3,CE4 - EACH MUST BE DRIVEN BY A MACRO
RESET INPUT (AR) OVERRIDES ALL INPUTS (EXCEPT SET)
TO PULL Qx OUTPUTS LOW
SET INPUT (AS) OVERRIDES ALL INPUTS (EXCEPT RESET)
TO PULL Qx OUTPUTS HIGH
ALL FAN-INS ARE 1 LOAD

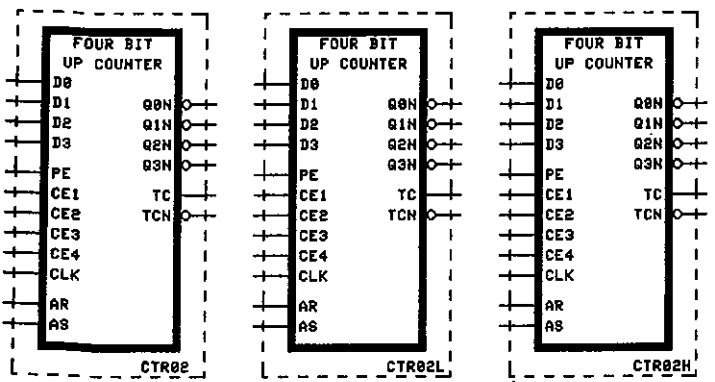
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

CTR02 6 L cells 4-BIT UP-COUNTER, RISING-EDGE LATCHED, WITH ASYNC. SET, ASYNC. RESET

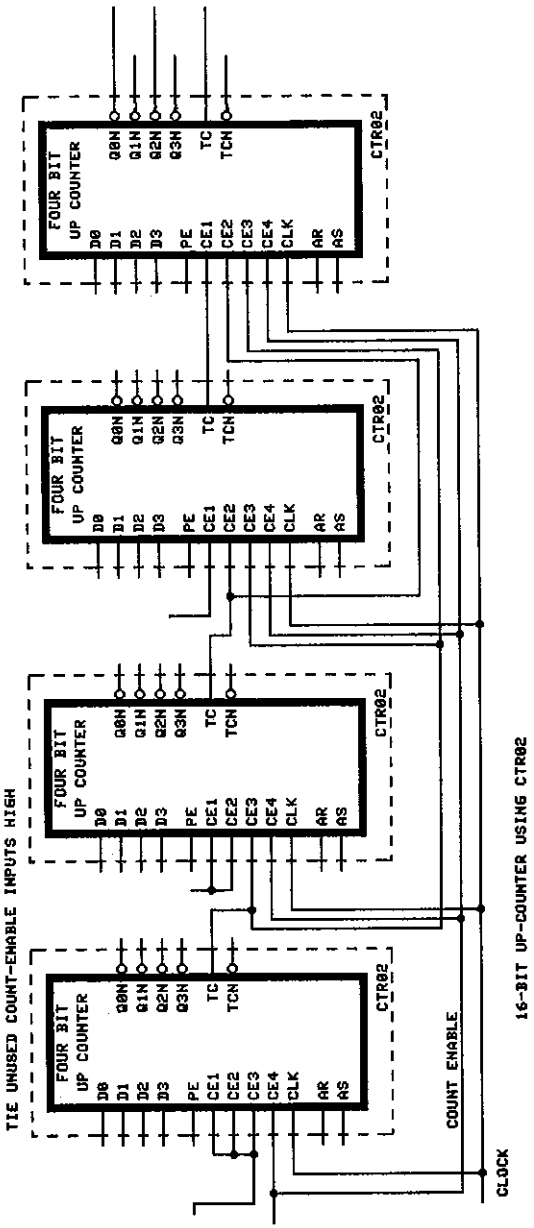
CTR02 is a positive edge triggered, resetable, four-bit up-counter with active low outputs. TC, TCN are synchronous with the QiN outputs and are in phase with them. This macro may be cascaded with itself to form up to a 16-bit counter by connecting TC outputs to CE inputs.

For any number of CEi inputs, i < 4, the unused CE inputs should be tied high.

AR	AS	PE	CE1	CE2	CE3	CE4	CLK	MODE
0	0	1	X	X	X	X	R	LOAD
0	0	0	0	X	X	X	R	HOLD
0	0	0	X	0	X	X	R	HOLD
0	0	0	X	X	0	X	R	HOLD
0	0	0	X	X	X	0	R	HOLD
0	0	0	1	1	1	1	R	COUNT
1	0	X	X	X	X	X	X	RESET
0	1	X	X	X	X	X	X	SET
1	1	X	X	X	X	X	X	UNKNOWN



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE



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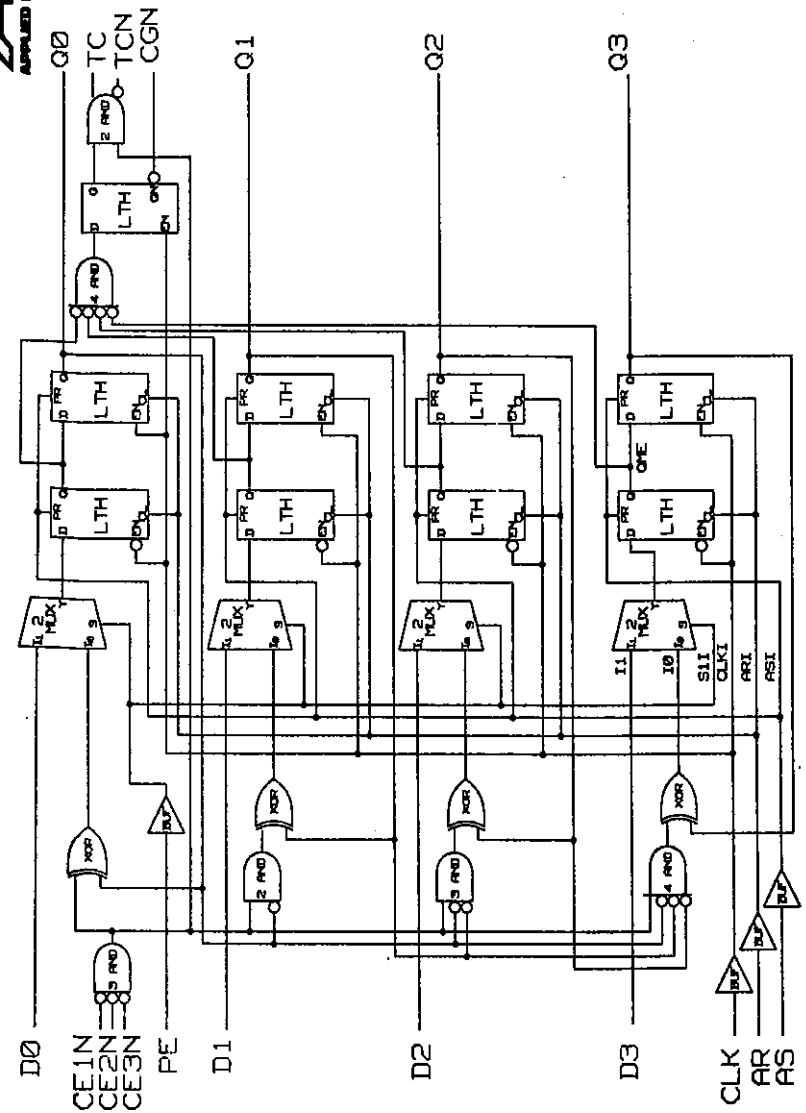
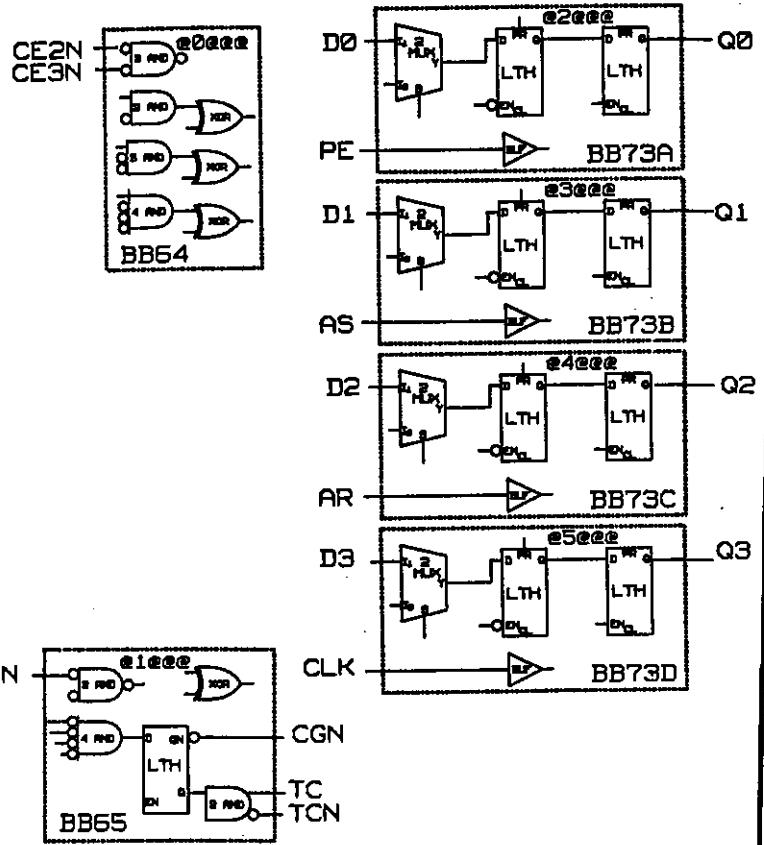
Q5000 CTR04
FUNCTIONAL DRAWING



Q5000 CTR04
BUILDING BLOCKS



PREPLACEMENTS MUST USE

THIS CELL ARRANGEMENT

BB73D @5@@@	BB73C @4@@@	BB73B @3@@@	BB73A @2@@@	BB65 @1@@@	BB64 @0@@@

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

detail

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

CTR04 6 L cells 4-BIT DOWN-COUNTER, RISING-EDGE LATCHED, ASYNC. SET, ASYNC. RESET, CGN OUTPUT

	S	L	H	
Tpd CLK->ALL Qi	1.73	1.55	0.98	ns
AR->ALL Qi	1.50	1.63	1.12	ns
AS->ALL Qi	1.70	1.53	0.98	ns
CLK->TC,TCN	2.02	1.93	1.36	ns
CLK->CGN	1.46	1.35	0.83	ns
CEiN->TC,TCN i= 0,1,2,3	0.68	0.66	0.42	ns
Tsu (PE)	2.00	2.00	1.00	ns min
Th (PE)	-0.30	-0.30	0.00	ns min
Tsu (CE1N,CE2N,CE3N)	3.30	2.90	1.60	ns min
Th (CE1N,CE2N,CE3N)	-0.90	-0.90	-0.90	ns min
Tsu (D0,D1,D2,D3)	2.30	1.80	0.90	ns min
Th (D0,D1,D2,D3)	0.00	0.00	0.00	ns min
Trec (AR,AS)	1.40	1.40	1.40	ns min
PW (CLK,AS,AR)	2.86	4.00	1.67	ns min
I	16.88	14.36	20.93	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU
INTERCONNECT PINS:	45	45	45	internal
MAXIMUM FREQUENCY OF OPERATION	150	115	195	MHz COM
(fMAX)	140	105	185	MHz MIL

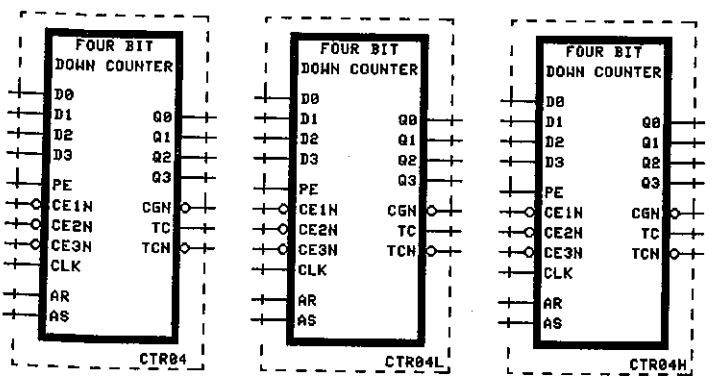
RISING EDGE TRIGGERED
PE,AR,AS,CLK - EACH MUST BE DRIVEN BY A MACRO
CE1N,CE2N,CE3N - AT LEAST ONE MUST BE DRIVEN BY A MACRO
RESET INPUT (AR) OVERRIDES ALL INPUTS (EXCEPT SET)
TO PULL Qx OUTPUTS LOW
SET INPUT (AS) OVERRIDES ALL INPUTS (EXCEPT RESET)
TO PULL Qx OUTPUTS HIGH

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

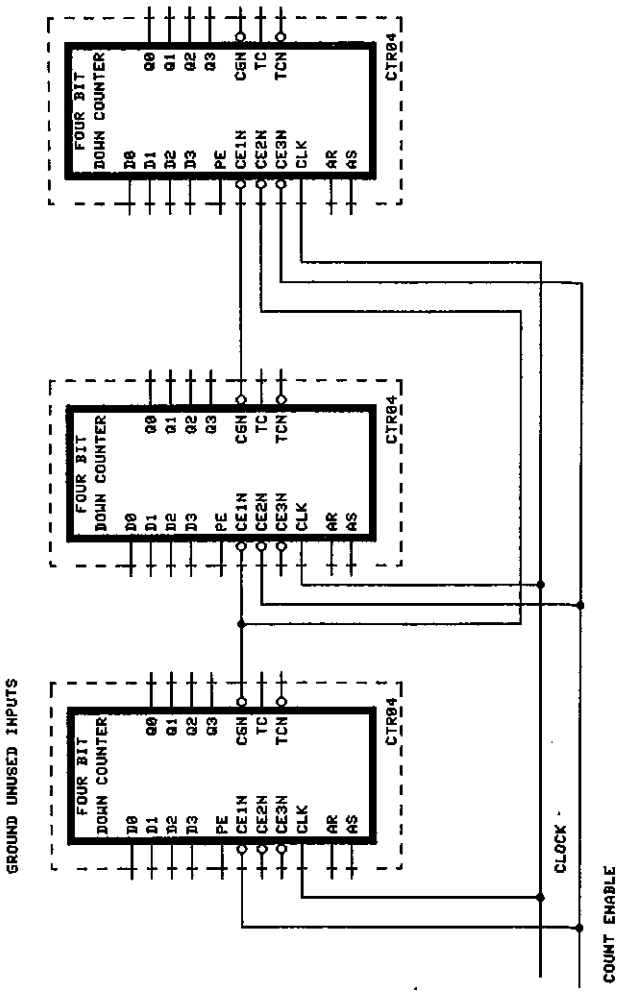
CTR04 6 L cells 4-BIT DOWN-COUNTER, RISING-EDGE LATCHED, ASYNC. SET, ASYNC. RESET, CGN OUTPUT

CTR04 is a positive edge triggered, resetable, four-bit down-counter with active high outputs. TC, TCN are synchronous with the Q outputs and are in phase with them. Cascadable for up to 12-bit fast down-counter by attaching CGN output from one stage to CEN input of following stage; can cascade additional stages by attaching TCN output of one stage to CEN input of following stage.

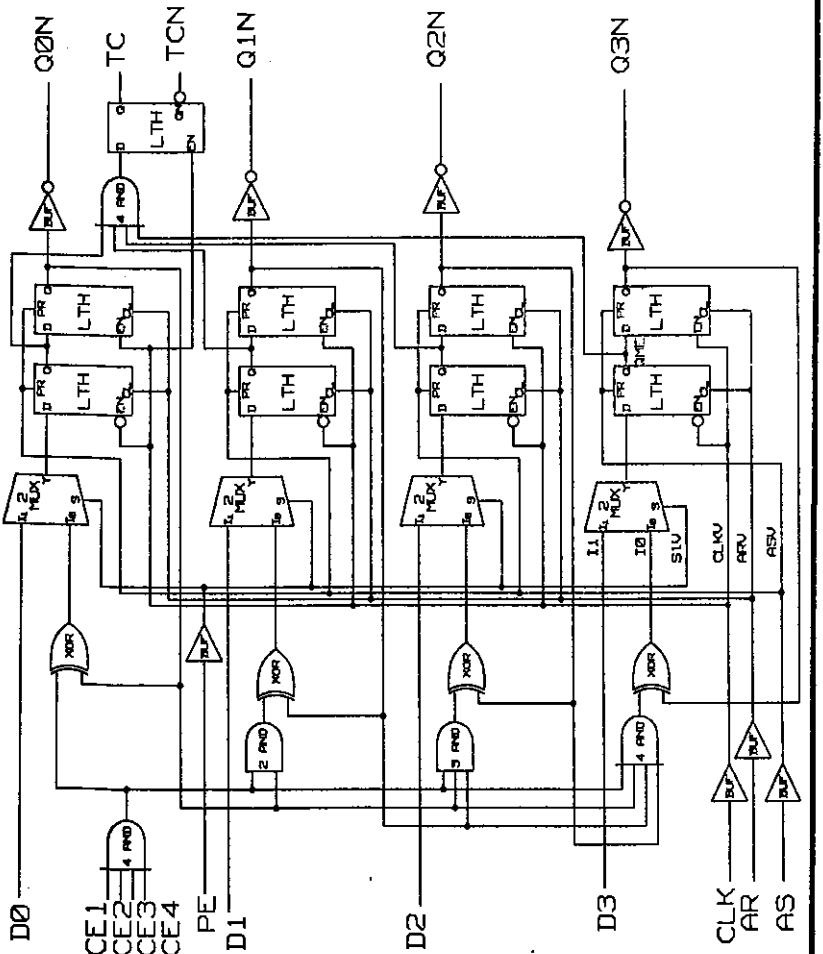
AR	AS	PE	CE1N	CE2N	CE3N	CLK	MODE
0	0	1	X	X	X	R	LOAD
0	0	0	1	X	X	R	HOLD
0	0	0	X	1	X	R	HOLD
0	0	0	X	X	1	R	HOLD
0	0	0	0	0	0	R	COUNT
1	0	X	X	X	X	X	RESET TO 0
0	1	X	X	X	X	X	SET TO 1
1	1	X	X	X	X	X	UNKNOWN



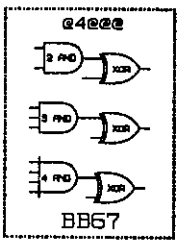
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

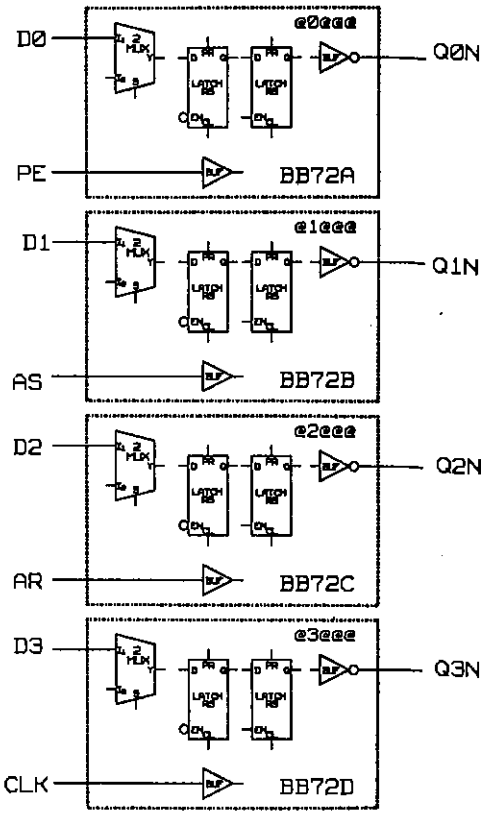


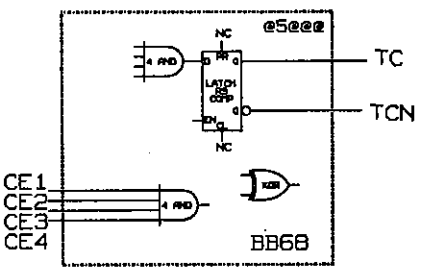
Q5000 CTR02
FUNCTIONAL DRAWING



Q5000 CTR02
BUILDING BLOCKS







PREPLACEMENTS MUST USE THIS CELL ARRANGEMENT:

BB72A @0@@@	BB72B @1@@@	BB72C @2@@@	BB72D @3@@@	BB67 @4@@@	BB68 @5@@@

AMCC Q5000 MACRO SUMMARY - CTRxx (804)

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

detail

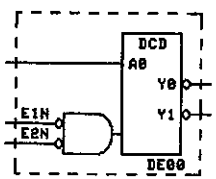
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL OR +5V REF ECL PATH,
ELSE I = IEE

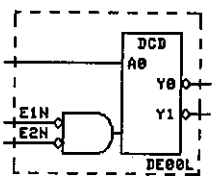
DE00 0.5 L cell 1:2 DECODER LOW with DUAL LOW-EN

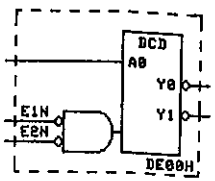
		S	L	H	
Tpd ++	A0->Y0	0.44	0.40	0.29	ns
--	A0->Y0	0.32	0.35	0.25	ns
Tpd +-	A0->Y1	0.37	0.42	0.30	ns
-+	A0->Y1	0.51	0.45	0.28	ns
Tpd	A0=0				
++	E1N,E2N->Y0	0.60	0.56	0.43	ns
--	E1N,E2N->Y0	0.52	0.56	0.40	ns
Tpd	A0=1				
++	E1N,E2N->Y1	0.70	0.64	0.47	ns
--	E1N,E2N->Y1	0.57	0.61	0.43	ns
I		1.17	0.81	1.62	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

EITHER E1N OR E2N MUST BE DRIVEN BY A MACRO

E1N	E2N	A0	Y1	Y0
0	0	0	1	0
0	0	1	0	1
X	1	X	1	1
1	X	X	1	1







ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL OR +5V REF ECL PATH,
ELSE I = IEE

DE21 L cell 2:4 DECODER WITH LOW-ENABLE, OUTPUT LOW

		S	L	H	
Tpd	++ A->Y0	0.54	0.49	0.35	ns
	-- A->Y0	0.38	0.43	0.29	ns
	+- A->Y1	0.36	0.40	0.29	ns
	-+ A->Y1	0.38	0.34	0.23	ns
	++ A->Y2	0.54	0.49	0.35	ns
	-- A->Y2	0.38	0.43	0.29	ns
	+- A->Y3	0.35	0.39	0.29	ns
	-+ A->Y3	0.38	0.33	0.22	ns
Tpd	++ B->Y0	0.69	0.64	0.48	ns
	-- B->Y0	0.57	0.61	0.40	ns
	++ B->Y1	0.60	0.55	0.44	ns
	-- B->Y1	0.53	0.57	0.39	ns
	+- B->Y2	0.57	0.61	0.51	ns
	-+ B->Y2	0.69	0.62	0.38	ns
	+- B->Y3	0.54	0.58	0.48	ns
	-+ B->Y3	0.58	0.53	0.34	ns
Tpd	++ EN->Y0,Y2	0.77	0.71	0.58	ns
	-- EN->Y0	0.80	0.85	0.53	ns
	++ EN->Y1	0.67	0.64	0.55	ns
	-- EN->Y1	0.78	0.82	0.53	ns
	-- EN->Y2	0.81	0.85	0.54	ns
	++ EN->Y3	0.68	0.64	0.56	ns
	-- EN->Y3	0.79	0.83	0.53	ns
I		2.12	1.40	2.80	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

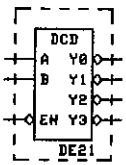
EN MUST BE DRIVEN BY A MACRO
B MUST BE DRIVEN BY A MACRO

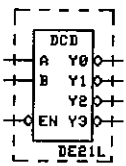
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL OR +5V REF ECL PATH,
ELSE I = IEE

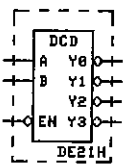
DE21 L cell 2:4 DECODER WITH LOW-ENABLE, OUTPUT LOW

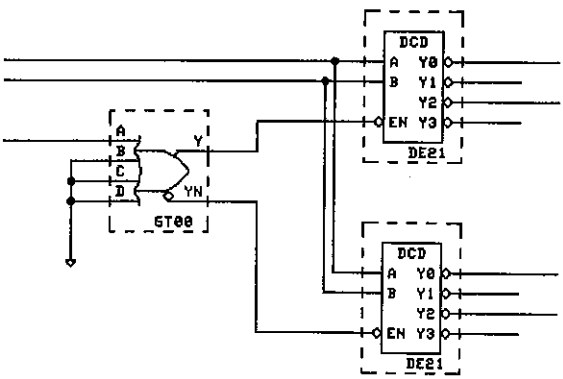
$Y0 = EN+B+A \quad Y1 = EN+B+\bar{A} \quad Y2 = EN+\bar{B}+A \quad Y3 = EN+\bar{B}+\bar{A}$

EN	B	A	Y0	Y1	Y2	Y3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0









3:8 DECODER

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL OR +5V REF ECL PATH,
ELSE I = IEE

DE24 L cell 2:4 DECODER, HIGH ENABLE, OUTPUT LOW

		S	L	H	
Tpd	++A->Y0	0.49	0.43	0.32	ns
	--A->Y0	0.33	0.37	0.27	ns
	+-A->Y1	0.36	0.40	0.30	ns
	-+A->Y1	0.40	0.36	0.25	ns
	++A->Y2	0.47	0.43	0.32	ns
	--A->Y2	0.33	0.37	0.27	ns
	+-A->Y3	0.36	0.40	0.30	ns
	-+A->Y3	0.39	0.35	0.24	ns
	++B->Y0	0.62	0.57	0.46	ns
	--B->Y0	0.56	0.59	0.40	ns
	++B->Y1	0.39	0.63	0.24	ns
	--B->Y1	0.59	0.34	0.41	ns
	+-B->Y2	0.71	0.75	0.58	ns
	-+B->Y2	0.60	0.55	0.34	ns
	+-B->Y3	0.57	0.61	0.51	ns
	-+B->Y3	0.36	0.32	0.34	ns
	+-E->Y0	0.75	0.79	0.68	ns
	-+E->Y2	0.71	0.66	0.44	ns
	+-E->Y1	0.76	0.80	0.69	ns
	-+E->Y3	0.79	0.73	0.44	ns
I		2.12	1.40	2.79	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.040	0.040	0.020	ns/LU
	FALLING	0.040	0.080	0.040	ns/LU

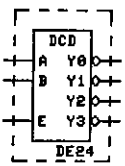
E MUST BE DRIVEN BY A MACRO
B MUST BE DRIVEN BY A MACRO

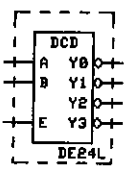
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL OR +5V REF ECL PATH,
ELSE I = IEE

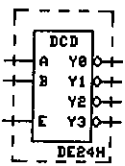
DE24 L cell 2:4 DECODER, HIGH ENABLE, OUTPUT LOW

$Y0 = \bar{E}+B+A \quad Y1 = \bar{E}+B+\bar{A} \quad Y2 = \bar{E}+\bar{B}+A \quad Y3 = \bar{E}+\bar{B}+\bar{A}$

E	B	A	Y0	Y1	Y2	Y3
1	0	0	0	1	1	1
1	0	1	1	0	1	1
1	1	0	1	1	0	1
1	1	1	1	1	1	0
0	X	X	1	1	1	1







ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

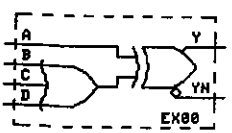
EX00 0.5 L cell 3-INPUT OR-EXOR/EXNOR

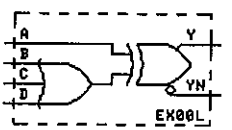
		S	L	H	
Tpd	++ A->Y	0.67	0.61	0.40	ns
	-- A->Y	0.40	0.46	0.31	ns
	+- A->Y	0.45	0.53	0.37	ns
	-+ A->Y	0.70	0.62	0.36	ns
Tpd	+- A->YN	0.44	0.50	0.36	ns
	-+ A->YN	0.61	0.54	0.32	ns
	++ A->YN	0.62	0.52	0.35	ns
	-- A->YN	0.37	0.42	0.29	ns
Tpd	++ B,C,D->Y	0.89	0.81	0.57	ns
	-- B,C,D->Y	0.70	0.76	0.47	ns
	+- B,C,D->Y	0.66	0.72	0.56	ns
	-+ B,C,D->Y	0.94	0.86	0.49	ns
Tpd	+- B,C,D->YN	0.63	0.69	0.54	ns
	-+ B,C,D->YN	0.87	0.79	0.45	ns
	++ B,C,D->YN	0.79	0.73	0.53	ns
	-- B,C,D->YN	0.66	0.71	0.45	ns
I		1.17	0.81	1.62	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

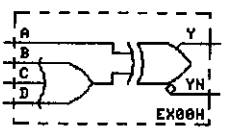
EITHER B, C OR D MUST BE DRIVEN BY A MACRO

$$Y = A \oplus (B + C + D)$$

$$YN = \overline{A \oplus (B + C + D)}$$







ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

EX03 L cell 5-INPUT OR, 2-INPUT EXNOR

		S	L	H	
Tpd	++A->YN	0.76	0.64	0.40	ns
	-+A->YN	0.65	0.57	0.31	ns
	+-A->YN	0.42	0.47	0.34	ns
	--A->YN	0.47	0.52	0.32	ns
Tpd	++B->YN	1.00	0.90	0.62	ns
	-+B->YN	0.92	0.83	0.44	ns
	+-B->YN	0.72	0.79	0.62	ns
	--B->YN	0.71	0.76	0.58	ns
Tpd	++C->YN	1.00	0.90	0.62	ns
	-+C->YN	0.92	0.83	0.44	ns
	+-C->YN	0.69	0.75	0.60	ns
	--C->YN	0.73	0.80	0.48	ns
Tpd	++D,E,F->YN	1.01	0.91	0.61	ns
	-+D,E,F->YN	0.90	0.81	0.45	ns
	+-D,E,F->YN	0.69	0.75	0.60	ns
	--D,E,F->YN	0.77	0.83	0.48	ns
I		0.81	0.63	1.26	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

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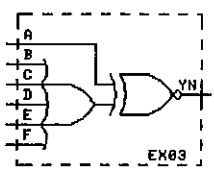
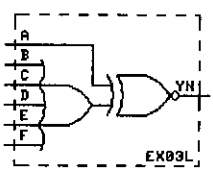
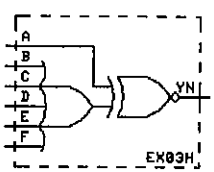
* EITHER B, C, D, E OR F MUST BE DRIVEN BY A MACRO

$$YN = \overline{A \oplus (B + C + D + E + F)}$$







ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

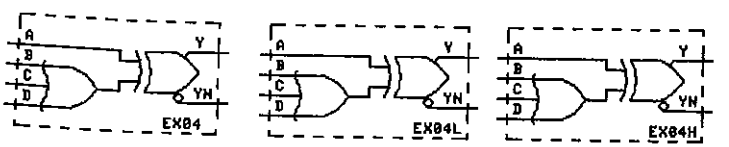
EX04 0.5 L cell 3-INPUT OR-EXOR/EXNOR

		S	L	H	
Tpd	++ A->Y	0.63	0.54	0.32	ns
	-- A->Y	0.38	0.43	0.28	ns
	+- A->Y	0.43	0.49	0.33	ns
	-+ A->Y	0.60	0.53	0.26	ns
Tpd	+- A->YN	0.43	0.50	0.33	ns
	-+ A->YN	0.61	0.54	0.27	ns
	++ A->YN	0.64	0.55	0.32	ns
	-- A->YN	0.38	0.43	0.28	ns
Tpd	++ B,C,D->Y	0.84	0.76	0.44	ns
	-- B,C,D->Y	0.66	0.72	0.48	ns
	+- B,C,D->Y	0.63	0.68	0.46	ns
	-+ B,C,D->Y	0.87	0.79	0.43	ns
Tpd	+- B,C,D->YN	0.63	0.69	0.46	ns
	-+ B,C,D->YN	0.87	0.79	0.46	ns
	++ B,C,D->YN	0.84	0.76	0.43	ns
	-- B,C,D->YN	0.66	0.71	0.47	ns
I		1.17	0.81	1.62	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

EITHER B, C OR D MUST BE DRIVEN BY A MACRO

$$Y = A \oplus (B + C + D)$$

$$YN = \overline{A \oplus (B + C + D)}$$



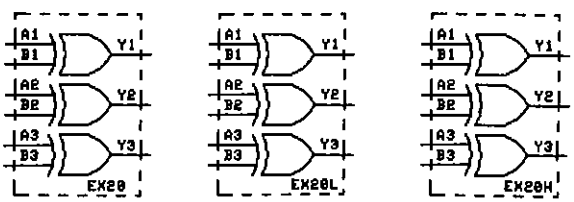
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

EX20 L cell TRIPLE 2-INPUT EXOR

		S	L	H	
Tpd	++A1->Y1,A3->Y3	0.62	0.54	0.35	ns
	+-A1->Y1,A3->Y3	0.42	0.47	0.33	ns
	-+A1->Y1,A3->Y3	0.60	0.53	0.31	ns
	--A1->Y1,A3->Y3	0.37	0.42	0.29	ns
Tpd	++B1->Y1,B3->Y3	0.77	0.72	0.53	ns
	+-B1->Y1,B3->Y3	0.62	0.67	0.53	ns
	-+B1->Y1,B3->Y3	0.83	0.75	0.43	ns
	--B1->Y1,B3->Y3	0.60	0.65	0.43	ns
Tpd	++A2->Y2	0.74	0.62	0.36	ns
	+-A2->Y2	0.50	0.57	0.36	ns
	-+A2->Y2	0.84	0.75	0.41	ns
	--A2->Y2	0.39	0.45	0.30	ns
Tpd	++B2->Y2	0.97	0.87	0.61	ns
	+-B2->Y2	0.70	0.77	0.51	ns
	-+B2->Y2	1.00	0.91	0.57	ns
	--B2->Y2	0.69	0.76	0.47	ns
I		2.43	1.89	3.78	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

B1, B2, B3 - EACH MUST BE DRIVEN BY A MACRO

Y1 = A1 ⊕ B1
Y2 = A2 ⊕ B2
Y3 = A3 ⊕ B3



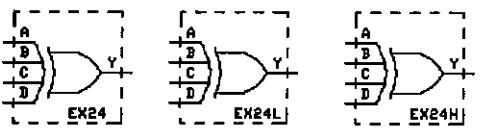
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

EX24 0.5 L cell 4-INPUT EXOR

		S	L	H	
Tpd	++ A,C->Y	1.41	1.20	0.62	ns
	-- A,C->Y	0.59	0.75	0.44	ns
	+- A,C->Y	0.62	0.71	0.48	ns
	-+ A,C->Y	1.20	1.06	0.57	ns
Tpd	++ B,D->Y	1.25	1.05	0.57	ns
	-- B,D->Y	0.56	0.67	0.40	ns
	+- B,D->Y	0.68	0.76	0.49	ns
	-+ B,D->Y	1.35	1.20	0.62	ns
I		1.26	1.08	1.71	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

B, D - EACH MUST BE DRIVEN BY A MACRO

$Y = A \oplus B \oplus C \oplus D$ $\quad \oplus$ = EXOR



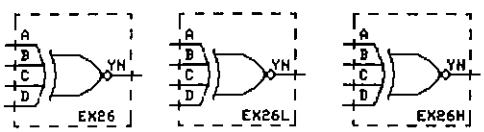
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

EX26 L cell 4-INPUT EXNOR

		S	L	H	
Tpd	+- A->YN	0.69	0.77	0.49	ns
	-+ A->YN	1.27	1.12	0.61	ns
	-- A->YN	0.55	0.67	0.41	ns
	++ A->YN	1.27	1.11	0.62	ns
Tpd	+- B->YN	0.89	1.02	0.66	ns
	-+ B->YN	1.51	1.29	0.75	ns
	-- B->YN	0.86	0.99	0.62	ns
	++ B->YN	1.47	1.29	0.78	ns
Tpd	+- C->YN	0.66	0.77	0.51	ns
	-+ C->YN	1.23	1.08	0.60	ns
	-- C->YN	0.61	0.73	0.44	ns
	++ C->YN	1.31	1.15	0.63	ns
Tpd	+- D->YN	0.89	1.02	0.66	ns
	-+ D->YN	1.45	1.29	0.78	ns
	-- D->YN	0.82	0.95	0.63	ns
	++ D->YN	1.48	1.34	0.79	ns
I		1.26	1.08	1.71	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

B, D - EACH MUST BE DRIVEN BY A MACRO

$$YN = \overline{A \oplus B \oplus C \oplus D}$$



AMCC Q5000 MACRO SUMMARY - EXxx

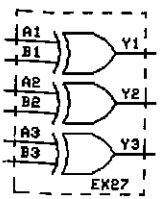
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

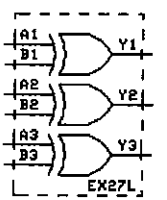
EX27 L cell TRIPLE 2-INPUT EXOR

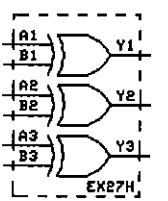
		S	L	H	
Tpd	++A1->Y1,A2->Y2, A3->Y3	0.62	0.54	0.30	ns
	+-A1->Y1,A2->Y2, A3->Y3	0.42	0.47	0.31	ns
	-+A1->Y1,A2->Y2, A3->Y3	0.60	0.53	0.26	ns
	--A1->Y1,A2->Y2, A3->Y3	0.37	0.42	0.27	ns
Tpd	++B1->Y1,B2->Y2, B3->Y3	0.82	0.74	0.43	ns
	+-B1->Y1,B2->Y2, B3->Y3	0.62	0.67	0.45	ns
	-+B1->Y1,B2->Y2, B3->Y3	0.83	0.75	0.40	ns
	--B1->Y1,B2->Y2, B3->Y3	0.60	0.65	0.44	ns
I		2.43	1.89	3.78	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

B1, B2, B3 - EACH MUST BE DRIVEN BY A MACRO

Y1 = A1 ⊕ B1
Y2 = A2 ⊕ B2
Y3 = A3 ⊕ B3







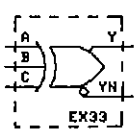
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

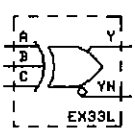
EX33 0.5 L cell 3-INPUT EXOR/EXNOR

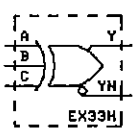
		S	L	H	
Tpd	++ A->Y	0.84	0.72	0.33	ns
	+- A->YN	0.40	0.45	0.31	ns
	-- A->Y	0.45	0.50	0.29	ns
	-+ A->YN	0.53	0.47	0.22	ns
	+- A->Y	0.40	0.45	0.31	ns
	++ A->YN	0.84	0.72	0.33	ns
	-+ A->Y	0.54	0.47	0.22	ns
	-- A->YN	0.45	0.50	0.29	ns
	++ B->Y	0.81	0.71	0.43	ns
	+- B->YN	0.70	0.75	0.49	ns
	-- B->Y	0.63	0.68	0.48	ns
	-+ B->YN	0.88	0.80	0.44	ns
	+- B->Y	0.67	0.72	0.49	ns
	-- B->YN	0.81	0.72	0.43	ns
	-+ B->Y	0.88	0.79	0.44	ns
	-- B->YN	0.63	0.69	0.48	ns
	++ C->Y	1.01	0.92	0.60	ns
	+- C->YN	0.86	0.91	0.67	ns
	-- C->Y	0.87	0.93	0.53	ns
	-+ C->YN	1.05	0.96	0.46	ns
	+- C->Y	0.84	0.89	0.67	ns
	++ C->YN	1.01	0.92	0.60	ns
	-+ C->Y	1.04	0.95	0.46	ns
	-- C->YN	0.88	0.93	0.53	ns
I		1.40	1.04	2.07	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.040	0.040	0.020	ns/LU
	FALLING	0.040	0.080	0.040	ns/LU

B, C - EACH MUST BE DRIVEN BY A MACRO

$Y = A \oplus B \oplus C$ $\qquad YN = \overline{A \oplus B \oplus C}$







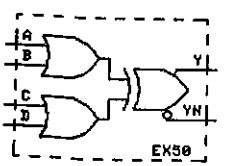
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

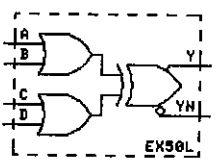
EX50 0.5 L cell 2-TERM, 2-INPUT OR-EXOR/EXNOR

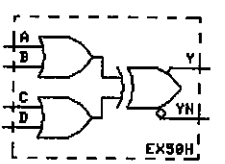
	S	L	H	
Tpd (C + D = 0)				
++ A,B->Y	0.89	0.79	0.49	ns
-- A,B->Y	0.57	0.65	0.38	ns
+- A,B->YN	0.48	0.53	0.39	ns
-+ A,B->YN	0.76	0.67	0.35	ns
Tpd (C + D = 1)				
+- A,B->Y	0.54	0.61	0.42	ns
-+ A,B->Y	0.86	0.75	0.42	ns
++ A,B->YN	0.93	0.80	0.46	ns
-- A,B->YN	0.47	0.53	0.35	ns
Tpd (A + B = 0)				
++ C,D->Y	1.14	1.03	0.68	ns
-- C,D->Y	1.07	1.16	0.67	ns
+- C,D->YN	1.07	1.15	0.75	ns
-+ C,D->YN	1.10	0.99	0.53	ns
Tpd (A + B = 1)				
+- C,D->Y	0.78	0.85	0.63	ns
-+ C,D->Y	1.16	1.01	0.56	ns
++ C,D->YN	1.08	1.00	0.63	ns
-- C,D->YN	0.79	0.90	0.55	ns
I	1.17	0.81	1.62	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU

EITHER C OR D MUST BE DRIVEN BY A MACRO

$Y = (A + B) \oplus (C + D)$ $YN = \overline{(A + B) \oplus (C + D)}$







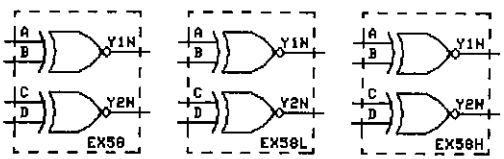
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

EX58 0.5 L cell DUAL 2-INPUT EXNOR

		S	L	H	
Tpd	++ A->Y1N	0.62	0.53	0.35	ns
	+- A->Y1N	0.42	0.47	0.33	ns
	-+ A->Y1N	0.60	0.53	0.31	ns
	-- A->Y1N	0.37	0.42	0.29	ns
Tpd	++ B->Y1N	0.82	0.74	0.49	ns
	+- B->Y1N	0.62	0.67	0.49	ns
	-+ B->Y1N	0.83	0.75	0.48	ns
	-- B->Y1N	0.61	0.66	0.48	ns
Tpd	++ C->Y2N	0.62	0.54	0.35	ns
	+- C->Y2N	0.39	0.44	0.32	ns
	-+ C->Y2N	0.55	0.48	0.28	ns
	-- C->Y2N	0.37	0.42	0.29	ns
Tpd	++ D->Y2N	0.84	0.77	0.50	ns
	+- D->Y2N	0.60	0.66	0.48	ns
	-+ D->Y2N	0.82	0.74	0.46	ns
	-- D->Y2N	0.66	0.72	0.50	ns
I		1.62	1.26	2.07	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

B, D - EACH MUST BE DRIVEN BY A MACRO

$Y1N = \overline{A \oplus B}$ $Y2N = \overline{C \oplus D}$



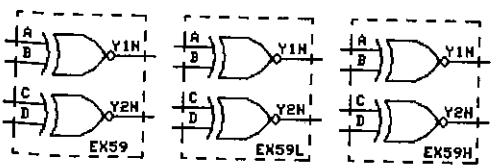
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

EX59 0.5 L cell DUAL 2-INPUT EXNOR

		S	L	H	
Tpd	++ A->Y1N,C->Y2N	0.63	0.53	0.36	ns
	+- A->Y1N,C->Y2N	0.43	0.48	0.35	ns
	-+ A->Y1N,C->Y2N	0.60	0.53	0.31	ns
	-- A->Y1N,C->Y2N	0.37	0.42	0.29	ns
Tpd	++ B->Y1N,D->Y2N	0.82	0.74	0.50	ns
	+- B->Y1N,D->Y2N	0.63	0.68	0.50	ns
	-+ B->Y1N,D->Y2N	0.84	0.76	0.48	ns
	-- B->Y1N,D->Y2N	0.57	0.62	0.48	ns
I		1.62	1.26	2.07	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

B, D - EACH MUST BE DRIVEN BY A MACRO

$Y1N = \overline{\overline{A} \oplus \overline{B}}$ $Y2N = \overline{\overline{C} \oplus \overline{D}}$



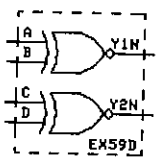
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

EX59D 0.5 L cell DUAL 2-INPUT EXNOR - DRIVER

		DRIVER	
Tpd	++ A->Y1N, C->Y2N	0.40	ns
	+- A->Y1N, C->Y2N	0.31	ns
	-+ A->Y1N, C->Y2N	0.35	ns
	-- A->Y1N, C->Y2N	0.26	ns
Tpd	++ B->Y1N, D->Y2N	0.54	ns
	+- B->Y1N, D->Y2N	0.47	ns
	-+ B->Y1N, D->Y2N	0.52	ns
	-- B->Y1N, D->Y2N	0.45	ns
I		2.79	mA
FAN-OUT LOAD LIMIT:		15	loads
k-FACTOR	RISING	0.02	ns/LU
	FALLING	0.02	ns/LU

B, D - EACH MUST BE DRIVEN BY A MACRO

$Y1N = \overline{A \oplus B}$ $Y2N = \overline{C \oplus D}$



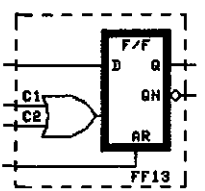
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

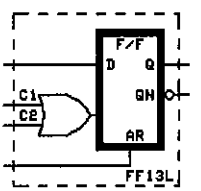
FF13 L cell D F/F WITH ASYNC. RESET, Q, QN

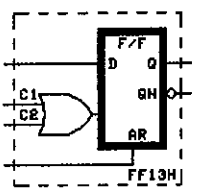
	S	L	H	
Tpd ++ C1,C2->Q	1.19	1.06	0.63	ns
+- C1,C2->Q	0.86	0.93	0.69	ns
Tpd +- C->QN	0.82	0.88	0.66	ns
++ C->QN	0.96	0.87	0.57	ns
Tpd +- AR->Q	0.96	1.06	0.79	ns
Tpd ++ AR->QN	1.23	1.10	0.79	ns
Tsu (D)	1.50	1.50	1.50	ns min
Th (D)	0.00	0.00	0.00	ns min
Trec	2.20	2.20	2.20	ns min
PW(C1,C2)	2.38	3.33	1.39	ns min
PW(AR)	2.38	3.33	1.39	ns min
I	2.07	1.71	2.75	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU

EITHER C1 OR C2 MUST BE DRIVEN BY A MACRO
AR MUST BE DRIVEN BY A MACRO

AR	D	C1+C2	Qn+1	QNn+1	
0	DATA	0	Qn	QNn	
0	DATA	1	Qn	QNn	
1	X	X	0	1	ASYNC. RESET
0	DATA	R	DATA	$\overline{DATA}$	







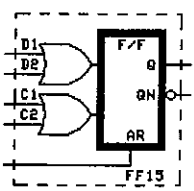
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

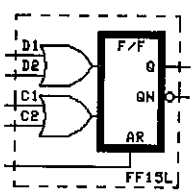
FF15 L cell D F/F WITH ASYNC.RESET, GATED CLOCK Q, QN

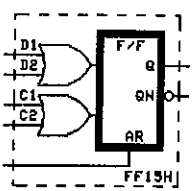
	S	L	H	
Tpd ++ C1,C2->Q	1.19	1.06	0.63	ns
+- C1,C2->Q	0.85	0.92	0.68	ns
Tpd ++ C1,C2->QN	0.82	0.88	0.66	ns
+- C1,C2->QN	0.98	0.88	0.59	ns
Tpd +- AR->Q	0.96	1.06	0.79	ns
Tpd ++ AR->QN	1.23	1.10	0.79	ns
Tsu (D1,D2)	1.40	1.40	1.40	ns min
Th (D1,D2)	-0.20	-0.20	-0.20	ns min
Trec	2.50	2.50	2.50	ns min
PW (C1,C2,AR)	2.38	3.33	1.39	ns min
I	2.07	1.71	2.75	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU

EITHER C1 OR C2 MUST BE DRIVEN BY A MACRO
AR MUST BE DRIVEN BY A MACRO

D1	D2	C1	C2	AR	Qn+1	QNn+1
X	X	0	0	0	Qn	QNn
X	X	X	1	0	Qn	QNn
X	X	1	X	0	Qn	QNn
1	X	R	0	0	1	0
X	1	R	0	0	1	0
1	X	0	R	0	1	0
X	1	0	R	0	1	0
0	0	R	0	0	0	1
0	0	0	R	0	0	1
X	X	X	X	1	0	1







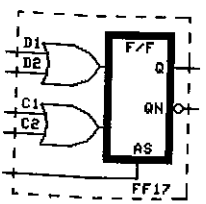
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

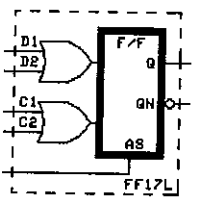
FF17 L cell D F/F WITH ASYNC.SET, GATED CLOCK Q, QN

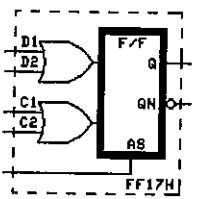
		S	L	H	
Tpd	++ C1,C2->Q	0.88	0.79	0.53	ns
	+- C1,C2->Q	0.80	0.87	0.62	ns
	++ C1,C2->QN	1.30	1.16	0.68	ns
	+- C1,C2->QN	0.93	1.02	0.74	ns
	++ AS->Q	1.12	1.03	0.74	ns
	+- AS->QN	1.02	1.13	0.82	ns
Tsu	(D1,D2)	1.30	1.30	1.30	ns min
Th	(D1,D2)	-0.20	-0.20	-0.20	ns min
Trec		2.20	2.20	2.20	ns min
PW	(C1,C2,AS)	2.38	3.33	1.39	ns min
I		2.07	1.71	2.52	mA
FAN-OUT LOAD LIMIT		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

* EITHER C1 OR C2 MUST BE DRIVEN BY A MACRO AS MUST BE DRIVEN BY A MACRO
AS MUST BE DRIVEN BY A MACRO

D1	D2	C1	C2	AS	Qn+1	QNn+1
X	X	0	0	0	Qn	QNn
X	X	X	1	0	Qn	QNn
X	X	1	X	0	Qn	QNn
1	X	R	0	0	1	0
X	1	R	0	0	1	0
1	X	0	R	0	1	0
X	1	0	R	0	1	0
0	0	R	0	0	0	1
0	0	0	R	0	0	1
X	X	X	X	1	1	0







ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

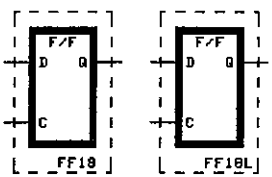
FF18 0.5 L cell D F/F WITH Q OUTPUT

	S	L	H	
Tpd ++ C->Q	1.35	1.23		ns
Tpd +- C->Q	0.94	1.03	N	ns
			O	
Tsu (D)	1.20	1.20	T	ns min
Th (D)	-0.20	-0.20		ns min
PW (C)	2.38	3.33	A	ns min
			V	
I	1.49	1.31	A	mA
			I	
FAN-OUT LOAD LIMIT:	9	4	L	loads
k-FACTOR RISING	0.04	0.04		ns/LU
FALLING	0.04	0.08		ns/LU

C MUST BE DRIVEN BY A MACRO
FOR HIGH-DENSITY APPLICATIONS, CONSULT AMCC

- NO H-OPTION

D	C	Qn+1
X	0	Qn
X	1	Qn
1	R	1
0	R	0



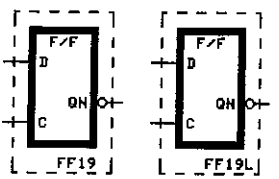
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

FF19 0.5 L cell D F/F WITH QN OUTPUT

	S	L	H	
Tpd ++ C->QN	0.96	0.86		ns
+- C->QN	0.74	0.80	N	ns
			O	
Tsu (D)	1.50	1.50	T	ns min
Th (D)	-0.20	-0.20		ns min
PW (C)	2.38	3.33	A	ns min
			V	
I	1.49	1.31	A	mA
			I	
FAN-OUT LOAD LIMIT:	9	4	L	loads
k-FACTOR RISING	0.04	0.04		ns/LU
FALLING	0.04	0.08		ns/LU

C MUST BE DRIVEN BY A MACRO
FOR HIGH-DENSITY APPLICATIONS, CONSULT AMCC
- NO H-OPTION

D	C	QNn+1
DATA	0	QNn
DATA	1	QNn
DATA	R	DATA

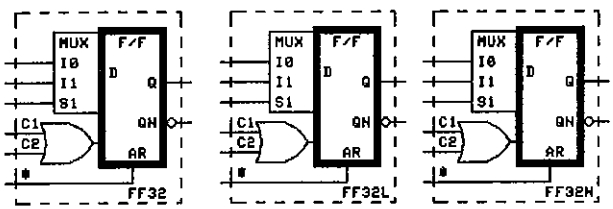


ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

FF32 L cell 2:1 MUX WITH D F/F, ASYNC. RESET, GATED CLOCK,

	S	L	H	
Tpd ++C->Q	1.44	1.30	0.84	ns
+-C->Q	1.14	1.24	0.92	ns
+-C->QN	0.99	1.06	0.82	ns
++C->QN	1.08	0.99	0.71	ns
Tpd +-AR->Q	1.19	1.33	0.91	ns
++AR->QN	1.17	1.07	0.72	ns
Tsu (I0,I1)	1.60	2.10	1.30	ns min
Tsu (S1)	1.80	2.20	1.40	ns min
Th (I0,I1)	0.20	0.20	0.20	ns min
Th (S1)	-0.10	-0.10	-0.10	ns min
Trec	1.30	1.30	1.30	ns min
PW(C1,C2,AR)	2.38	3.33	1.39	ns min
I	2.30	1.94	3.20	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU

AR COUNTS AS 2 LOADS
DATA IS LATCHED ON RISING EDGE OF C1 OR C2
EITHER C1 OR C2 SHOULD BE DRIVEN BY A MACRO
S1, AR - EACH MUST BE DRIVEN BY A MACRO



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

FF32 L cell 2:1 MUX WITH D F/F, ASYNC. RESET, GATED CLOCK,

S1	I0	I1	C1	C2	AR	Qn+1	QNn+1
X	X	X	0	0	0	Qn	QNn
X	X	X	1	X	0	Qn	QNn
X	X	X	X	1	0	Qn	QNn
0	0	X	R	0	0	0	1
0	1	X	R	0	0	1	0
1	X	0	R	0	0	0	1
1	X	1	R	0	0	1	0
0	0	X	0	R	0	0	1
0	1	X	0	R	0	1	0
1	X	0	0	R	0	0	1
1	X	1	0	R	0	1	0
X	0	0	R	0	0	0	1
X	0	0	0	R	0	0	1
X	0	1	R	0	0	UNKNOWN	
X	0	1	0	R	0	UNKNOWN	
X	1	0	R	0	0	UNKNOWN	
X	1	0	0	R	0	UNKNOWN	
X	1	1	R	0	0	1	0
X	1	1	0	R	0	1	0
X	X	X	X	X	1	1	0

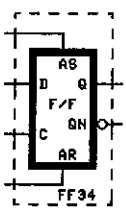
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

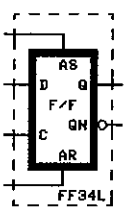
FF34 L cell D FLIP/FLOP WITH AS, AR, COMPLEMENTARY Q, QN

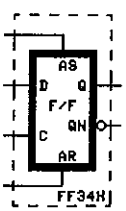
	S	L	H	
Tpd ++C->Q	1.27	1.13	0.71	ns
+-C->Q	0.79	0.89	0.68	ns
++C->QN	1.17	1.04	0.66	ns
+-C->QN	0.77	0.85	0.66	ns
++AS->Q	1.48	1.34	0.86	ns
+-AS->QN	0.90	1.00	0.71	ns
+-AR->Q	0.94	1.05	0.73	ns
++AR->QN	1.32	1.20	0.79	ns
Tsu (D)	1.50	1.50	0.90	ns min
Th (D)	-0.55	-0.55	0.05	ns min
Trec	0.90	0.90	0.90	ns min
PW(C1,C2,AR,AS)	2.86	4.00	1.67	ns min
I	2.74	2.38	3.19	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU

C, AS, AR - EACH MUST BE DRIVEN BY A MACRO

AR	AS	D	C	Qn+1	QNn+1
1	0	X	X	0	1
0	1	X	X	1	0
1	1	X	X	unknown	
0	0	X	0	Qn	QNn
0	0	X	1	Qn	QNn
0	0	0	R	0	1
0	0	1	R	1	0







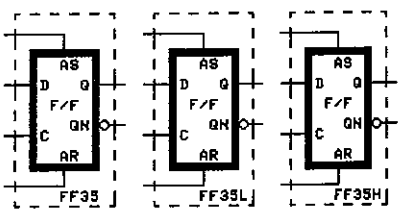
AMCC Q5000 MACRO SUMMARY - FFxx (804)
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

FF35 L cell D FLIP/FLOP WITH AS, AR, COMPLEMENTARY Q, QN

		S	L	H	
Tpd	++C->Q	1.12	0.98	0.51	ns
	+-C->Q	0.77	0.84	0.56	ns
	++C->QN	0.77	0.84	0.51	ns
	+-C->QN	1.12	0.98	0.56	ns
	C = 0				
	++AS->Q	1.39	1.63	0.87	ns
	+-AS->QN	1.82	1.54	0.93	ns
	+-AR->Q	1.39	1.54	0.93	ns
	++AR->QN	1.50	1.74	0.97	ns
	C = 1				
	++AS->Q	1.93	1.74	0.90	ns
	+-AS->QN	1.50	1.61	0.97	ns
	+-AR->Q	1.93	1.67	0.90	ns
	++AR->QN	1.82	1.66	0.87	ns
Tsu (D)		1.20	1.20	0.60	ns min
Th (D)		-0.40	-0.40	0.10	ns min
Trec (AS,AR)		0.90	0.90	0.90	ns min
PW (C1,C2,AR)		2.38	3.33	1.39	ns min
I		3.02	2.66	3.69	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

C, AS, AR - EACH MUST BE DRIVEN BY A MACRO

AR	AS	D	C	Qn+1	QNn+1
1	0	X	X	0	1
0	1	X	X	1	0
1	1	X	X	UNKNOWN	
0	0	X	0	Qn	QNn
0	0	X	1	Qn	QNn
0	0	0	R	0	1
0	0	1	R	1	0

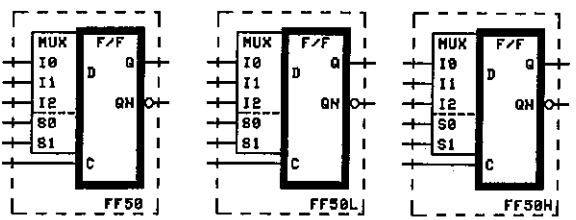


ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

FF50 L cell D F/F WITH 3:1 MUX DATA INPUT, Q, QN

	S	L	H	
Tpd ++C->Q	1.01	0.92	0.65	ns
+-C->Q	0.77	0.83	0.68	ns
Tpd ++C->QN	1.03	0.94	0.66	ns
+-C->QN	0.78	0.84	0.69	ns
Tsu (I0,I1,I2)	1.65	1.30	1.40	ns min
Tsu (S0,S1)	1.95	1.75	1.80	ns min
Th (I0,I1,I2)	-0.35	-0.35	0.20	ns min
Th (S0,S1)	-0.70	-0.70	0.60	ns min
PW(C)	2.38	3.33	1.39	ns min
I	2.29	1.93	3.19	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU

S1, S0 AND C - EACH MUST BE DRIVEN BY A MACRO
DATA LATCHED ON RISING EDGE OF C



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

FF50 L cell D F/F WITH 3:1 MUX DATA INPUT, Q, QN

S0	S1	I0	I1	I2	C	Qn+1	QNn+1
X	X	X	X	X	0	Qn	QNn
X	X	X	X	X	1	Qn	QNn
0	0	0	X	X	R	0	1
0	0	1	X	X	R	1	0
1	0	X	0	X	R	0	1
1	0	X	1	X	R	1	0
0	1	X	X	0	R	0	1
0	1	X	X	1	R	1	0
1	1	X	X	X	R	UNKNOWN	
0	X	1	X	1	R	1	0
0	X	0	X	0	R	0	1
X	0	1	1	X	R	1	0
X	0	0	0	X	R	0	1

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

FF53 L cell 3:1 MUX W/POSITIVE EDGE FLIP/FLOP

	S	L	H	
Tpd ++C->Q	1.31	1.20	0.81	ns
+-C->Q	1.04	1.15	0.85	ns
++C->QN	0.98	0.91	0.68	ns
+-C->QN	0.88	0.96	0.76	ns
Tpd +-AR >Q	0.95	1.05	0.78	ns
++AR >QN	0.93	0.84	0.54	ns
Tsu (I0,I1,I2)	1.60	1.60	1.60	ns min
Tsu (S0,S1)	1.80	1.80	1.70	ns min
Th (I0,I1,I2)	0.30	0.30	0.30	ns min
Th (S0,S1)	-0.40	-0.40	-0.40	ns min
Trec	1.80	1.80	1.70	ns min
PW (C,AR)	2.38	3.33	1.39	ns min
I	2.07	1.71	2.75	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU

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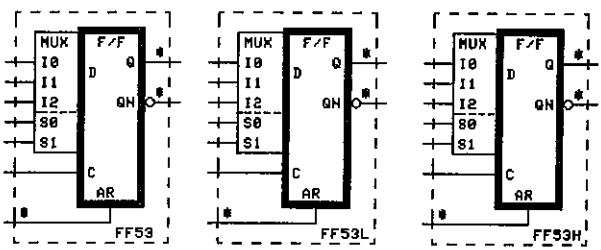
* OUTPUT CANNOT BE WIRE-ORED
  AR, S0, S1 - EACH MUST BE DRIVEN BY A MACRO
  C MUST BE DRIVEN BY A MACRO
* AR COUNTS AS 2 LOADS



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

FF53 L cell 3:1 MUX W/POSITIVE EDGE FLIP/FLOP

AR	S0	S1	I0	I1	I2	C	Qn+1	QNn+1
0	X	X	X	X	X	0	Qn	QNn
0	X	X	X	X	X	1	Qn	QNn
0	0	0	0	X	X	R	0	1
0	0	0	1	X	X	R	1	0
0	1	0	X	0	X	R	0	1
0	1	0	X	1	X	R	1	0
0	0	1	X	X	0	R	0	1
0	0	1	X	X	1	R	1	0
0	1	1	X	X	X	R	UNKNOWN	
0	0	X	1	X	1	R	1	0
0	0	X	0	X	0	R	0	1
0	X	0	1	1	X	R	1	0
0	X	0	0	0	X	R	0	1
1	X	X	X	X	X	X	0	1

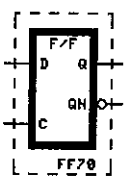
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

FF70 L cell D F/F OPTIMIZED FOR MINIMUM META-STABLE STATE AND MAXIMUM MTBF POSITIVE EDGE TRIGGERED

	S	L	H	
Tpd ++C->Q	0.55			ns
+-C->Q	0.57	N	N	ns
+-C->QN	0.57	O	O	ns
++C->QN	0.55	T	T	ns
Tsu (D)	1.00	A	A	ns min
Th (D)	-0.10	V	V	ns min
PW(C)	1.39	A	A	ns min
		I	I	
I	2.79	L	L	mA
FAN-OUT LOAD LIMIT:	9			loads
k-FACTOR RISING	0.02			ns/LU
FALLING	0.04			ns/LU

C MUST BE DRIVEN BY A MACRO

D	C	Qn+1	QNn+1
X	0	Qn	QNn
X	1	Qn	QNn
1	R	1	0
0	R	0	1



AMCC Q5000 MACRO SUMMARY - FFxx (804)

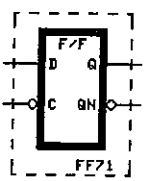
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

FF71 L cell D F/F OPTIMIZED FOR MINIMUM META-STABLE STATE AND MAXIMUM MTBF NEGATIVE EDGE TRIGGERED

	S	L	H	
Tpd -+(C->Q)	0.68			ns
--(C->Q)	0.71	N	N	ns
-+(C->QN)	0.68	O	O	ns
--(C->QN)	0.71	T	T	ns
Tsu	1.30	A	A	ns min
Th	-0.20	V	V	ns min
PW(C)	2.38	A	A	ns min
		I	I	
I	2.79	L	L	mA
FAN-OUT LOAD LIMIT:	9			loads
k-FACTOR RISING	0.02			ns/LU
FALLING	0.04			ns/LU

C MUST BE DRIVEN BY A MACRO

D	C	Qn+1	QNn+1
X	0	Qn	QNn
X	1	Qn	QNn
1	F	1	0
0	F	0	1



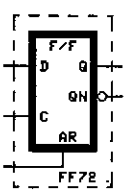
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

FF72 L cell D F/F WITH ASYNC RESET
OPTIMIZED FOR MINIMUM META-STABLE
STATE AND MAXIMUM MTBF POSITIVE
EDGE TRIGGERED

	S	L	H	
Tpd ++C->Q	0.65			ns
+-C->Q	0.62	N	N	ns
++C->QN	0.54	O	O	ns
+-C->QN	0.58	T	T	ns
+-AR->Q	0.76			ns
++AR->QN	0.59			ns
		A	A	
Tsu (D)	0.77	V	V	ns min
Th (D)	-0.07	A	A	ns min
Trec (AR)	2.10	I	I	ns min
Pw(C)	1.39	L	L	ns min
Pw(AR)	1.39			ns min
I	3.24			mA
FAN-OUT LOAD LIMIT:	9			loads
k-FACTOR RISING	0.02			ns/LU
FALLING	0.04			ns/LU

C MUST BE DRIVEN BY A MACRO
AR MUST BE DRIVEN BY A MACRO

AR	D	C	Qn+1	QNn+1
0	DATA	0	Qn	QNn
0	DATA	1	Qn	QNn
1	X	X	0	1
0	DATA	R	DATA	$\overline{DATA}$

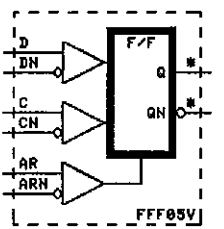


ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

FFF05V 2 L cells VERY HI-SPEED, DIFFERENTIAL D F/F
WITH DIFFERENTIAL ASYNCHRONOUS RESET

		V	
Tpd	++C->Q,QN	0.52	ns
	+-C->Q,QN	0.52	ns
	++AR->Q,QN	0.52	ns
	+-AR->Q,QN	0.52	ns
Tsu	(D)	0.50	ns min
Thd	(D)	0.15	ns min
Trec	(AR-,C+)	1.40	ns min
PW	(C,AR)	0.83	ns min
IEE		6.00	mA
FAN-OUT LOAD LIMIT:		9	loads
INTERCONNECT PINS:		20	internal
k-FACTOR	RISING	0.020	ns/LU
	FALLING	0.020	ns/LU

D,DN MUST BE DIFFERENTIALLY DRIVEN FROM ONE MACRO
C,CN MUST BE DIFFERENTIALLY DRIVEN FROM ONE MACRO
AR,ARN MUST BE DIFFERENTIALLY DRIVEN FROM ONE MACRO
*Q,QN OUTPUTS ARE 1/2 SWING (250mV)
*Q,QN MUST DRIVE A DIFFERENTIAL INPUT PAIR
*Q,QN CANNOT BE WIRE-ORED
*Q,QN CANNOT BE POWERED-DOWN



V MACRO

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

FFF05V 2 L cells VERY HI-SPEED, DIFFERENTIAL D F/F
WITH DIFFERENTIAL ASYNCHRONOUS RESET

D	DN	AR	ARN	C	CN	Qn+1	QNn+1
X	X	1	0	X	X	0	1
X	X	0	0	X	X	UNKNOWN-ILLEGAL	
X	X	1	1	X	X	UNKNOWN-ILLEGAL	
0	1	0	1	R	F	0	1
1	0	0	1	R	F	1	0
0	0	0	1	R	F	UNKNOWN-ILLEGAL	
1	1	0	1	R	F	UNKNOWN-ILLEGAL	
X	X	0	1	1	0	Qn	QNn
X	X	0	1	0	1	Qn	QNn
X	X	0	1	0	0	UNKNOWN-ILLEGAL	
X	X	0	1	1	1	UNKNOWN-ILLEGAL	

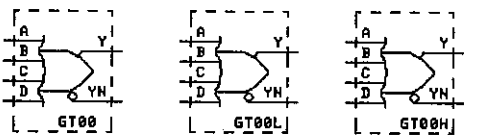
AMCC Q5000 MACRO SUMMARY - GTxx (804)

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT00 0.5 L cell 4-INPUT OR/NOR

		S	L	H	
Tpd ++	A,B,C,D->Y	0.49	0.45	0.33	ns
Tpd --	A,B,C,D->Y	0.41	0.45	0.29	ns
Tpd -+	A,B,C,D->YN	1.00	0.88	0.44	ns
Tpd +-	A,B,C,D->YN	0.55	0.62	0.43	ns
I		0.93	0.59	1.13	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

$Y = A + B + C + D$ $\qquad YN = \overline{A + B + C + D}$



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

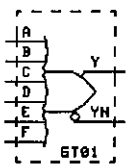
GT01 L cell 6-INPUT OR/NOR

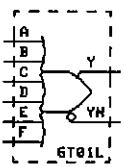
		S	L	H	
Tpd ++ A,B,C,D,E,F->Y		0.95	0.86	0.58	ns
Tpd -- A,B,C,D,E,F->Y		0.64	0.71	0.37	ns
Tpd +- A,B,C,D,E,F->YN		0.60	0.53	0.27	ns
Tpd -+ A,B,C,D,E,F->YN		0.47	0.51	0.43	ns
I		1.40	1.04	2.07	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

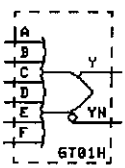
A,B,C - AT LEAST ONE MUST BE DRIVEN BY A MACRO
D,E,F - AT LEAST ONE MUST BE DRIVEN BY A MACRO

$Y = A + B + C + D + E + F$

$YN = \overline{A + B + C + D + E + F}$





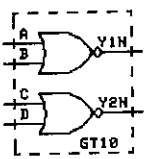


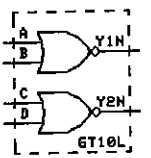
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

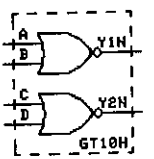
GT10 0.5 L cell DUAL 2-INPUT NOR

	S	L	H	
Tpd -+ A,B->Y1N; C,D->Y2N	0.60	0.53	0.31	ns
Tpd +- A,B->Y1N; C,D->Y2N	0.41	0.46	0.33	ns
I	1.17	0.81	1.62	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU

$Y1N = \overline{A + B}$ $Y2N = \overline{C + D}$





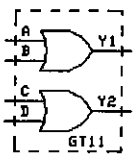


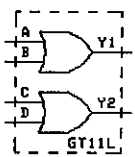
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

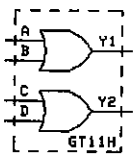
GT11 0.5 L cell DUAL 2-INPUT OR

		S	L	H	
Tpd ++ A,B->Y1,C,D->Y2		0.46	0.42	0.31	ns
Tpd -- A,B->Y1,C,D->Y2		0.34	0.38	0.26	ns
I		1.15	0.79	1.60	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

Y1 = A + B Y2 = C + D







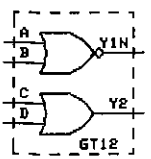
AMCC Q5000 MACRO SUMMARY - GTxx (804)

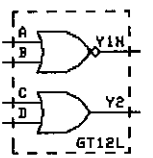
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

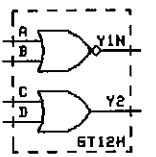
GT12 0.5 L cell 2-INPUT NOR; 2-INPUT OR

		S	L	H	
Tpd -+ A,B->Y1N		0.60	0.46	0.31	ns
Tpd +- A,B->Y1N		0.41	0.53	0.33	ns
Tpd ++ C,D->Y2		0.46	0.43	0.31	ns
Tpd -- C,D->Y2		0.34	0.38	0.26	ns
I		1.15	0.79	1.60	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

$Y1N = \overline{A + B}$ $Y2 = C + D$





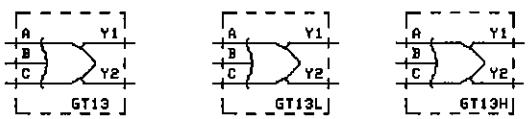


ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT13 0.5 L cell 3-INPUT OR; DUAL OUTPUTS

	S	L	H	
Tpd A,B,C->Y1,Y2				
++ (1 INPUT	0.54	0.51	0.36	ns
-- CHANGING)	0.40	0.45	0.29	ns
Tpd ++ (ANY 2 INPUTS	0.48	0.42	0.29	ns
-- CHANGING)	0.37	0.41	0.30	ns
Tpd ++ (ALL INPUTS	0.40	0.34	0.23	ns
-- CHANGING)	0.34	0.39	0.29	ns
I	0.95	0.59	1.17	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU

Y1 = Y2 = A + B + C



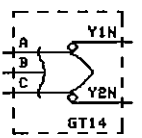
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

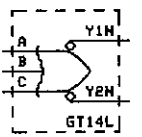
GT14 0.5 L cell 3-INPUT NOR; DUAL OUTPUTS

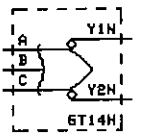
		S	L	H	
Tpd -+ A,B,C->Y1N,Y2N		0.60	0.56	0.32	ns
Tpd +- A,B,C->Y1N,Y2N		0.38	0.41	0.35	ns
I		1.17	0.81	1.62	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

A,B,C - AT LEAST ONE MUST BE DRIVEN BY A MACRO

$$Y1N = Y2N = \overline{A + B}$$







ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

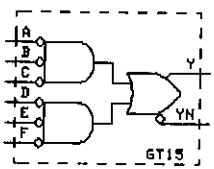
GT15 L cell 2-TERM 3-INPUT OR-AND/NAND

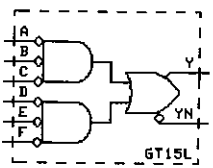
		S	L	H	
Tpd -+ A,B,C->Y		1.09	0.99	0.53	ns
Tpd +- A,B,C->Y		0.62	0.70	0.39	ns
Tpd ++ A,B,C->YN		0.69	0.59	0.31	ns
Tpd -- A,B,C->YN		0.46	0.52	0.35	ns
Tpd -+ D,E,F->Y		1.28	1.14	0.64	ns
Tpd +- D,E,F->Y		0.66	0.74	0.53	ns
Tpd ++ D,E,F->YN		0.92	0.82	0.52	ns
Tpd -- D,E,F->YN		0.86	0.95	0.56	ns
I		1.15	0.79	1.58	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

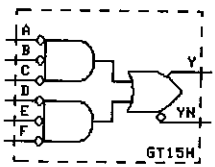
D,E,F - AT LEAST ONE MUST BE DRIVEN BY A MACRO

$$Y = \overline{\bar{A}\bar{B}\bar{C}} + \overline{\bar{D}\bar{E}\bar{F}} = \overline{(A + B + C)(D + E + F)}$$

$$YN = \overline{\bar{A}\bar{B}\bar{C}} + \overline{\bar{D}\bar{E}\bar{F}} = (A + B + C)(D + E + F)$$







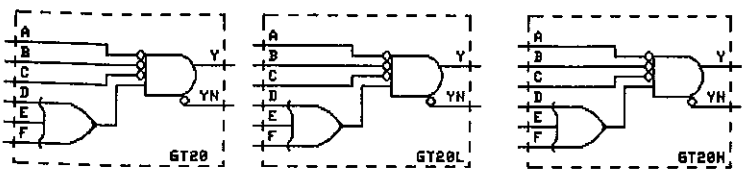
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT20 L cell 3-INPUT OR-AND/NAND WITH 3 LOW-ENABLES

	S	L	H	
Tpd -+ A,B,C->Y	1.30	1.17	0.65	ns
Tpd +- A,B,C->Y	0.72	0.82	0.47	ns
Tpd ++ A,B,C->YN	0.29	0.25	0.17	ns
Tpd -- A,B,C->YN	0.34	0.38	0.28	ns
Tpd ++ D,E,F->Y	1.21	1.07	0.63	ns
Tpd -- D,E,F->Y	0.84	0.96	0.57	ns
Tpd -+ D,E,F->YN	0.67	0.61	0.40	ns
Tpd +- D,E,F->YN	0.53	0.56	0.44	ns
I	1.15	0.79	1.58	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU

D,E,F - AT LEAST ONE MUST BE DRIVEN BY A MACRO

$Y = \overline{A}\overline{B}\overline{C}(D + E + F)$ $YN = A + B + C + \overline{D}\overline{E}\overline{F}$



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

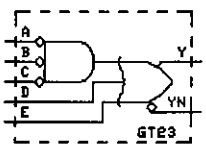
GT23 L cell 3-INPUT NOR - 3-INPUT OR/NOR

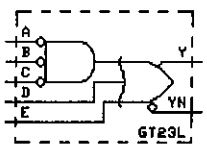
	S	L	H	
Tpd -+ A,B,C->Y	0.65	0.60	0.39	ns
Tpd +- A,B,C->Y	0.50	0.54	0.42	ns
Tpd ++ A,B,C->YN	0.95	0.85	0.53	ns
Tpd -- A,B,C->YN	0.71	0.79	0.50	ns
Tpd ++ D,E->Y	0.35	0.31	0.23	ns
Tpd -- D,E->Y	0.35	0.38	0.28	ns
Tpd -+ D,E->YN	0.93	0.83	0.46	ns
Tpd +- D,E->YN	0.52	0.59	0.37	ns
I	1.17	0.81	1.62	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU

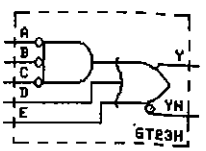
A,B,C - AT LEAST ONE MUST BE DRIVEN BY A MACRO

$Y = (\bar{A}\ \bar{B}\ \bar{C}) + D + E = \overline{(A + B + C)} + D + E$

$YN = \bar{Y}$







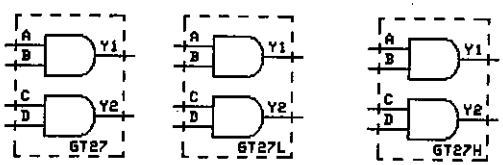
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT27 0.5 L cell DUAL 2-INPUT AND

		S	L	H	
Tpd	++ A->Y1	0.66	0.60	0.38	ns
	-- A->Y1	0.41	0.45	0.31	ns
	++ B->Y1	0.76	0.70	0.48	ns
	-- B->Y1	0.60	0.65	0.49	ns
	++ C->Y2	0.54	0.49	0.33	ns
	-- C->Y2	0.36	0.40	0.27	ns
	++ D->Y2	0.64	0.59	0.44	ns
	-- D->Y2	0.54	0.59	0.45	ns
	TWO INPUTS SWITCHING:				
Tpd	++ A,B->Y1	0.80	0.73	0.50	ns
	-- A,B->Y1	0.53	0.57	0.38	ns
	++ C,D->Y2	0.68	0.62	0.45	ns
	-- C,D->Y2	0.48	0.52	0.35	ns
I		1.62	1.26	2.07	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

B,D - EACH MUST BE DRIVEN BY A MACRO

Y1 = AB Y2 = CD



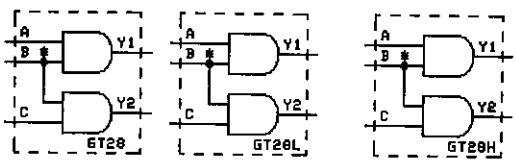
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT28 0.5 L cell DUAL 2-INPUT AND, ONE INPUT COMMON

	S	L	H	
Tpd ++ A->Y1	0.66	0.59	0.38	ns
-- A->Y1	0.41	0.46	0.31	ns
Tpd ++ B->Y1	0.78	0.70	0.49	ns
-- B->Y1	0.66	0.72	0.50	ns
Tpd ++ B->Y2	0.66	0.60	0.45	ns
-- B->Y2	0.61	0.65	0.47	ns
Tpd ++ C->Y2	0.54	0.49	0.33	ns
-- C->Y2	0.36	0.40	0.27	ns
BOTH CHANGING:				
Tpd ++ A,B->Y1	0.81	0.73	0.51	ns
-- A,B->Y1	0.54	0.58	0.39	ns
Tpd ++ B,C->Y2	0.68	0.62	0.46	ns
-- B,C->Y2	0.48	0.53	0.36	ns
I	1.39	1.03	1.84	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU

* B COUNTS AS 1 LOAD
B MUST BE DRIVEN BY A MACRO

Y1 = AB Y2 = BC



AMCC Q5000 MACRO SUMMARY - GTxx (804)

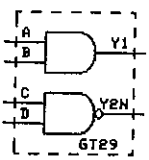
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

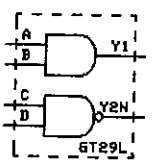
GT29 0.5 L cell 2-INPUT AND, 2-INPUT NAND

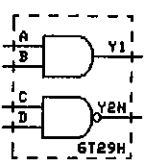
		S	L	H	
Tpd	++ A->Y1	0.54	0.49	0.33	ns
	-- A->Y1	0.36	0.40	0.27	ns
Tpd	++ B->Y1	0.64	0.59	0.44	ns
	-- B->Y1	0.54	0.59	0.45	ns
Tpd	+- C->Y2N	0.34	0.37	0.28	ns
	-+ C->Y2N	0.40	0.36	0.24	ns
Tpd	+- D->Y2N	0.57	0.61	0.47	ns
	-+ D->Y2N	0.61	0.56	0.38	ns
	BOTH CHANGING:				
Tpd	++ A,B->Y1	0.68	0.62	0.45	ns
	-- A,B->Y1	0.48	0.52	0.35	ns
Tpd	++ C,D->Y2N	0.68	0.72	0.53	ns
	-- C,D->Y2N	0.36	0.32	0.19	ns
I		1.62	1.26	2.07	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

* B,D - EACH MUST BE DRIVEN BY A MACRO

$Y1 = AB \qquad Y2N = \overline{C}\,\overline{D} = \overline{C} + \overline{D}$







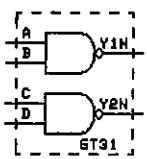
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

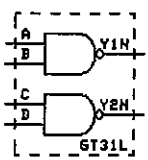
GT31 0.5 L cell DUAL 2-INPUT NAND

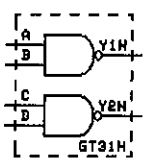
		S	L	H	
Tpd	-+ A->Y1N	0.34	0.30	0.20	ns
	+- A->Y1N	0.32	0.36	0.27	ns
Tpd	-+ B->Y1N	0.71	0.65	0.43	ns
	+- B->Y1N	0.64	0.68	0.49	ns
Tpd	-+ C->Y2N	0.39	0.35	0.24	ns
	+- C->Y2N	0.34	0.37	0.28	ns
Tpd	-+ D->Y2N	0.60	0.55	0.38	ns
	+- D->Y2N	0.57	0.60	0.46	ns
I		1.60	1.26	2.08	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

B,D - EACH MUST BE DRIVEN BY A MACRO

$$Y1N = \overline{AB} = \bar{A} + \bar{B} \qquad Y2N = \overline{CD} = \bar{C} + \bar{D}$$







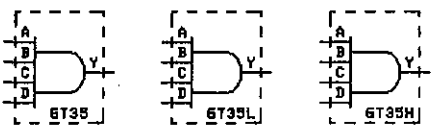
AMCC Q5000 MACRO SUMMARY - GTxx (804)

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT35 L cell 4-INPUT AND

		S	L	H	
Tpd ++	A,B,C->Y	0.90	0.86	0.57	ns
--	A,B,C->Y	0.80	0.84	0.58	ns
Tpd ++	D->Y	0.99	0.95	0.62	ns
--	D->Y	1.04	1.08	0.71	ns
I		1.71	1.53	3.06	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

Y = ABCD



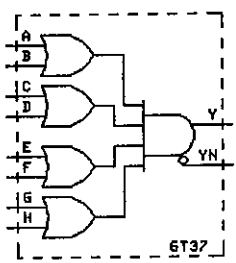
AMCC Q5000 MACRO SUMMARY - GTxx (804)

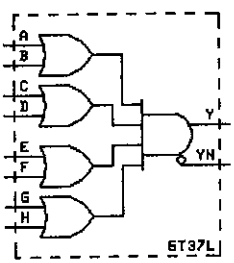
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

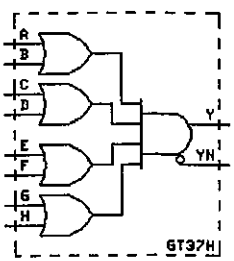
GT37 L cell QUAD 2-INPUT OR - 4-INPUT AND/NAND

	S	L	H	
Tpd ++ A,B,C,D->Y	1.01	0.96	0.64	ns
Tpd -- A,B,C,D->Y	1.12	1.17	0.74	ns
Tpd -+ A,B,C,D->YN	1.26	1.23	0.77	ns
Tpd +- A,B,C,D->YN	0.93	0.97	0.63	ns
Tpd ++ E,F->Y	1.01	0.97	0.63	ns
Tpd -- E,F->Y	1.09	1.14	0.73	ns
Tpd -+ E,F->YN	1.24	1.20	0.76	ns
Tpd +- E,F->YN	0.94	0.98	0.62	ns
Tpd ++ G,H->Y	1.16	1.11	0.71	ns
Tpd -- G,H->Y	1.34	1.40	0.87	ns
Tpd -+ G,H->YN	1.50	1.46	0.93	ns
Tpd +- G,H->YN	1.06	1.10	0.70	ns
I	2.07	1.71	3.42	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU

$Y = (A + B)(C + D)(E + F)(G + H)$ $YN = \bar{Y}$







AMCC Q5000 MACRO SUMMARY - GTxx (804)

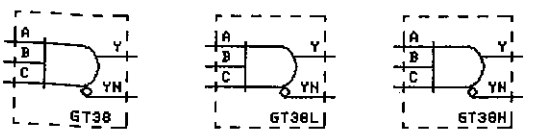
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT38 0.5 L cell 3-INPUT AND/NAND

		S	L	H	
Tpd	++ A->Y	0.75	0.67	0.43	ns
Tpd	-- A->Y	0.47	0.53	0.34	ns
Tpd	-+ A->YN	0.38	0.34	0.22	ns
	+- A->YN	0.34	0.38	0.28	ns
	++ B->Y	0.83	0.74	0.54	ns
	-- B->Y	0.74	0.83	0.49	ns
	-+ B->YN	0.61	0.55	0.34	ns
	+- B->YN	0.48	0.52	0.45	ns
	++ C->Y	1.01	0.92	0.68	ns
	-- C->Y	1.02	1.10	0.62	ns
	-+ C->YN	0.81	0.75	0.45	ns
	+- C->YN	0.65	0.68	0.61	ns
I		1.35	0.99	1.98	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

B,C - EACH MUST BE DRIVEN BY A MACRO

$Y = ABC$ $\qquad YN = \overline{ABC} = \bar{A} + \bar{B} + \bar{C}$



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT43 0.5 L cell DUAL 2-INPUT AND

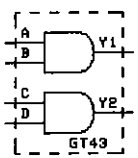
	S	L	H	
Tpd ++ A,B->Y1 (1)	0.63	0.57		ns
-- A,B->Y1	0.38	0.43		ns
Tpd ++ A,B->Y1 (2)	0.94	0.94		ns
-- A,B->Y1	0.25	0.28		ns
Tpd ++ C->Y2 (1)	0.75	0.67		ns
-- C->Y2	0.43	0.49		ns
Tpd ++ D->Y2 (1)	0.74	0.66		ns
-- D->Y2	0.41	0.47		ns
Tpd ++ C,D->Y2 (2)	1.10	1.05		ns
-- C,D->Y2	0.27	0.30		ns
I	1.62	1.26		mA
FAN-OUT LOAD LIMIT:	9	4		loads
k-FACTOR RISING	0.04	0.04		ns/LU
FALLING	0.04	0.08		ns/LU

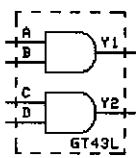
---

* B,D - EACH MUST BE DRIVEN BY A MACRO
(1) INPUTS SWITCHING GREATER THAN OR EQUAL TO 1ns OF EACH OTHER.
(2) INPUTS SWITCHING LESS THAN 1ns OF EACH OTHER.

- NO H-OPTION

Y1 = AB Y2 = CD





ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

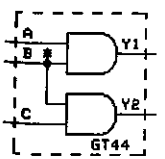
GT44 0.5 L cell DUAL 2-INPUT AND, ONE INPUT COMMON

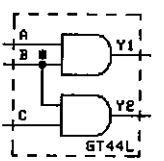
	S	L	H	
(1 INPUT CHANGING)				
Tpd ++ A->Y1	0.74	0.66		ns
-- A->Y1	0.43	0.49		ns
Tpd ++ B->Y1	0.78	0.70		ns
-- B->Y1	0.47	0.52		ns
Tpd ++ B->Y2	0.95	0.85		ns
-- B->Y2	0.58	0.66		ns
Tpd ++ C->Y2	0.92	0.84		ns
-- C->Y2	0.52	0.60		ns
(2 INPUTS CHANGING)				
Tpd ++ A,B->Y1	1.13	1.06		ns
-- A,B->Y1	0.31	0.35		ns
Tpd ++ B,C->Y2	1.38	1.29		ns
-- B,C->Y2	0.34	0.38		ns
I	1.85	1.49		mA
FAN-OUT LOAD LIMIT:	9	4		loads
k-FACTOR RISING	0.04	0.04		ns/LU
FALLING	0.04	0.08		ns/LU

* B COUNTS AS 1 LOAD
  B MUST BE DRIVEN BY A MACRO

• NO H-OPTION

Y1 = AB Y2 = BC





ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT45 0.5 L cell 2-INPUT AND, 2-INPUT NAND

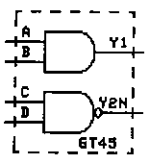
		S	L	H	
Tpd ++	A,B->Y1 (1)	0.85	0.76		ns
--	A,B->Y1	0.47	0.54		ns
++	A,B->Y1 (2)	1.25	1.17		ns
--	A,B->Y1	0.40	0.33		ns
Tpd +-	C->Y2N (1)	0.34	0.38		ns
-+	C->Y2N	0.40	0.36		ns
+-	C->Y2N (2)	0.69	0.73		ns
-+	C->Y2N	0.36	0.31		ns
Tpd +-	D->Y2N (1)	0.57	0.60		ns
-+	D->Y2N	0.61	0.56		ns
I		1.62	1.26		mA
FAN-OUT LOAD LIMIT:		9	4		loads
k-FACTOR	RISING	0.04	0.04		ns/LU
	FALLING	0.04	0.08		ns/LU

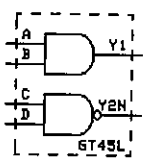
---

* B,D - EACH MUST BE DRIVEN BY A MACRO
(1) INPUTS SWITCHING GREATER THAN OR EQUAL TO 1ns OF EACH OTHER.
(2) INPUTS SWITCHING LESS THAN 1ns OF EACH OTHER.

• NO H-OPTION

$Y1 = AB$ $Y2N = \overline{C}\,\overline{D}$





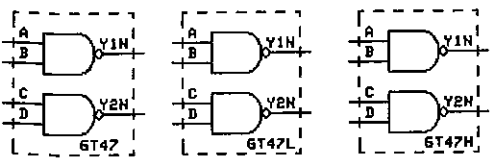
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT47 0.5 L cell DUAL 2-INPUT NAND

		S	L	H	
Tpd +-	A,C->Y1,Y2N	0.34	0.37	0.28	ns
-+	A,C->Y1,Y2N	0.39	0.35	0.24	ns
Tpd +-	B,D->Y1,Y2N	0.57	0.60	0.46	ns
-+	B,D->Y1,Y2N	0.61	0.56	0.39	ns
I		0.81	0.63	0.70	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

B,D - EACH MUST BE DRIVEN BY A MACRO

$Y1N = \overline{AB}$ $Y2N = \overline{CD}$



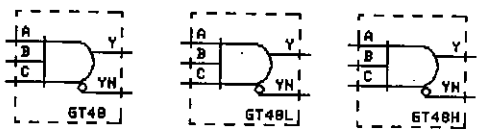
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT48 0.5 L cell 3-INPUT AND/NAND

		S	L	H	
Tpd	++ A->Y	0.75	0.67	0.35	ns
Tpd	-- A->Y	0.47	0.53	0.30	ns
	++ B->Y	0.83	0.74	0.43	ns
	-- B->Y	0.74	0.83	0.46	ns
	++ C->Y	1.01	0.92	0.58	ns
	-- C->Y	1.02	1.10	0.50	ns
	+- A->YN	0.34	0.38	0.26	ns
Tpd	-+ A->YN	0.38	0.34	0.19	ns
	+- B->YN	0.48	0.52	0.41	ns
	-+ B->YN	0.61	0.55	0.35	ns
	+- C->YN	0.65	0.68	0.59	ns
	-+ C->YN	0.81	0.75	0.40	ns
Tpd	++ A,B,C->Y	0.72	0.75	0.62	ns
	-- A,B,C->Y	0.77	0.87	0.62	ns
	+- A,B,C->Y	0.72	0.75	0.62	ns
	-+ A,B,C->Y	0.34	0.30	0.14	ns
I		1.35	0.99	2.07	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

B,C - EACH MUST BE DRIVEN BY A MACRO

$Y = ABC$ $\qquad YN = \overline{ABC} = \bar{A} + \bar{B} + \bar{C}$



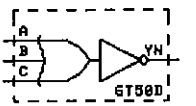
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT50D 0.5 L cell 3-INPUT NOR DRIVER

		DRIVER	
Tpd +- A,B,C->YN		0.39	ns
Tpd -+ A,B,C->YN		0.55	ns
I		1.17	mA
FAN-OUT LOAD LIMIT:		15	loads
k-FACTOR	RISING	0.02	ns/LU
	FALLING	0.02	ns/LU

OUTPUT CANNOT BE WIRE-ORED

$$YN = \overline{A + B + C}$$



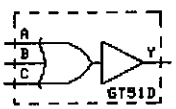
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT51D 0.5 L cell 3-INPUT OR DRIVER

		DRIVER	
Tpd ++ A,B,C->Y		0.34	ns
Tpd -- A,B,C->Y		0.28	ns
I		1.17	mA
FAN-OUT LOAD LIMIT:		15	loads
k-FACTOR	RISING	0.02	ns/LU
	FALLING	0.02	ns/LU

OUTPUT CANNOT BE WIRE-ORED

Y = A + B + C



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT52D 0.5 L cell 2-INPUT NAND DRIVER

		DRIVER	
Tpd	+-A->YN	0.05	ns
	-+A->YN	0.31	ns
Tpd	+-B->YN	0.49	ns
	-+B->YN	0.43	ns
I		1.62	mA
FAN-OUT LOAD LIMIT:		15	loads
k-FACTOR	RISING	0.02	ns/LU
	FALLING	0.02	ns/LU

B MUST BE DRIVEN BY A MACRO
OUTPUT CANNOT BE WIRE-ORED

$$YN = \overline{A}\overline{B}$$

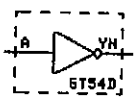
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT54D L cell INVERTING SUPER-DRIVER

		DRIVER	
Tpd +- A->YN		0.32	ns
Tpd -+ A->YN		0.29	ns
I		3.96	mA
FAN-OUT LOAD LIMIT:		25	loads
k-FACTOR	RISING	0.01	ns/LU
	FALLING	0.01	ns/LU

OUTPUT CANNOT BE WIRE-ORED
OUTPUT MAY BE POWERED-DOWN

$YN = \bar{A}$



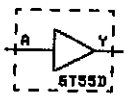
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT55D L cell NON-INVERTING SUPER-DRIVER

		DRIVER	
Tpd ++ A->Y		0.40	ns
Tpd -- A->Y		0.26	ns
I		3.96	mA
FAN-OUT LOAD LIMIT:		25	loads
k-FACTOR	RISING	0.01	ns/LU
	FALLING	0.01	ns/LU

A MUST BE DRIVEN BY A MACRO
OUTPUT CANNOT BE WIRE-ORED

Y = A



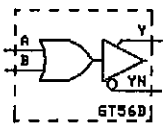
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT56D 0.5 L cell 2-INPUT OR/NOR DRIVER

		DRIVER	
Tpd ++ A,B->Y		0.35	ns
Tpd -- A,B->Y		0.28	ns
Tpd +- A,B->YN		0.38	ns
Tpd -+ A,B->YN		0.46	ns
I		1.89	mA
FAN-OUT LOAD LIMIT:		15	loads
k-FACTOR	RISING	0.02	ns/LU
	FALLING	0.02	ns/LU

OUTPUT CANNOT BE WIRE-ORED
OUTPUT MAY BE POWERED-DOWN

$Y = A + B$ $\qquad$ $YN = \overline{\overline{A} + \overline{B}} = \overline{\overline{A}}\,\overline{\overline{B}}$



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT60 L cell 8-INPUT OR/NOR

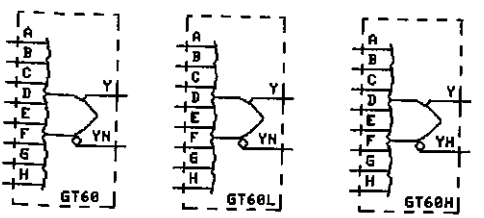
	S	L	H	
Tpd:				
++A,B,C,D,E,F,G,H->Y	0.97	0.88	0.61	ns
--A,B,C,D,E,F,G,H->Y	0.67	0.74	0.39	ns
+-A,B,C,D,E,F,G,H->YN	0.54	0.60	0.50	ns
-+A,B,C,D,E,F,G,H->YN	0.81	0.72	0.35	ns
I	1.62	1.26	2.52	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU

A,B,C - AT LEAST ONE MUST BE DRIVEN BY A MACRO
D,E,F - AT LEAST ONE MUST BE DRIVEN BY A MACRO
G,H - AT LEAST ONE MUST BE DRIVEN BY A MACRO

NOTE: THE ABOVE SPECS ARE FOR 1 INPUT CHANGING.

$Y = A + B + C + D + E + F + G + H$

$YN = \overline{A + B + C + D + E + F + G + H}$

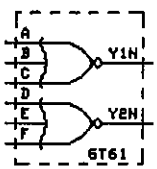


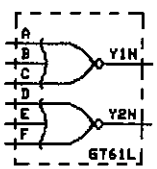
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

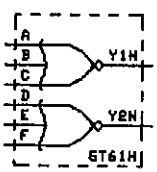
GT61 L cell DUAL 3-INPUT NOR

		S	L	H	
Tpd A,B,C->Y1N					
D,E,F->Y2N					
	+- (ANY 1 INPUT	0.47	0.53	0.37	ns
	-+ CHANGING)	0.80	0.70	0.37	ns
	+- (ANY 2 INPUTS	0.49	0.56	0.35	ns
	-+ CHANGING)	0.92	0.83	0.45	ns
	+- (ANY 3 INPUTS	0.57	0.64	0.37	ns
	-+ CHANGING)	1.03	0.93	0.52	ns
I		1.17	0.81	1.62	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

$Y1N = \overline{A + B + C}$ $Y2N = \overline{D + E + F}$





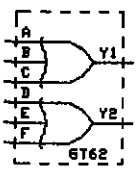


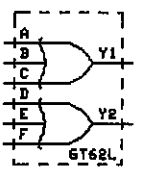
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

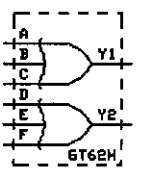
GT62 L cell DUAL 3-INPUT OR

	S	L	H	
Tpd A,B,C->Y1 D,E,F->Y2				
++ (ANY 1 INPUT	0.46	0.43	0.31	ns
-- CHANGING)	0.37	0.41	0.27	ns
++ (ANY 2 INPUTS	0.37	0.34	0.23	ns
-- CHANGING)	0.34	0.38	0.27	ns
++ (ANY 3 INPUTS	0.30	0.26	0.18	ns
-- CHANGING)	0.32	0.35	0.27	ns
I	1.17	0.81	1.62	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.04	0.04	0.02	ns/LU
FALLING	0.04	0.08	0.04	ns/LU

Y1 = A + B + C Y2 = D + E + F







AMCC Q5000 MACRO SUMMARY - GTxx (804)

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT64 L cell DIFFERENTIAL BUFFER W/COMP OUTPUTS
V MACRO TO NON-V MACRO CONVERSION

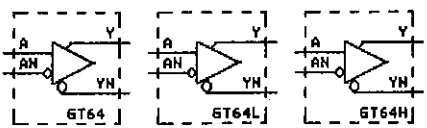
		S	L	H	
Tpd A,AN->Y,YN (--) (++) (-+) (+-)		0.32	0.34	0.24	ns
IEE		0.95	0.58	1.17	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

---

* A,AN - EACH MUST BE DRIVEN BY A MACRO
A,AN - MUST BE DIFFERENTIALLY DRIVEN

Y = A|AN YN = $\overline{A|AN}$
A|AN = differential

A	AN	Y	YN	
0	0	UNKNOWN		ILLEGAL
0	1	0	1	
1	0	1	0	
1	1	UNKNOWN		ILLEGAL



AMCC Q5000 MACRO SUMMARY - GTxx

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

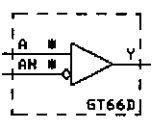
GT66D L cell DIFFERENTIAL 25-LOAD DRIVER
V MACRO TO NON-V MACRO CONVERSION

		D	
Tpd ++	A->Y	0.24	ns
--	A->Y	0.23	ns
Tpd -+	AN->Y	0.24	ns
+-	AN->Y	0.23	ns
I		3.51	mA
k-FACTOR	RISING	0.01	ns/LU
	FALLING	0.01	ns/LU
FAN-OUT LOAD LIMIT:		25	loads

OUTPUT CANNOT BE WIRE-ORED
A, AN EACH MUST BE DRIVEN BY A MACRO
A, AN MUST BE DIFFERENTIALLY DRIVEN

$$Y = A\overline{AN}$$

A	AN	Y
0	0	UND
0	1	0
1	0	1
1	1	UND



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

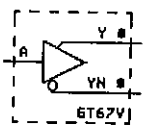
GT67V L cell VERY HI-SPEED TRANSLATOR DRIVER
OTHER MACRO TO V MACRO

		V	
Tpd	A->Y,YN (++)(+-)(-+)(--)	0.24	ns
I		1.89	mA
FAN-OUT LOAD LIMIT:		15	loads
k-FACTOR	RISING	0.020	ns/LU
	FALLING	0.020	ns/LU

---

*Y,YN OUTPUTS ARE 1/2 SWING (250mV)
*Y,YN MUST DRIVE A DIFFERENTIAL INPUT PAIR
*Y,YN CANNOT BE WIRE-ORED
*Y,YN CANNOT BE POWERED-DOWN

Y = A
YN = $\bar{A}$



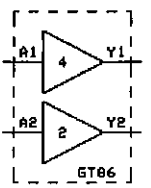
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT86 L cell 4-STAGE GATE DELAY; 2-STAGE GATE DELAY

		S	L	H	
Tpd ++	A1->Y1	1.60			ns
--	A1->Y1	1.52			ns
Tpd ++	A2->Y2	0.81			ns
--	A2->Y2	0.73			ns
I		2.97			mA
FAN-OUT LOAD LIMIT:		9			loads
k-FACTOR	RISING	0.04			ns/LU
	FALLING	0.04			ns/LU

- NO OPTIONS

Y1 = A1 Y2 = A2



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT87D 0.5 L cell STATIC HIGH - STATIC LOW DRIVER

DRIVER

----- Tpd DOES NOT APPLY TO THIS MACRO SINCE THE INPUT NEVER CHANGES ----------

I		1.89	mA
FAN-OUT LOAD LIMIT:		32	loads
k-FACTOR	RISING	STATIC	ns/LU
	FALLING	STATIC	ns/LU

A MUST BE TIED TO GROUND
A MUST NOT BE DRIVEN BY A MACRO
OUTPUT MAY NOT BE WIRE-ORED
OUTPUT MAY BE POWERED-DOWN

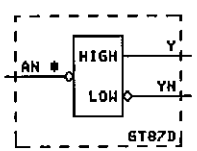
This driver is used to supply a ststic "1" or a static "0" to drive those macro input pins that are UNUSED in a given circuit but must be DRIVEN BY A MACRO. Use when an L-option (4 LOADS) or S-option (9 LOADS) simple OR/NOR gate cannot be used.

Y = "1" NAME THIS SIGNAL "VHIxxx"
YN = "0" NAME THIS SIGNAL "VLOxxx"

where "xxx" is 1 to 3 characters, letters or numbers or mixed such as:

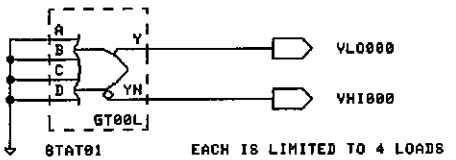
VHI001 VHI1A
VLO002 VLOBB1

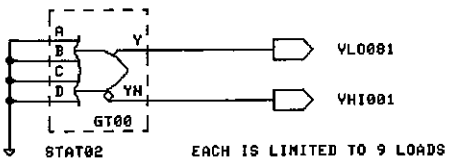
These signals are static (do not switch) and must be accounted for in any fault-grading analysis in the same manner as a grounded or terminated signal.

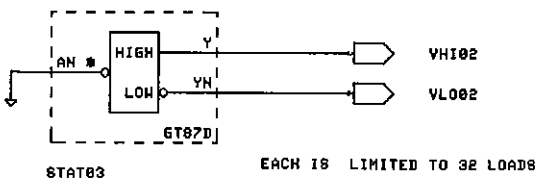


ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

STATIC DRIVING SCHEMES:







DO NOT USE A 15-LOAD OR 25-LOAD DRIVER MACRO
DO NOT USE AN H-OPTION MACRO
DO NOT DRIVE V MACROS

AMCC Q5000 MACRO SUMMARY - GTxx (804)

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT91V L cell VERY HI-SPEED DIFFERENTIAL-INPUT AND/NAND

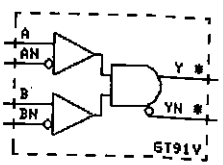
		V	
Tpd	++A->Y	0.23	ns
	--A->Y	0.23	ns
	++B->Y	0.35	ns
	--B->Y	0.36	ns
	+-A->YN	0.23	ns
	-+A->YN	0.23	ns
	+-B->YN	0.35	ns
	-+B->YN	0.36	ns
I		2.60	mA
FAN-OUT LOAD LIMIT:		9	loads
k-FACTOR	RISING	0.020	ns/LU
	FALLING	0.020	ns/LU

A, AN, B, BN - EACH MUST BE DRIVEN BY A MACRO
A, AN MUST BE DIFFERENTIALLY DRIVEN FROM ONE MACRO
B, BN MUST BE DIFFERENTIALLY DRIVEN FROM ONE MACRO
*Y,YN OUTPUTS ARE 1/2 SWING (250mV)
*Y,YN MUST DRIVE A DIFFERENTIAL INPUT PAIR
*Y,YN CANNOT BE WIRE-ORED
*Y,YN CANNOT BE POWERED-DOWN

Y = A AND B A,B are differential

YN = $\overline{A \text{ AND } B}$

A	AN	B	BN	Y	YN	
0	0	X	X	UND	UND	ILLEGAL
0	1	0	1	0	1	
X	X	0	0	UND	UND	ILLEGAL
1	0	1	0	0	1	
1	1	X	X	UND	UND	ILLEGAL
1	0	1	0	1	0	
X	X	1	1	UND	UND	ILLEGAL
0	1	0	1	0	1	



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

GT92V L cell VERY HI-SPEED DIFFERENTIAL-INPUT PAIRS OR/NOR

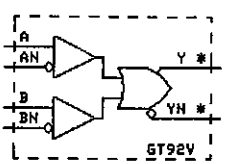
		V	
Tpd	++A->Y	0.23	ns
	--A->Y	0.23	ns
	++B->Y	0.35	ns
	--B->Y	0.36	ns
	+-A->YN	0.23	ns
	-+A->YN	0.23	ns
	+-B->YN	0.35	ns
	-+B->YN	0.36	ns
I		2.60	mA
FAN-OUT LOAD LIMIT:		9	loads
k-FACTOR	RISING	0.020	ns/LU
	FALLING	0.020	ns/LU

A, AN, B, BN - EACH MUST BE DRIVEN BY A MACRO
A, AN MUST BE DIFFERENTIALLY DRIVEN FROM ONE MACRO
B, BN MUST BE DIFFERENTIALLY DRIVEN FROM ONE MACRO
*Y,YN OUTPUTS ARE 1/2 SWING (250mV)
*Y,YN MUST DRIVE A DIFFERENTIAL INPUT PAIR
*Y,YN CANNOT BE WIRE-ORED
*Y,YN CANNOT BE POWERED-DOWN

$$Y = A + B$$

$$YN = \overline{A + B}$$

A	AN	B	BN	Y	YN	
0	0	X	X	UND	UND	ILLEGAL
0	1	0	1	0	1	
X	X	0	0	UND	UND	ILLEGAL
1	0	1	0	0	1	
1	1	X	X	UND	UND	ILLEGAL
1	0	1	0	1	0	
X	X	1	1	UND	UND	ILLEGAL
0	1	0	1	0	1	



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

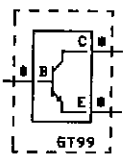
GT99 L cell MINIMUM SIZE TRANSISTOR FOR USE AS A THERMAL DIODE

	S	L	H	
I	3.30			mA

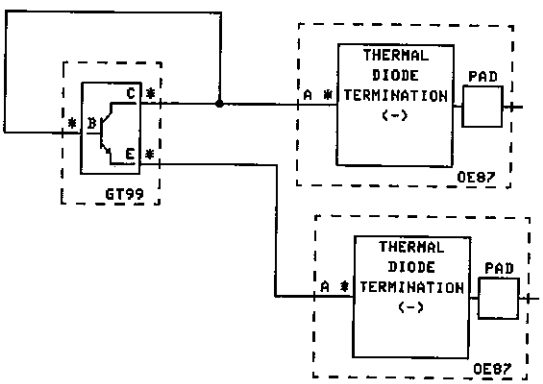
B MUST BE DRIVEN BY A MACRO
CONNECT OUTPUTS TO TWO OE86 OUTPUT MACROS
CONNECT IN C-B SHORT DIODE CONFIGURATION

- NO OPTIONS

C=B OR "1"
E=B OR "1"



THERMAL DIODE

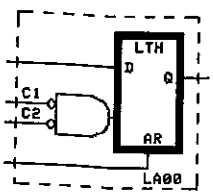


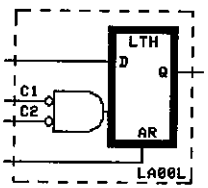
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

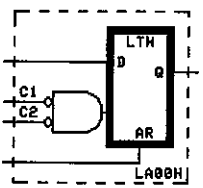
LA00 0.5 L cell D-LATCH WITH ASYNC. RESET, LOW-TRANSPARENT

		S	L	H	
Tpd	--D->Q	0.54	0.63	0.39	ns
	-+D->Q	0.97	0.86	0.50	ns
Tpd	--C1,C2->Q	0.93	1.03	0.64	ns
	-+C1,C2->Q	1.03	0.93	0.57	ns
Tpd	AR->Q				
	+-transparent,D=1	0.88	0.96	0.67	ns
	+-latched 1	0.95	1.04	0.70	ns
	-+transparent,D=1	1.19	1.31	0.73	ns
Tsu	(high data)	0.80	0.60	0.30	ns min
	(low data)	1.10	1.10	0.70	ns min
Th	(high data)	-0.10	-0.10	-0.10	ns min
	(low data)	0.10	0.00	0.20	ns min
Trec		1.40	1.40	1.00	ns min
PW	(C1,C2)	2.38	3.33	1.39	ns min
PW	(AR)	2.38	3.33	1.39	ns min
I		1.49	1.30	1.71	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.040	0.040	0.020	ns/LU
	FALLING	0.040	0.080	0.040	ns/LU

C1, C2 - AT LEAST ONE MUST BE DRIVEN BY A MACRO
AR MUST BE DRIVEN BY A MACRO







ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

LA00 0.5 L cell D-LATCH WITH ASYNC. RESET, LOW-TRANSPARENT

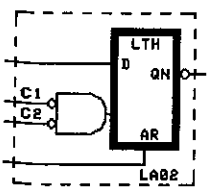
AR	C1	C2	D	Q	
0	1	X	X	Qn	
0	X	1	X	Qn	
0	0	0	1	1	TRANSPARENT
0	0	0	0	0	TRANSPARENT
1	X	X	X	0	

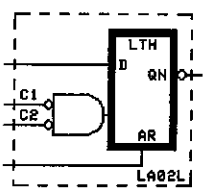
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

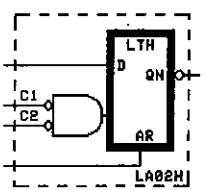
LA02 0.5 L cell D-LATCH, with ASYNC. RESET, LOW-TRANSPARENT

	S	L	H	
Tpd -+D->QN	0.77	0.68	0.38	ns
+-D->QN	0.51	0.57	0.39	ns
Tpd -+C->QN	0.94	0.85	0.53	ns
--C->QN	0.73	0.80	0.56	ns
Tpd AR->QN				
++transparent,D=1	1.21	1.10	0.70	ns
--transparent,D=1	0.91	0.98	0.72	ns
++latched 1	1.08	1.00	0.68	ns
Tsu (low data)	1.0	1.0	0.6	ns min
(high data)	2.5	2.5	1.0	ns min
Th (low data)	0.3	0.3	0.1	ns min
(high data)	0.0	0.0	0.2	ns min
Trec	1.0	1.0	1.0	ns min
PW (C1,C2)	2.38	3.33	1.39	ns min
PW (AR)	2.38	3.33	1.39	ns min
I	1.49	1.32	1.71	mA
FAN-OUT LOAD LIMIT:	9	4	9	loads
k-FACTOR RISING	0.040	0.040	0.020	ns/LU
FALLING	0.040	0.080	0.040	ns/LU

C1,C2 - AT LEAST ONE MUST BE DRIVEN BY A MACRO
AR MUST BE DRIVEN BY A MACRO







ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

LA02 0.5 L cell D-LATCH, with ASYNC. RESET, LOW-TRANSPARENT

AR	D	C1	C2	QNn+1	
1	X	X	X	1	
0	0	0	0	1	TRANSPARENT
0	1	0	0	0	TRANSPARENT
0	X	X	1	QNn	
0	X	1	X	QNn	

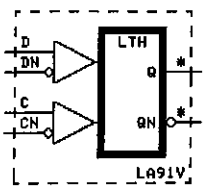
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

LA91V L cell VERY HI-SPEED, DIFFERENTIAL DATA, DIFFERENTIAL CLOCK, TRANSPARENT HIGH

		V	
Tpd	++D->Q	0.26	ns
	--D->Q	0.26	ns
	+-D->QN	0.26	ns
	-+D->QN	0.26	ns
	++C->Q	0.36	ns
	--C->Q	0.36	ns
	+-C->QN	0.36	ns
	-+C->QN	0.36	ns
Tsu	(D|DN)	0.11	ns min
Th	(D|DN)	0.20	ns min
PW	(C|CN)	0.83	ns min
I		3.75	mA
FAN-OUT LOAD LIMIT:		9	loads
k-FACTOR	RISING	0.020	ns/LU
	FALLING	0.020	ns/LU

---

*Q,QN OUTPUTS ARE 1/2 SWING (250mV)
*Q,QN MUST DRIVE A DIFFERENTIAL INPUT PAIR
*Q,QN CANNOT BE WIRE-ORED
*Q,QN CANNOT BE POWERED-DOWN



V MACRO

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

LA91V L cell VERY HI-SPEED, DIFFERENTIAL DATA, DIFFERENTIAL CLOCK, TRANSPARENT HIGH

D	DN	C	CN	Qn+1	QNn+1	
0	1	1	0	0	1	
0	0	1	0	UND	UND	ILLEGAL
1	0	1	0	1	0	
1	1	1	0	UND	UND	ILLEGAL
DATA	$\overline{DATA}$	0	1	Qn	QNn	
DATA	$\overline{DATA}$	0	0	UND	UND	ILLEGAL
DATA	$\overline{DATA}$	1	1	UND	UND	ILLEGAL

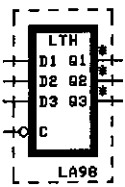
UND = undefined

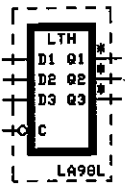
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

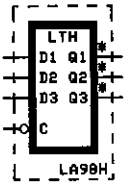
LA98 L cell TRIPLE D LATCH, WITH COMMON CLOCK

		S	L	H	
Tpd	++ D1->Q1	0.86	0.78	0.47	ns
	-- D1->Q1	0.50	0.58	0.37	ns
Tpd	++ D2->Q2	0.99	0.89	0.55	ns
	-- D2->Q2	0.55	0.65	0.41	ns
Tpd	++ D3->Q3	0.85	0.77	0.47	ns
	-- D3->Q3	0.49	0.57	0.37	ns
Tpd	-- C->Q1	0.87	0.96	0.56	ns
	-+ C->Q1	1.03	0.94	0.53	ns
Tpd	-- C->Q2	0.92	1.04	0.60	ns
	-+ C->Q2	1.16	1.06	0.62	ns
Tpd	-- C->Q3	0.86	0.94	0.56	ns
	-+ C->Q3	1.02	0.93	0.53	ns
Tsu	(C->Q1,Q2,Q3)	0.70	0.70	0.20	ns min
Th	(C->Q1,Q2,Q3)	0.10	0.10	0.30	ns min
PW	(C)	2.38	3.33	1.39	ns min
I		2.65	2.11	3.50	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.040	0.040	0.020	ns/LU
	FALLING	0.040	0.080	0.040	ns/LU

C MUST BE DRIVEN BY A MACRO
* Q1, Q2, Q3 MAY NOT BE WIRE-ORED
Q1, Q2, Q3 MAY NOT BE POWERED-DOWN
TRANSPARENT LOW CLOCK



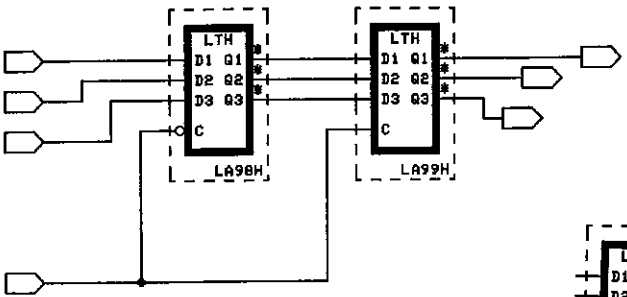




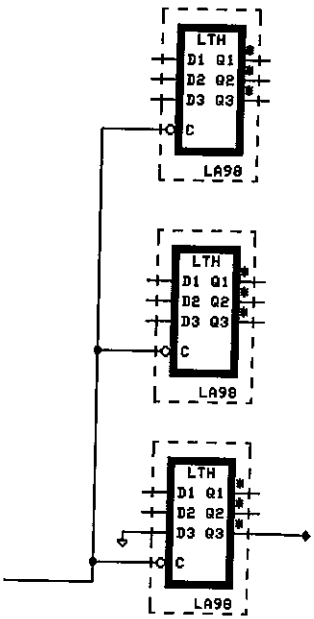
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

LA98 L cell TRIPLE D LATCH, WITH COMMON CLOCK

Di	C	Qin+1	
X	1	Qin	
1	0	1	TRANSPARENT
0	0	0	TRANSPARENT



3 RISING EDGE F/FS - 2 CELLS



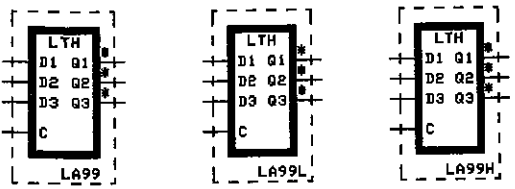
OCTAL LATCH

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

LA99 L cell TRIPLE D LATCH, WITH COMMON CLOCK

		S	L	H	
Tpd	++ D1->Q1	0.86	0.78	0.48	ns
	-- D1->Q1	0.49	0.58	0.37	ns
Tpd	++ D2->Q2	1.00	0.90	0.56	ns
	-- D2->Q2	0.54	0.64	0.41	ns
Tpd	++ D3->Q3	0.85	0.77	0.47	ns
	-- D3->Q3	0.49	0.57	0.37	ns
Tpd	+- C->Q1	1.01	0.93	0.62	ns
	++ C->Q1	0.84	0.93	0.67	ns
Tpd	+- C->Q2	1.15	1.05	0.69	ns
	++ C->Q2	0.91	1.03	0.72	ns
Tpd	+- C->Q3	1.00	0.92	0.67	ns
	++ C->Q3	0.84	0.92	0.67	ns
Tsu	(C->Q1,Q2,Q3)	0.70	0.70	0.20	ns min
Th	(C->Q1,Q2,Q3)	0.10	0.10	0.30	ns min
PW	(C)	2.38	3.33	1.67	ns min
I		2.65	2.11	3.50	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.040	0.040	0.020	ns/LU
	FALLING	0.040	0.080	0.040	ns/LU

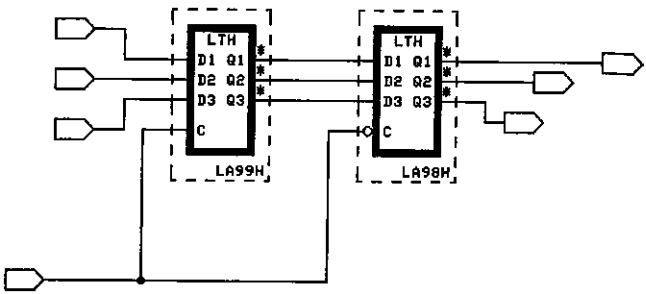
* Q1, Q2, Q3 MAY NOT BE WIRE-ORED
  Q1, Q2, Q3 MAY NOT BE POWERED-DOWN
  C MUST BE DRIVEN BY A MACRO
  TRANSPARENT HIGH CLOCK



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

LA99 L cell TRIPLE D LATCH, WITH COMMON CLOCK

Di	C	Qin+1	
X	0	Qin	
1	1	1	TRANSPARENT
0	1	0	TRANSPARENT



3 FALLING EDGE F/FS - 2 CELLS

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

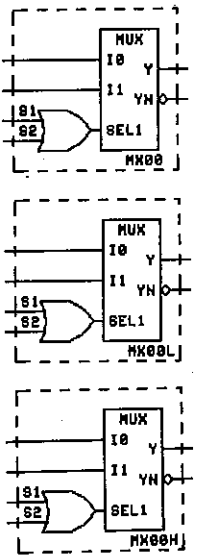
MX00 0.5 L cell 2:1 MUX WITH GATED SELECT, Y, YN

		S	L	H	
Tpd ++	I0,I1->Y	0.57	0.51	0.35	ns
--	I0,I1->Y	0.38	0.42	0.28	ns
Tpd +-	I0,I1->YN	0.48	0.53	0.36	ns
-+	I0,I1->YN	0.71	0.63	0.35	ns
Tpd	S1,S2->Y				
++	I0=0,I1=1	0.70	0.62	0.48	ns
--	I0=0,I1=1	0.70	0.73	0.48	ns
+-	I0=1,I1=0	0.68	0.73	0.55	ns
-+	I0=1,I1=0	0.68	0.63	0.40	ns
Tpd	S1,S2->YN				
++	I0=1,I1=0	0.87	0.79	0.55	ns
--	I0=1,I1=0	0.60	0.65	0.45	ns
+-	I0=0,I1=1	0.61	0.63	0.51	ns
-+	I0=0,I1=1	0.89	0.80	0.46	ns
I		1.14	0.78	1.57	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

S1, S2 - AT LEAST ONE MUST BE DRIVEN BY A MACRO

$Y = I1\ (S1 + S2) + I0\ (\overline{\overline{S1} + \overline{S2}});\ YN = \overline{Y}$

S1	S2	I0	I1	Y	YN
0	0	1	X	1	0
0	0	0	X	0	1
X	1	X	1	1	0
X	1	X	0	0	1
1	X	X	1	1	0
1	X	X	0	0	1
X	X	0	0	0	1
X	X	0	1	UNKNOWN	
X	X	1	0	UNKNOWN	
X	X	1	1	1	0



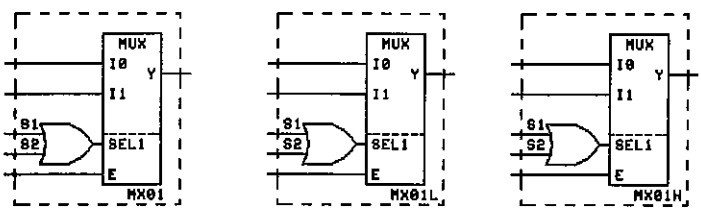
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

MX01 0.5 L cell 2:1 MUX; ENABLE; GATED SELECT, Y

		S	L	H	
Tpd	++I0,I1->Y	0.74	0.66	0.41	ns
	--I0,I1->Y	0.47	0.53	0.33	ns
	++S1,S2->Y	0.85	0.76	0.51	ns
	--S1,S2->Y	0.79	0.87	0.51	ns
	+-S1,S2->Y	0.67	0.73	0.53	ns
	-+S1,S2->Y	0.86	0.77	0.47	ns
	++E->Y	1.03	0.94	0.69	ns
	--E->Y	0.91	1.02	0.59	ns
I		0.99	0.81	1.67	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

E MUST BE DRIVEN BY A MACRO
S1, S2 - AT LEAST ONE MUST BE DRIVEN BY A MACRO

$$Y_{enabled} = I1\ (S1 + S2) + I0\ \overline{(S1 + S2)}$$



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

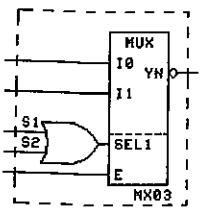
MX03 0.5 L cell 2:1 MUX; ENABLE; GATED SELECT, YN

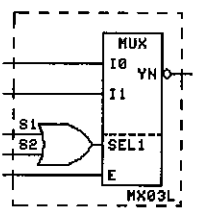
		S	L	H	
Tpd	+- I0,I1->YN	0.57	0.65	0.71	ns
	-+ I0,I1->YN	0.89	0.79	0.41	ns
Tpd	S1->YN				
	+- I0=0,I1=1	0.85	0.92	0.67	ns
	-+ I0=0,I1=1	1.06	0.95	0.56	ns
	++ I0=1,I1=0	1.08	0.98	0.64	ns
	-- I0=1,I1=0	0.85	0.94	0.55	ns
Tpd	++ E->YN	1.20	1.08	0.76	ns
	-- E->YN	1.08	1.18	0.64	ns
I		0.99	0.81	1.66	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

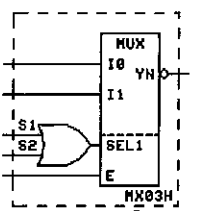
E MUST BE DRIVEN BY A MACRO
S1, S2 - AT LEAST ONE MUST BE DRIVEN BY A MACRO

$$YN_{enabled} = (I1(S1+S2) + I0(\overline{S1}+\overline{S2}))$$

E	S1+S2	I0	I1	YN
0	X X	X	X	0
1	0 0	0	X	1
1	0 0	1	X	0
1	1 X	X	0	1
1	X 1	X	0	1
1	1 X	X	1	0
1	X 1	X	1	0
1	X X	0	0	1
1	X X	0	1	UNKNOWN
1	X X	1	0	UNKNOWN
1	X X	1	1	0





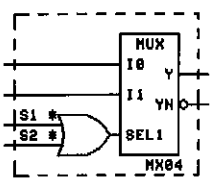


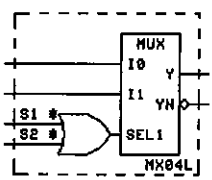
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

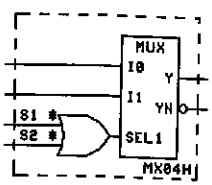
MX04 0.5 L cell 2:1 MUX WITH GATED SELECT, Y, YN

		S	L	H	
Tpd	++I0->Y	0.59	0.50	0.17	ns
	+-I0->YN	0.30	0.34	0.18	ns
	--I0->Y	0.52	0.57	0.32	ns
	-+I0->YN	0.67	0.60	0.32	ns
	++I1->Y	0.55	0.49	0.17	ns
	+-I1->YN	0.29	0.34	0.18	ns
	--I1->Y	0.52	0.57	0.32	ns
	-+I1-YN	0.67	0.59	0.31	ns
	++S1,S2->Y	0.80	0.71	0.39	ns
	+-S1,S2->Y	0.76	0.83	0.39	ns
	-+S1,S2->Y	0.73	0.78	0.46	ns
	--S1,S2->Y	0.82	0.74	0.39	ns
	+-S1,S2->YN	0.57	0.62	0.44	ns
	++S1,S2->YN	0.89	0.80	0.44	ns
	--S1,S2->YN	0.88	0.80	0.45	ns
	-+S1,S2->YN	0.59	0.64	0.45	ns
I		1.17	0.81	1.62	mA
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU
FAN-OUT LOAD LIMIT:		9	4	9	loads

* EITHER S0 OR S1 - MUST BE DRIVEN BY A MACRO







ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

MX04 0.5 L cell 2:1 MUX WITH GATED SELECT, Y, YN

$Y = I1\ (S1 + S2) + I0\ (\overline{S1} + \overline{S2})$ $\qquad YN = \overline{Y}$

S1	S2	I0	I1	Y	YN
0	0	1	X	1	0
0	0	0	X	0	1
X	1	X	1	1	0
X	1	X	0	0	1
1	X	X	1	1	0
1	X	X	0	0	1
X	X	0	0	0	1
X	X	0	1	UNKNOWN	
X	X	1	0	UNKNOWN	
X	X	1	1	1	0

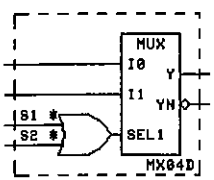
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

MX04D 0.5 L cell 2:1 MUX,GATED SELECT,Y,YN, DRIVER

		DRIVER	
Tpd	++I0->Y	0.23	ns
	+-I0->YN	0.16	ns
	--I0->Y	0.32	ns
	-+I0->YN	0.34	ns
	++I1->Y	0.23	ns
	+-I1->YN	0.16	ns
	--I1->Y	0.32	ns
	-+I1-YN	0.34	ns
	++S1,S2->Y	0.44	ns
	+-S1,S2->Y	0.47	ns
	-+S1,S2->Y	0.46	ns
	--S1,S2->Y	0.45	ns
	+-S1,S2->YN	0.41	ns
	++S1,S2->YN	0.47	ns
	--S1,S2->YN	0.48	ns
	-+S1,S2->YN	0.43	ns
I		2.34	mA
k-FACTOR	RISING	0.02	ns/LU
	FALLING	0.02	ns/LU
FAN-OUT LOAD LIMIT:		15	loads

---

* EITHER S0 OR S1 - MUST BE DRIVEN BY A MACRO



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

MX04D 0.5 L cell 2:1 MUX WITH GATED SELECT, Y, YN

$Y = I1\ (S1 + S2) + I0\ (\overline{S1} + \overline{S2})$ $YN = \overline{Y}$

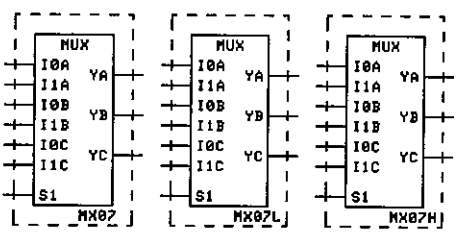
S1	S2	I0	I1	Y	YN
0	0	1	X	1	0
0	0	0	X	0	1
X	1	X	1	1	0
X	1	X	0	0	1
1	X	X	1	1	0
1	X	X	0	0	1
X	X	0	0	0	1
X	X	0	1	UNKNOWN	
X	X	1	0	UNKNOWN	
X	X	1	1	1	0

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

MX07 L cell TRIPLE 2:1 MUX, COMMON SELECT

		S	L	H	
Tpd	++ I0A->YA	0.63	0.49	0.33	ns
	-- I0A->YA	0.41	0.41	0.21	ns
Tpd	++ I1A->YA	0.63	0.49	0.26	ns
	-- I1A->YA	0.47	0.48	0.21	ns
Tpd	++ I0B->YB	0.73	0.57	0.35	ns
	-- I0B->YB	0.40	0.46	0.30	ns
Tpd	++ I1B->YB	0.65	0.57	0.35	ns
	-- I1B->YB	0.48	0.54	0.31	ns
Tpd	++ I0C,I1C->YC	0.54	0.49	0.33	ns
	-- I0C->YC	0.37	0.41	0.29	ns
	-- I1C->YC	0.49	0.48	0.29	ns
Tpd	S1->YA				
	++ I0i=0,I1i=0	0.79	0.63	0.49	ns
	-- I0i=0,I1i=1	0.75	0.75	0.45	ns
	+- I0i=1,I1i=0	0.73	0.66	0.56	ns
	-+ I0i=1,I1i=0	0.66	0.73	0.40	ns
Tpd	S1->YB				
	++ I0i=0,I1i=1	0.81	0.74	0.54	ns
	-- I0i=1,I1i=1	0.76	0.82	0.50	ns
	+- I0i=1,I1i=0	0.74	0.77	0.60	ns
	-+ I0i=1,I1i=0	0.85	0.79	0.45	ns
Tpd	S1->YC				
	++ I0i=0,I1i=1	0.68	0.63	0.49	ns
	-- I0i=0,I1i=1	0.71	0.75	0.47	ns
	+- I0i=1,I1i=0	0.68	0.66	0.57	ns
	-+ I0i=1,I1i=0	0.72	0.72	0.41	ns
	i= A,B,C				
I		1.98	1.44	2.88	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

S1 MUST BE DRIVEN BY A MACRO



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

MX07 L cell TRIPLE 2:1 MUX, COMMON SELECT

$YA = S1.I1A + \overline{S1}.I0A$
$YB = S1.I1B + \overline{S1}.I0B$
$YC = S1.I1C + \overline{S1}.I0C$

S1	I1x	I0x	Yx (x=A,B,C)
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1
X	0	0	0
X	0	1	UNKNOWN
X	1	0	UNKNOWN
X	1	1	1

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

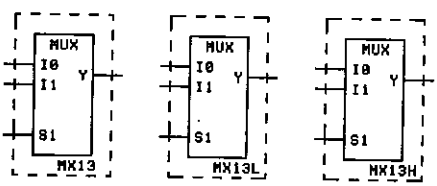
MX13 0.5 L cell 2:1 MUX

		S	L	H	
Tpd ++	I0->Y	0.54	0.49	0.33	ns
--	I0->Y	0.37	0.41	0.28	ns
Tpd ++	I1->Y	0.49	0.49	0.33	ns
--	I1->Y	0.43	0.48	0.29	ns
Tpd	S1->Y				
++	I0=0,I1=1	0.67	0.61	0.47	ns
--	I0=0,I1=1	0.60	0.64	0.44	ns
+-	I0=1,I1=0	0.66	0.70	0.54	ns
-+	I0=1,I1=0	0.68	0.62	0.38	ns
I		0.81	0.63	1.26	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

S1 MUST BE DRIVEN BY A MACRO

$$Y = (I0.\overline{S1}) + (I1.S1)$$

S1	I0	I1	Y
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1
X	0	0	0
X	1	1	1
X	1	0	UNKNOWN
X	0	1	UNKNOWN

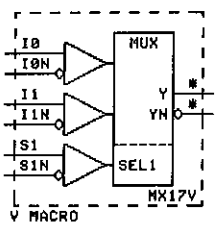


ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

MX17V L cell 2:1 MUX, SUPER HIGH SPEED MUX
DIFFERENTIAL INPUTS

		V	
Tpd ++	I0,I1->Y	0.24	ns
--	I0,I1->Y	0.24	ns
+-	I0,I1->YN	0.24	ns
-+	I0,I1->YN	0.24	ns
Tpd ++	S1->Y,YN	0.35	ns
+-	S1->Y,YN	0.35	ns
-+	S1->Y,YN	0.35	ns
--	S1->Y,YN	0.35	ns
I		3.05	mA
k-FACTOR	RISING	0.020	ns/LU
	FALLING	0.020	ns/LU
FAN-OUT LOAD LIMIT:		9	loads

S1,S1N EACH MUST BE DRIVEN BY A MACRO
I0,I0N MUST BE DIFFERENTIALLY DRIVEN FROM ONE MACRO
I1,I1N MUST BE DIFFERENTIALLY DRIVEN FROM ONE MACRO
S1,S1N MUST BE DIFFERENTIALLY DRIVEN FROM MACRO
*Y,YN OUTPUTS ARE 1/2 SWING (250mV)
*Y,YN MUST DRIVE A DIFFERENTIAL INPUT PAIR
*Y,YN CANNOT BE WIRE-ORED
*Y,YN CANNOT BE POWERED-DOWN



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

MX17V L cell 2:1 MUX, SUPER HIGH SPEED MUX
DIFFERENTIAL INPUTS

$$Y = (I1.S1) + (I0.\overline{S1})$$

I0	I0N	I1	I1N	S1	S1N	Y	YN	
X	X	X	X	0	0	UND	UND	ILLEGAL
0	0	X	X	0	1	UND	UND	ILLEGAL
0	1	X	X	0	1	0	1	
1	0	X	X	0	1	1	0	
1	1	X	X	0	1	UND	UND	ILLEGAL
X	X	0	0	1	0	UND	UND	ILLEGAL
X	X	0	1	1	0	0	1	
X	X	1	0	1	0	1	0	
X	X	1	1	1	0	UND	UND	ILLEGAL
X	X	X	X	1	1	UND	UND	ILLEGAL
0	1	0	1	X	X	0	1	
1	0	1	0	X	X	1	0	

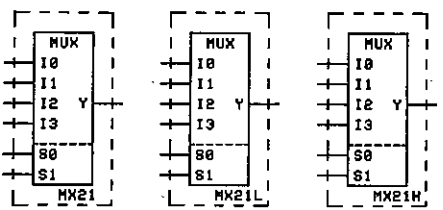
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

MX21 L cell 4:1 MUX

		S	L	H	
Tpd	++ I0->Y	0.95	0.84	0.49	ns
	-- I0->Y	0.60	0.70	0.40	ns
	++ I1->Y	0.93	0.81	0.49	ns
	-- I1->Y	0.59	0.70	0.40	ns
	++ I2->Y	0.98	0.86	0.49	ns
	-- I2->Y	0.60	0.70	0.40	ns
	++ I3->Y	1.00	0.88	0.50	ns
	-- I3->Y	0.64	0.74	0.42	ns
	-- S0->Y	0.93	1.05	0.56	ns
	-+ S0->Y	1.30	1.17	0.64	ns
	+- S0->Y	1.02	1.12	0.71	ns
	++ S0->Y	1.06	0.94	0.64	ns
	-- S1->Y	1.07	1.18	0.65	ns
	-+ S1->Y	1.38	1.24	0.69	ns
	+- S1->Y	1.24	1.35	0.90	ns
	++ S1->Y	1.29	1.16	0.80	ns
I		1.00	0.83	1.62	mA
FAN-OUT LOAD LIMIT		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

S0, S1 - BOTH MUST BE DRIVEN BY A MACRO

$Y = I0 \cdot \overline{S0} \cdot \overline{S1} + I1 \cdot S0 \cdot \overline{S1} + I2 \cdot \overline{S0} \cdot S1 + I3 \cdot S0 \cdot S1$

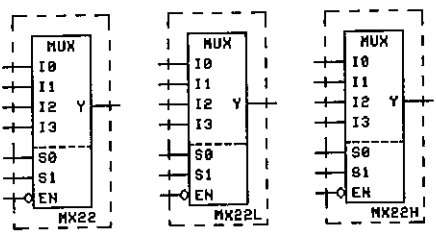


ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

MX22 L cell 4:1 MUX WITH LOW ENABLE

		S	L	H	
Tpd	++I0->Y	1.52	1.33	0.71	ns
	--I0->Y	0.93	1.11	0.58	ns
	++I1->Y	1.47	1.28	0.69	ns
	--I1->Y	0.87	1.04	0.55	ns
Tpd	++I2->Y	1.52	1.27	0.71	ns
	--I2->Y	0.93	1.08	0.58	ns
	++I3->Y	1.50	1.32	0.69	ns
	--I3->Y	0.88	1.05	0.56	ns
Tpd	++S0->Y	1.56	1.34	0.84	ns
	+-S0->Y	1.17	1.33	0.82	ns
	-+S0->Y	1.64	1.41	0.81	ns
	--S0->Y	1.28	1.45	0.75	ns
Tpd	++S1->Y	1.70	1.56	1.11	ns
	+-S1->Y	1.54	1.64	1.10	ns
	-+S1->Y	1.67	1.65	0.92	ns
	--S1->Y	1.40	1.57	0.85	ns
Tpd	-+EN->Y	1.37	1.19	0.56	ns
	+-EN->Y	0.83	0.96	0.68	ns
I		1.26	1.08	2.16	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

S0, S1 - BOTH MUST BE DRIVEN BY A MACRO



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

MX22 L cell 4:1 MUX WITH LOW ENABLE

$Y = I0.\overline{S0}.\overline{S1}.\overline{EN} + I1.S0.\overline{S1}.\overline{EN} + I2.\overline{S0}.S1.\overline{EN} + I3.S0.S1.\overline{EN}$

EN	S0	S1	I0	I1	I2	I3	Y
0	0	0	0	X	X	X	0
0	0	0	1	X	X	X	1
0	1	0	X	0	X	X	0
0	1	0	X	1	X	X	1
0	0	1	X	X	0	X	0
0	0	1	X	X	1	X	1
0	1	1	X	X	X	0	0
0	1	1	X	X	X	1	1
0	X	X	0	0	0	0	0
0	X	X	1	1	1	1	1
1	X	X	X	X	X	X	0
X	X	X	0	0	0	0	0

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

MX25 L cell 4:1 MUX
IMPROVED MX21, WITH YN OUTPUT

			S	L	H	
Tpd	++	I0->Y	1.13	0.99	0.43	ns
	+-	I0->YN	0.67	0.77	0.41	ns
	--	I0->Y	0.68	0.80	0.38	ns
	-+	I0->YN	1.12	0.98	0.37	ns
	++	I1->Y	1.13	0.99	0.43	ns
	+-	I1->YN	0.64	0.74	0.41	ns
	--	I1->Y	0.68	0.80	0.38	ns
	-+	I1->YN	1.12	0.98	0.37	ns
	++	I2->Y	1.13	0.99	0.43	ns
	+-	I2->YN	0.67	0.77	0.41	ns
	--	I2->Y	0.68	0.80	0.38	ns
	-+	I2->YN	1.13	0.99	0.38	ns
	++	I3->Y	1.13	0.99	0.43	ns
	+-	I3->YN	0.64	0.74	0.41	ns
	--	I3->Y	0.67	0.79	0.38	ns
	-+	I3-YN	1.13	0.99	0.38	ns
	++	S0->Y	1.20	1.07	0.53	ns
	+-	S0->YN	0.74	0.83	0.53	ns
	+-	S0->Y	1.28	1.06	0.58	ns
	++	S0->YN	1.38	1.23	0.56	ns
	-+	S0->Y	0.95	1.14	0.55	ns
	--	S0->YN	0.80	0.91	0.55	ns
	-+	S0->Y	1.01	1.14	0.58	ns
	-+	S0->YN	1.48	1.31	0.57	ns
	++	S1->Y	1.42	1.28	0.70	ns
	+-	S1->YN	1.00	1.14	0.74	ns
	+-	S1->Y	1.19	1.31	0.76	ns
	++	S1->YN	1.54	1.44	0.71	ns
	-+	S1->Y	1.50	1.35	0.56	ns
	--	S1->YN	1.04	1.16	0.58	ns
	--	S1->Y	1.16	1.28	0.59	ns
	-+	S1->YN	1.61	1.45	0.58	ns

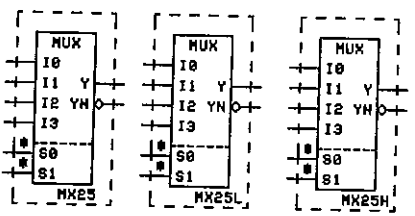
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

MX25 L cell 4:1 MUX
IMPROVED MX21, WITH YN OUTPUT

		S	L	H	
I		1.40	1.04	2.07	mA
FAN-OUT LOAD LIMIT		9	4	9	loads
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU

S0, S1 - BOTH MUST BE DRIVEN BY A MACRO

S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3



ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

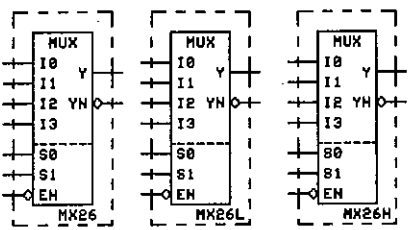
MX26	L cell	4:1 MUX WITH LOW ENABLE			
		S	L	H	
Tpd +-	EN->Y	1.46	1.52	1.28	ns
-+	EN->Y	1.87	1.64	1.23	ns
Tpd ++	EN>-YN	2.32	2.12	1.44	ns
--	EN->YN	2.08	2.20	1.50	ns
++	I0->Y	1.25	1.09	0.46	ns
--	I0->Y	0.76	0.89	0.42	ns
+-	I0->YN	0.60	0.76	0.41	ns
-+	I0->YN	1.11	0.97	0.36	ns
++	I1->Y	1.25	1.07	0.46	ns
--	I1->Y	0.78	0.89	0.42	ns
+-	I1->YN	0.63	0.69	0.41	ns
-+	I1->YN	1.12	0.94	0.36	ns
++	I2->Y	1.26	1.11	0.46	ns
--	I2->Y	0.79	0.89	0.42	ns
+-	I2->YN	0.63	0.73	0.41	ns
-+	I2->YN	1.07	0.95	0.36	ns
++	I3->Y	1.26	1.10	0.46	ns
--	I3->Y	0.78	0.89	0.41	ns
+-	I3->YN	0.59	0.68	0.40	ns
-+	I3->YN	1.05	0.92	0.36	ns
++	S0->Y	1.34	1.18	0.56	ns
--	S0->Y	1.23	1.39	0.63	ns
+-	S0->Y	1.34	1.18	0.62	ns
-+	S0->Y	1.33	1.33	0.59	ns
+-	S0->YN	0.72	0.81	0.52	ns
-+	S0->YN	1.37	1.22	0.54	ns
++	S0->YN	1.33	1.23	0.53	ns
--	S0->YN	1.48	1.31	0.55	ns
++	S1->Y	1.51	1.34	0.74	ns
--	S1->Y	1.40	1.52	0.64	ns
+-	S1->Y	1.51	1.44	0.76	ns
-+	S1->Y	1.50	1.47	0.60	ns
++	S1->YN	1.47	1.37	0.71	ns
--	S1->YN	1.46	1.40	0.57	ns
+-	S1->YN	0.89	0.98	0.71	ns
-+	S1->YN	1.57	1.41	0.56	ns

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

MX26	L cell	4:1 MUX WITH LOW ENABLE			
		S	L	H	
I		2.07	1.71	2.75	mA
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU
FAN-OUT LOAD LIMIT:		9	4	9	loads

S0, S1 - BOTH MUST BE DRIVEN BY A MACRO

S1	S0	EN	Y	YN
0	0	0	I0	$\overline{I0}$
0	1	0	I1	$\overline{I1}$
1	0	0	I2	$\overline{I2}$
1	1	0	I3	$\overline{I3}$
X	X	1	0	1



AMCC Q5000 MACRO SUMMARY - REGxx (804)

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

REG00 4.5 L cells 4-BIT 4:1 MUX WITH D F/F
- UNIVERSAL REGISTER

		S	L	H	
Tpd	++CP->QA,QB,QC,QD	1.60	1.47	0.99	ns
	+-CP->QA,QB,QC,QD	1.09	1.35	0.90	ns
Tsu	(AIi,BIi,CIi,DIi)	1.33	1.33	1.64	ns min
Thd	(AIi,BIi,CIi,DIi)	-0.52	-0.52	-0.52	ns min
Tsu	(S0)	1.79	1.79	2.09	ns min
Thd	(S0)	-1.26	-1.26	-1.26	ns min
Tsu	(SI)	2.17	2.17	2.17	ns min
Thd	(SI)	-1.57	-1.57	-1.57	ns min
	i= 0,1,2,3				
PW(CP)		2.38	3.33	1.39	ns min
I		7.11	6.39	8.01	mA
FAN-OUT LOAD LIMIT:		9	4	9	loads
INTERCONNECT PINS:		15	15	15	internal
k-FACTOR	RISING	0.04	0.04	0.02	ns/LU
	FALLING	0.04	0.08	0.04	ns/LU
MAXIMUM FREQUENCY OF OPERATION (fMAX)		210	150	360	MHz

---

* CP COUNTS AS 2 LOADS
S0, S1, CP - EACH MUST BE DRIVEN BY A MACRO

REG00 is a general-purpose or universal register configured as a four 4:1 MUXs with the output of each mux going into the D input of a positive-edge triggered D flip-flop.

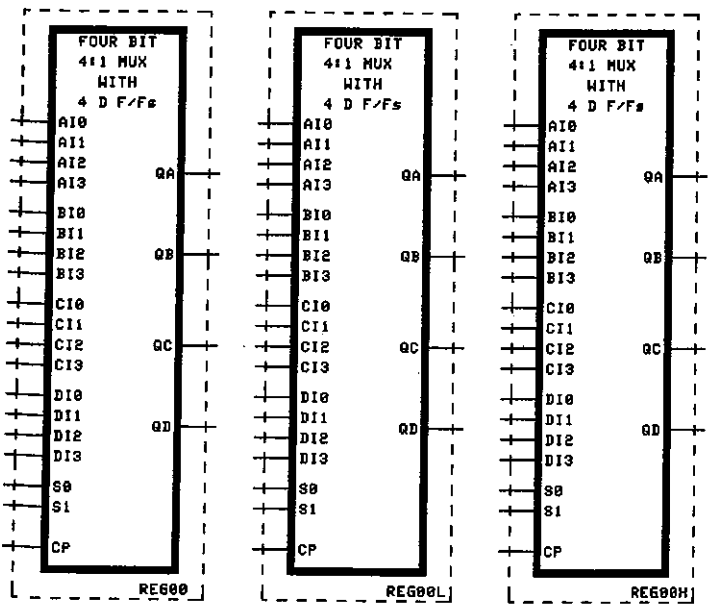
S1	S0	I
0	0	I0
0	1	I1
1	0	I2
1	1	I3

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC
I = ICC FOR 100% TTL, ELSE I = IEE

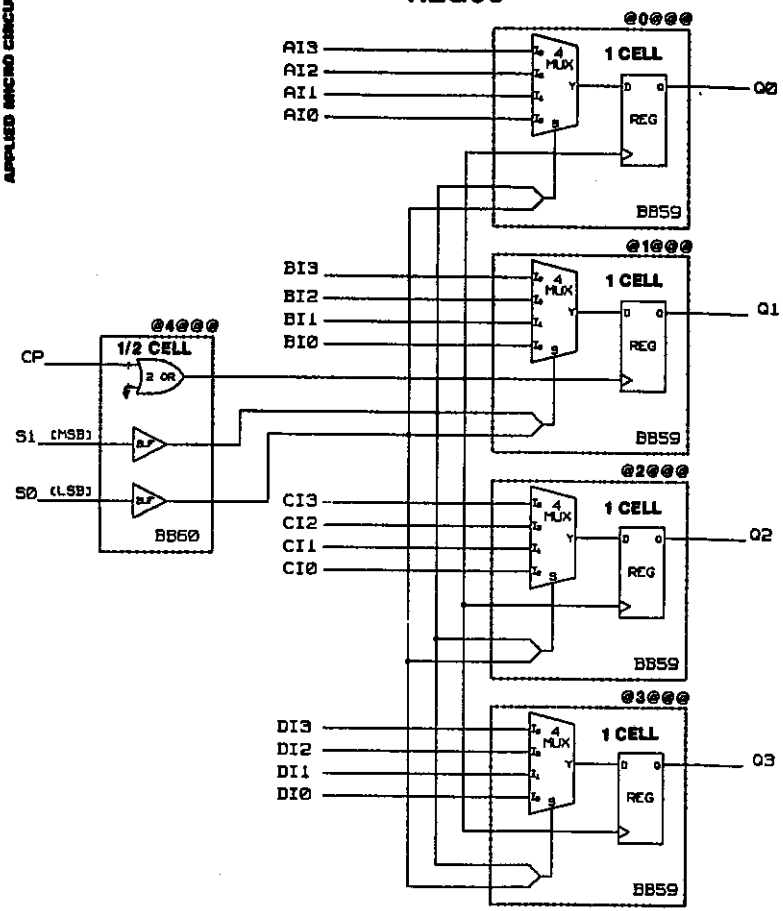
REG00 4.5 L cells 4-BIT 4:1 MUX WITH D F/F
- UNIVERSAL REGISTER

S1	S0	xI0	xI1	xI2	xI3	CP	Qxn+1 (x=A,B,C,D)
0	0	0	X	X	X	R	0
0	0	1	X	X	X	R	1
0	1	X	0	X	X	R	0
0	1	X	1	X	X	R	1
1	0	X	X	0	X	R	0
1	0	X	X	1	X	R	1
1	1	X	X	X	0	R	0
1	1	X	X	X	1	R	1
X	X	X	X	X	X	0	Qxn
X	X	X	X	X	X	1	Qxn

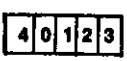
R = rising edge of the clock



REG00



PREPLACEMENTS MUST USE THIS CELL ARRANGEMENT



Section 6-5:

Special

WIRE-ORS

WIRE-OR MACROS (SYMBOLS) - REQUIRED

WIREOR2
WIREOR3
WIREOR4

- TIMING DELAYS DUE TO WIRE-ORS IN THE LOGIC ARE ACCOUNTED FOR BY THE FRONT-, INTERMEDIATE- AND BACK-ANNOTATION SOFTWARE.

- PARAMETRIC WIRE-ORS ARE NOT ALLOWED ON AMCC SCHEMATICS.

- ALL INPUT PINS ON A WIRE-OR MUST BE DRIVEN BY A MACRO AND THAT MACRO MAY DRIVE NO OTHER LOADS.

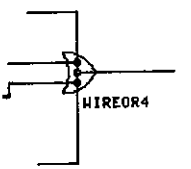
- NO WIRE-OR MAY DRIVE ANOTHER WIRE-OR.

- THE OUTPUT OF A WIRE-OR IS NOT TERMINATED.

- NO DRIVERS OR V-MACROS MAY DRIVE A WIRE-OR.

- OTHER MACROS THAT CANNOT DRIVE A WIRE-OR ARE IDENTIFIED BY AN "*" ON THE OUTPUT PIN.

- EXCESSIVE FAN-OUT LOADING ON A WIRE-OR WILL BE DETECTED.



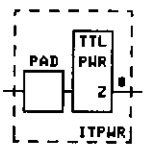
ADDED POWER AND GROUNDS

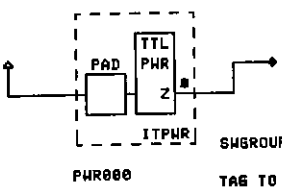
ITPWR I/O CELL ADDED V_{CC} (+5V) PAD

REQUIRED WHEN AN ADDED TTL POWER PAD IS NEEDED.
USES THE PAD PORTION OF THE I/O CELL.
USED TO OBTAIN A CORRECT POPULATION REPORT AND EXTERNAL PIN (PAD) COUNT BY THE AMCC MACROMATRIX ERC SOFTWARE.

- GROUND THE INPUT PIN WITH THE WIRE POINTING UP
- TERMINATE THE OUTPUT

NOTE: When placing an ITPWR macro, the macro must be interspersed with the simultaneously switching outputs it supports. On the Q5000T array and any other array with packages that contain internal power-ground planes, an ITPWR must be placed on a PAD that will allow it to be connected to the internal plane if it is at all possible. Placing it on a pad that must connect to a package pin requires a custom DUT board for test.





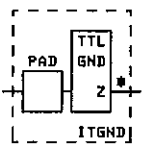
ADDED POWER AND GROUNDS

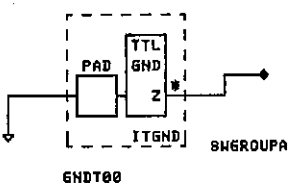
ITGND I/O CELL ADDED TTL GND PAD

REQUIRED WHEN AN ADDED TTL GROUND PAD IS NEEDED.
USES THE PAD PORTION OF THE I/O CELL.
USED TO OBTAIN A CORRECT POPULATION REPORT AND EXTERNAL PIN (PAD) COUNT BY THE AMCC MACROMATRIX ERC SOFTWARE.

- GROUND THE INPUT PIN WITH THE WIRE POINTING DOWN
- TERMINATE THE OUTPUT

NOTE: When placing an ITGND macro, the macro must be interspersed with the simultaneously switching outputs it supports. On the Q5000T array and any other array with packages that contain internal power-ground planes, an ITGND must be placed on a PAD that will allow it to be connected to the internal plane if it is at all possible. Placing it on a pad that must connect to a package pin requires a custom DUT board for test.





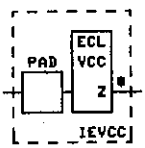
ADDED POWER AND GROUNDS

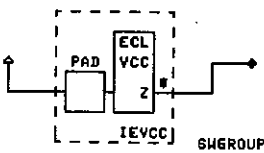
IEVCC I/O CELL ADDED ECL VCC PAD

REQUIRED WHEN AN ADDED ECL VCC PAD IS NEEDED.
USES THE PAD PORTION OF THE I/O CELL.
USED TO OBTAIN A CORRECT POPULATION REPORT AND EXTERNAL PIN (PAD) COUNT BY THE AMCC MACROMATRIX ERC SOFTWARE.

- GROUND THE INPUT PIN WITH THE WIRE POINTING DOWN FOR STANDARD-REFERENCE ECL; POINTING UP FOR +5V REF ECL.
- TERMINATE THE OUTPUT
- IEVCC is a GROUND pad in a STD-REF ECL circuit.
- IEVCC is a POWER pad in a +5V REF ECL circuit.

NOTE: When placing an IEVCC macro, the macro must be interspersed with the simultaneously switching outputs it supports. On the Q5000T array and any other array with packages that contain internal power-ground planes, an IEVCC must be placed on a PAD that will allow it to be connected to the internal plane if it is at all possible. Placing it on a pad that must connect to a package pin requires a custom DUT board for test.

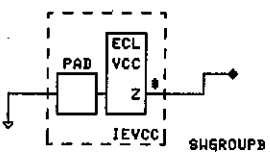




PWRE00

+5VREF ECL SYSTEM

TAG TO APPROPRIATE SWITCH GROUP



GNDE00

STD REF ECL SYSTEM

CHIP MACROS:

The chip macro documents the number of fixed power and ground pins that a particular array has for a given I/O mode. It also documents the internal pin count limit, the number of each type of cell available on a given array, the allowed cell utilization, the default power supply or supplies, the worst-case current multiplier for MIL and for COM product grades and other data as required by the AMCC MacroMatrix software.

- MUST BE USED - THE MACROMATRIX ERC SOFTWARE REQUIRES THAT A CHIP MACRO BE USED ON THE SCHEMATICS

- Follow directions in the MACROMATRIX USER'S GUIDE (Volume II, Section 8) and MACROMATRIX INSTALLATION MANUAL (Volume II, Section 7) to attach parameters or values to the chip macros as required - the procedure is EWS-specific.

- Ground and terminate inputs and outputs as shown in the examples. The inputs to a chip macro are always tied to global ground regardless of the individual chip technology (BiCMOS, Bipolar).

- The VTA pin is for use by the BIxx macros that require it. If none are present, terminate the pin. The Q5000 Series has no released BIxx macros.

- Chip macros are named (CHIP00) but are not listed in the placement file, use no cells and draw no current. They are informational units only.

- Page 1 of the schematics should contain the chip macros and the added power and ground macros.

AMCC Q5000 MACRO LIBRARY SUMMARY - SPECIAL (804)

CHIP MACROS

Chip Macro Parameters that are legal for the Q5000 Series:

		TTL	100% ECL	MIX	+5MIX
PRODUCT_NAME	AMCC ASSIGNED NAME	X	X	X	X
DEVICE_NUMBER	AMCC ASSIGNED NUMBER	X	X	X	X
PRODUCT_GRADE	MIL OR COM	X	X	X	X
POWER_SUPPLY	FOR OTHER THAN DEFAULT	-	X	X	-

The first three parameters are REQUIRED for design submission - the ERCs will use default values and continue but the resulting report (AMCCERC.LST) cannot be submitted.

Allowed POWER_SUPPLY parameter values for the Q5000 Series:

default	What appears on the chip macro graphic
STD4	-4.5V ECL VEE SUPPLY; ECL VCC = 0V
STD5	-5.2V ECL VEE SUPPLY; ECL VCC = 0V
5VREF	+5V ECL VCC SUPPLY; ECL VEE = 0V

CHIP MACROS

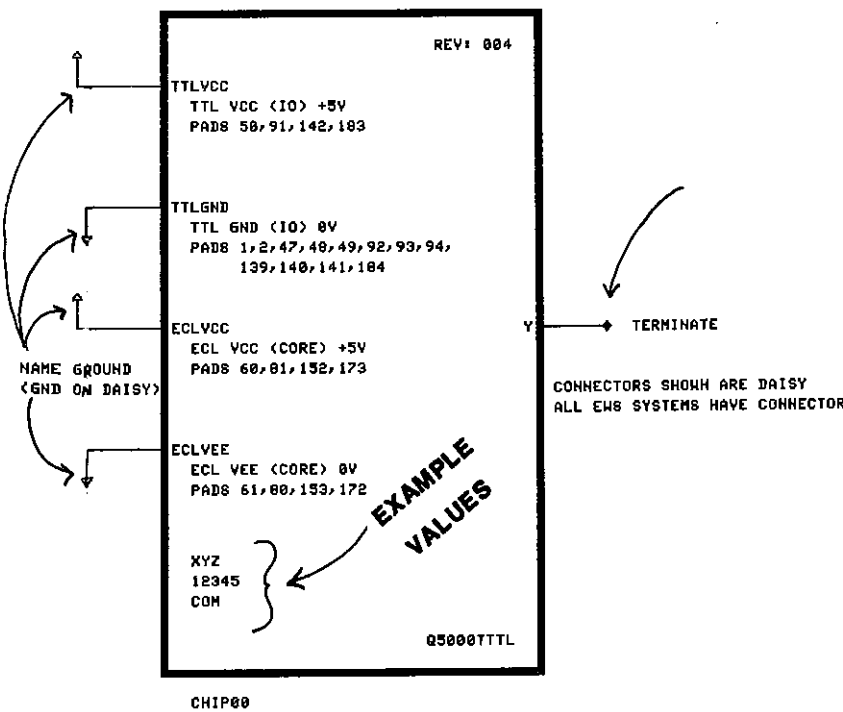
FOR SINGLE POWER SUPPLY +5V CIRCUITS; 100% TTL:

Q5000TTTL	FOR 100% TTL CIRCUIT ON A Q5000T
Q3500TTTL	FOR 100% TTL CIRCUIT ON A Q3500T
Q1300TTTL	FOR 100% TTL CIRCUIT ON A Q1300T
QM1600TTTL	FOR 100% TTL CIRCUIT ON A QM1600T

FOR SINGLE POWER SUPPLY CIRCUITS; 100% ECL:

Q5000TECL10K	FOR 100% ECL 10K CIRCUIT ON A Q5000T
Q3500TECL10K	FOR 100% ECL 10K CIRCUIT ON A Q3500T
Q1300TECL10K	FOR 100% ECL 10K CIRCUIT ON A Q1300T
QM1600TECL10K	FOR 100% ECL 10K CIRCUIT ON A QM1600T
Q5000TECL100K	FOR 100% ECL 100K CIRCUIT ON A Q5000T
Q3500TECL100K	FOR 100% ECL 100K CIRCUIT ON A Q3500T
Q1300TECL100K	FOR 100% ECL 100K CIRCUIT ON A Q1300T
QM1600TECL100K	FOR 100% ECL 100K CIRCUIT ON A QM1600T

SUPPLY = -5.2V, -4.5V, or +5V

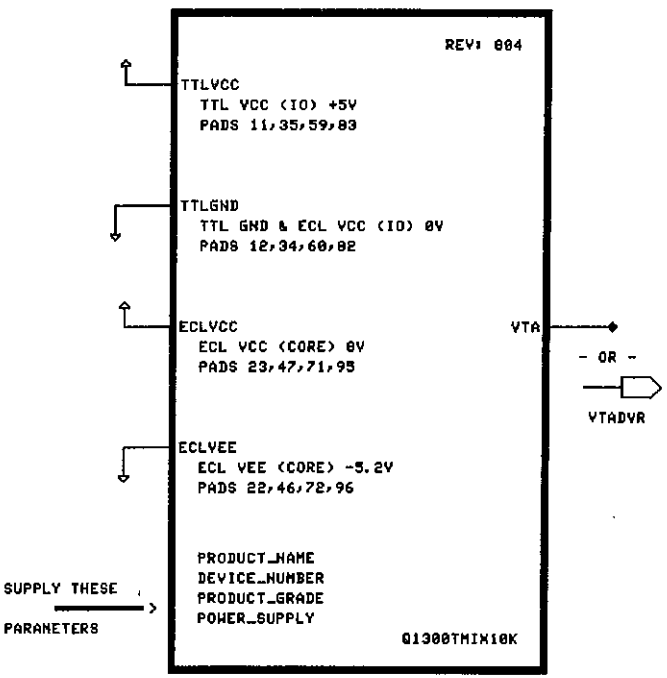


CHIP MACROS

FOR DUAL POWER SUPPLY CIRCUITS; ECL/TTL MIX:

Q5000TMIX10K FOR ECL 10K/TTL CIRCUIT ON A Q5000T
Q3500TMIX10K FOR ECL 10K/TTL CIRCUIT ON A Q3500T
Q1300TMIX10K FOR ECL 10K/TTL CIRCUIT ON A Q1300T
QM1600TMIX10K FOR ECL 10K/TTL CIRCUIT ON A QM1600T

Q5000TMIX100K FOR ECL 100K/TTL CIRCUIT ON A Q5000T
Q3500TMIX100K FOR ECL 100K/TTL CIRCUIT ON A Q3500T
Q1300TMIX100K FOR ECL 100K/TTL CIRCUIT ON A Q1300T
QM1600TMIX100K FOR ECL 100K/TTL CIRCUIT ON A QM1600T



BIXX MACROS REQUIRE VTA PIN - NONE RELEASED

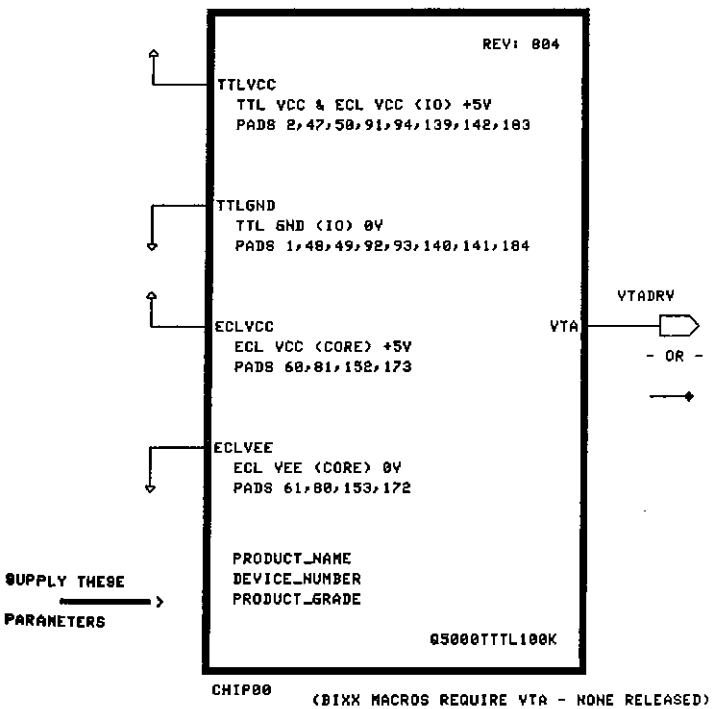
AMCC Q5000 MACRO LIBRARY SUMMARY - SPECIAL (804)

CHIP MACROS

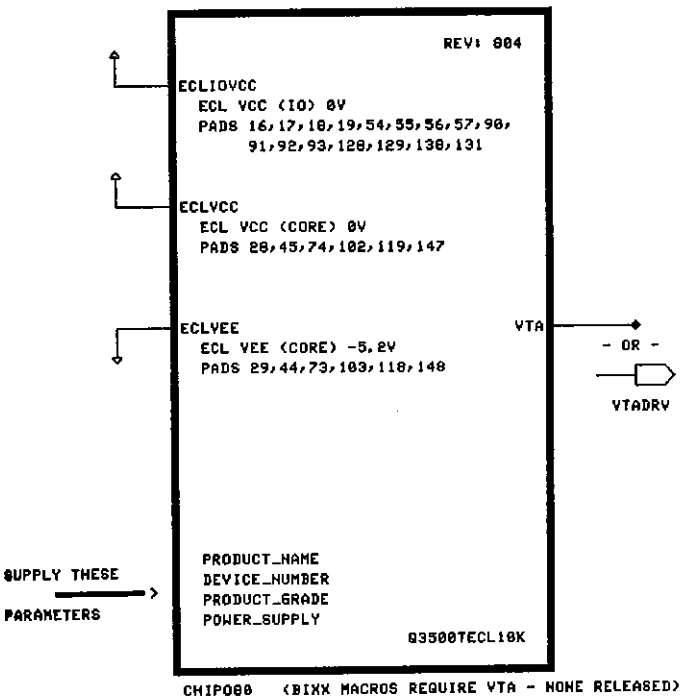
FOR SINGLE POWER SUPPLY +5V CIRCUITS; ECL/TTL MIX:

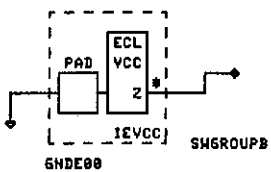
Q5000TTTL10K FOR +5V REF ECL 10K/TTL CIRCUIT ON A Q5000T
Q3500TTTL10K FOR +5V REF ECL 10K/TTL CIRCUIT ON A Q3500T
Q1300TTTL10K FOR +5V REF ECL 10K/TTL CIRCUIT ON A Q1300T
QM1600TTTL10K FOR +5V REF ECL 10K/TTL CIRCUIT ON A QM1600T

Q5000TTTL100K FOR +5V REF ECL 100K/TTL CIRCUIT ON A Q5000T
Q3500TTTL100K FOR +5V REF ECL 100K/TTL CIRCUIT ON A Q3500T
Q1300TTTL100K FOR +5V REF ECL 100K/TTL CIRCUIT ON A Q1300T
QM1600TTTL100K FOR +5V REF ECL 100K/TTL CIRCUIT ON A QM1600T



CHIP MACROS





STD REF ECL SYSTEM