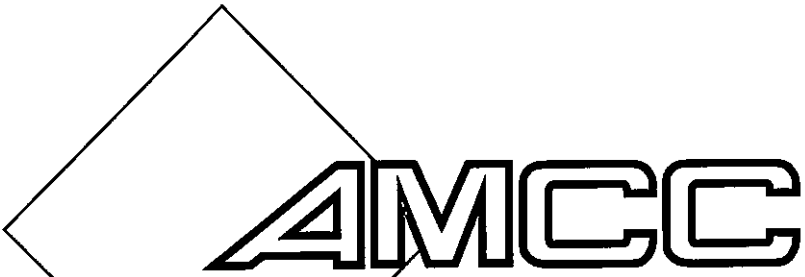

MacroMatrix® Design Manual

Volume I

Q20000 Series

Bipolar Logic Arrays

Applied MicroCircuits Corporation

(210)

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AMCC holds the patents for the Clock Driver Output, U.S. Patent 4,970,414. Japan Patent 2-177686.

AMCC holds the patents for the Turbo design: U.S. Patent 4,835,420; U.S. Patent 4,874,970; U.S. Patent 4,926,065.

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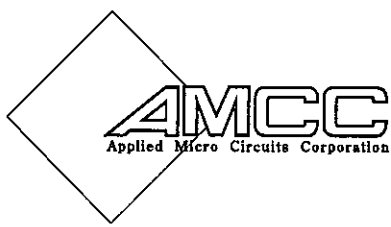
- Valid - Cadence Design Systems, Inc.
- Verilog - Cadence Design Systems, Inc.
- Synopsys - Synopsys, Inc.



AMCC
APPLIED MICRO CIRCUITS CORPORATION

November 15, 1992

Dear AMCC Customer:

We are pleased to provide you with an enhanced edition of our MacroMatrix design software. MacroMatrix has undergone several significant modifications to improve ease-of-use and design correctness that require your careful attention. Several new tools have been added for placement, packaging support, and design submission automation. Please refer to the accompanying MacroMatrix Newsletter for details.

MacroMatrix News also contains updated information regarding third party design tool support and steps needed to install and transition your design to this new release. Conversion of your existing MacroMatrix installation to this new installation should take no more than 1 hour. All designs submitted to AMCC after January 1, 1993, will have to use this new software for design verification (except Mentor 7.X users). No exceptions will be permitted. Customers planning to submit designs prior to that date have the option of continuing to use the previous software.

Included with this shipment are the new Volume 2 and Volume 3 of the AMCC MacroMatrix design manuals. These manuals supersede all previous versions of Volume 2 of the MacroMatrix Design Manual.

Should you have any questions regarding the appropriate usage of this new software release, please do not hesitate to contact any of our application engineers, sales representatives, or your assigned AMCC implementation engineer.

Sincerely,

Jeff Hilbert

Jeff Hilbert
ASIC Business Unit Director

6195 Lusk Blvd. □ San Diego, California 92121-2793 □ (619) 450-9333 □ FAX (619) 450-9885

From AMCC . . .

MacroMatrix News

October 1992

INTRODUCING RACECHECK

RaceCheck is a tool developed by AMCC for verifying that no problems exist in the test vectors to be used for automated test. RaceCheck incorporates **Teradyne's LASAR 6™** simulator into an easily executable form. A series of translators for getting data from AMCC generic format into LASAR format and back to AMCC generic format have been provided.

The entire process, including running LASAR and checking the results, has been encased into a shell that prompts the user for needed information and then submits the process to a job queue for actual execution.

WHY USE RACECHECK

Prior to the use of this type of tool, AMCC's experience showed that a number of designs required the presence of an AMCC implementation engineer at test in order to debug the test itself. This could impact delivery schedules. The use of this kind of tool by AMCC has virtually eliminated the need for debugging test patterns on the tester. The vector races can now be debugged on a simulator early in the design cycle where the process is much simpler and much faster.

Delays may be incurred due to the time it takes to send information back and forth between AMCC and our customers. Customer assistance is sometimes needed to help debug a problem, and customer approval is always required to make design or test vector changes. The placing of RaceCheck in the hands of our customers will reduce the time required to process an NRE after submission to AMCC and therefore improve the delivery schedule.

AMCCPACKAGE

The ***amccpackage*** software package provides direct on-line access to the AMCC Package Data Base on all AMCC-supported engineering work-stations and platforms. AMCC customers will now be able to interrogate the list of available packages by array type and technology at any point in the design process, and generate output files containing the pad to pin connections, power plane availability and pin capacitance information with or without a design netlist being present.

Once the design has reached the stage where a netlist has been created, ***amccpackage*** is used to check that the captured design will fit in the package selected. If the design does fit, then the ***amccpackage*** program will generate the ***output.dly*** file for use by the ***amccann*** annotation software program.

AMCCSUBMIT

The ***amccsubmit*** software package is a new program that is run hy the customer when their design is ready for submission to AMCC for processing; that is, after the design has been captured, simulated, and reviewed to the designer's satisfaction. ***amccsubmit*** simplifies the design submission process via its easy-to-use menu-driven style of data entry. ***amccsubmit*** is used by AMCC customers to describe all of the simulations and tests that must be performed to verify the "goodness" of the circuit design, whether the simulations involve functional tests, AC tests, parametric tests, or at-speed simulations. The design validation and customer description information also may be entered on the customer's work-station via this software package.

amccsubmit generates a clear and concise design submission report, simplifying the documentation and hand-off processes for both AMCC and our customers. ***amccsubmit*** is a major step forward in the pursuit of a paper-less and error free design submission process.

MENTOR 8.1

MacroMatrix software running under Release 8.0 from Mentor Graphics is under development for AMCC customers. There is a Mentor software bug which has delayed our conversion to Mentor 8.0. We are currently working with Mentor to resolve the issue and plan to release MacroMatrix on Mentor 8.1 late in 1992.

Synopsys Support

AMCC has added Synopsys synthesis support for the Q20000 Series of ECL/TTL Logic Array family. We have added a technology library for the Q20000 series for the Design Compiler tool from Synopsys, which is normally used for CMOS and BiCMOS designs. You do not need to purchase the separate ECL Design Compiler tool in order to apply logic synthesis techniques to your Q20000 array design! A set of "release notes" is available that describes in detail AMCC's support for Synopsys tools. The Q20000 library support adds to our previous support of Design Compiler for our Q24000 BiCMOS arrays.

PLL Arrays - CRU and CSU Macro and 8B/10B Functional Block Distribution

Not included in the normal library release tapes are the specialized macro functions for AMCC's Q20P010 and Q20P025 PLL arrays. Please contact AMCC for additional information on usage and distribution of CRU and CSU macros and other functional blocks, including certain non-disclosure requirements as applicable.

Changes to the Q20000 Library

The index to Section 6 - Macro Library Documentation - identifies changes made to individual macros. Some Tpd timing delays have been respecified. PW, fmax, k-Factors are respecified for some macros and they are identified in the index. A few new macros have been added.

For PLL macros, they are now documented as individual macros. However, they are not included in the release tape. Contact AMCC if you wish to use PLL macros.

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Macro Documentation
See index in Chapter 6

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SECTION 1
INTRODUCTION

Introduction to Volume I

This design manual provides a summary of the AMCC (Applied Micro Circuits Corporation) Q20000 Turbo Series Logic Arrays. Volume I is composed of the following sections:

It also includes information on:

- Product features
- Performance specifications
- Design Interface and support
- List of available macros

The AMCC Packaging Brochure should also be referenced for further information on packaging.

The Q20000 Series supports the arrays shown in Table 1-1.

TABLE 1-1 SUPPORTED ARRAYS	
Q20120	
Q20M100 **	
Q20080	
Q20045	PLL:
Q20025	Q20P025
Q20010	Q20P010
Q20004**	
	Q20P001**

** Advance Information

SUMMARY OF VOLUME I

Volume I of this three-volume design manual is intended as a self-contained design aid to allow the proper selection of an array for a particular design, to indicate the packaging available for that array, and to provide the designer with a better understanding of the capabilities of the Q20000 Turbo Series Bipolar Logic Arrays.

Section 2 contains design rules specific to this array series.

The macro summary and detailed macro specifications are presented in reference manual format in Section 6 with a rapid graphic reference provided by Quicksheets in Section 11. Either a macro-conversion of an existing design, or the direct design of a circuit can be implemented using the available macros.

SUMMARY OF VOLUME II

Volume II is intended to include all system-specific information for each workstation supported by AMCC.

Volume II of this design manual is composed of the following sections:

VOLUME II	
Section 1:	Introduction
Section 2:	System-Specific Design Methodology
Section 3:	MacroMatrix Installation and Operation Guide with system-specific design rules
Section 4:	Design Submission - Beyond ***amccsubmit***
Section 5:	***RaceCheck*** User's Manual
Section 6:	MacroMatrix News - This Release
Section 7:	Index

SUMMARY OF VOLUME III

Volume III includes all generic (system independent) information and Volume III is the same regardless of the workstation supported.

Volume III of this design manual is composed of the following sections:

VOLUME III	
Section 1:	Introduction
Section 2:	AMCC Schematic Rules and Conventions
Section 3:	Vector Submission Rules and Guidelines
Section 4:	***amccerc*** User's Guide
Section 5:	***amccpackage*** User's Guide
Section 6:	***amccann*** User's Guide
Section 7:	***amccvrc*** User's Guide
Section 8:	***amccsubmit*** User's Guide
Section 9:	AMCC Glossary
Section 10:	Index

Workstation and System Operation; EWS-Specific Rules; Installation of the Library And Patches

Volume II of this design manual contains the Engineering-workstation (EWS) or non-schematic entry system design methodology as applicable, covering both the system-specific rules and the operational commands of the AMCC MacroMatrix support software on the specific system.

Volume II also contains the MacroMatrix Installation and Operations manualS which summarize the system-specific commands required for operation of the AMCC support software. Library and patch installation procedures are also documented. Documentation is also provided for the use of the super shell *run_amcc,* Valid's *run_dir* , and the sub-shells:

SHELLS		
run_amccerc	*run_amccann*	*run_amccpackage*
run_amccsimfmt	*run_amccvrc*	*run_amccsubmit*
run_agif	etc.	

Design Validation Document

The Design Validation document previously used by AMCC has been incorporated into ***amccsubmit***. the program prompts are answered and the report submitted as part of the design submission package.

Design Submission Document

The Design Submission document has been incorporated into ***amccsubmit*** The program prompts are answered and the report submitted as part of the design submission package.

MacroMatrix User's Guides

Volume III contains the MacroMatrix User's Guides that detail the Engineering Rules Check (***amccerc***) software with error messages and probable causes; the Vector Rules Check (***amccvrc***) user's guide; the package selection (***amccpackage***) and the Annotation software and interface (***amccann***) user's guide; and the automated validation and submission software (***amccsubmit***) with a user's guide and examples.

Glossary, Index

Volume III also presents the AMCC glossary with definitions of terms and file identification. Each volume of the design manual contains an index for that volume.

TRADEMARKS

The following trademarks are recognized by AMCC throughout this design manual:

- Cadence - Cadence Design Systems, Inc.
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- LASAR Version 6 - Teradyne, Inc.
- MacroMatrix - Applied Micro Circuits Corporation (AMCC)
- Mentor - Mentor Graphics Corporation
- Sun - Sun Microsystems Corporation
- Valid - Cadence Design Systems, Inc.
- Verilog - Cadence Design Systems, Inc.
- Synopsys - Synopsys, Inc.

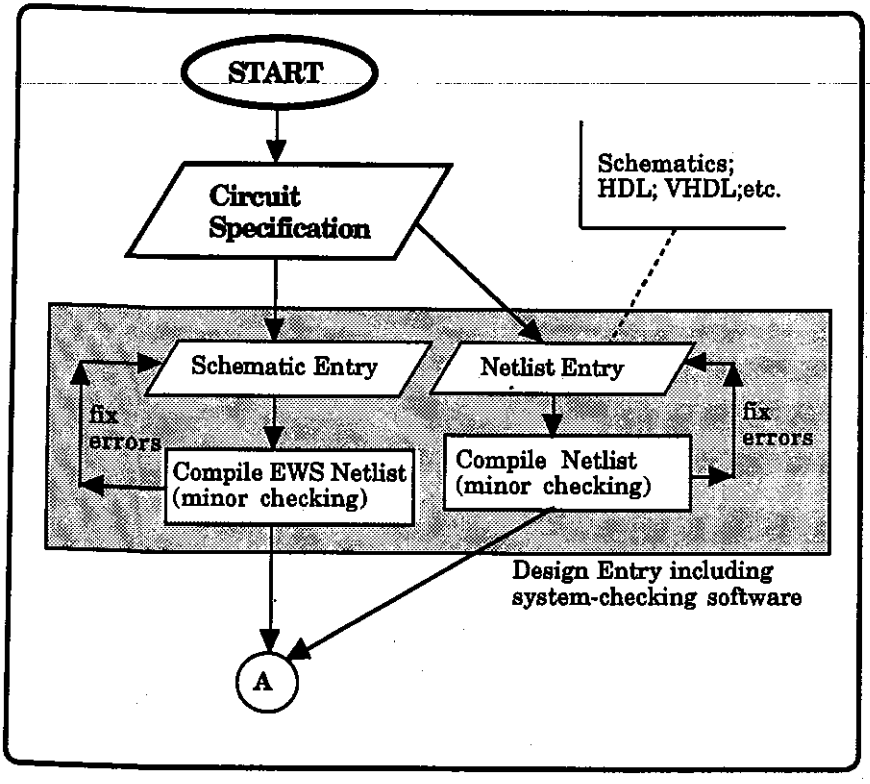

Figure 1-1a Creating the Netlist

DESIGN SUPPORT INTERFACE

Figures 1-1a-e provide an overview of the design interface and support offered by AMCC showing the various steps required in a typical design. The basic flow is unchanged for workstation or netlist-based submissions, with the exception of the creation steps.

Schematic Entry

Schematic entry can be performed by either the customer or by AMCC. Following schematic entry,the netlist must be generated. The netlist may be created via VHDL and other sources. If it is a netlist that AMCC software can recognize, the next step is to convert it into the AMCC Generic Interface Format or ***agif***. The resulting netlist is called ***circuit.sdi.*** This netlist is submitted as part of the design submission package.

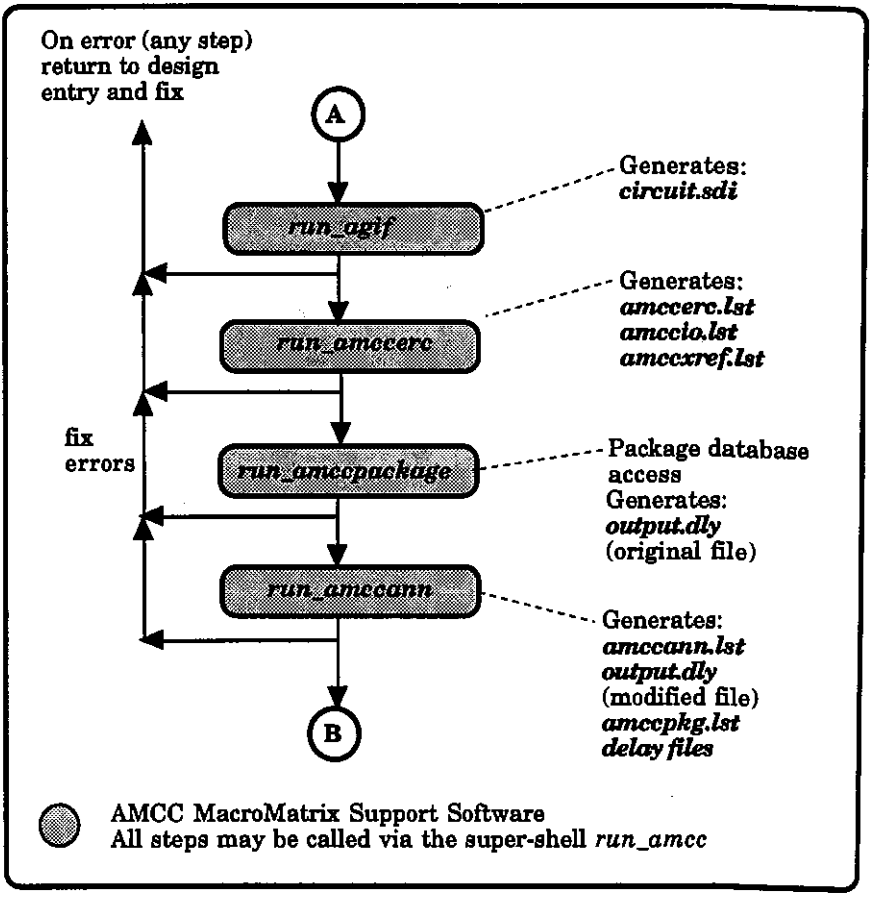

Figure 1-1b AGIF through *amccann*

AMCCERC

Following ***agif***, the AMCC Engineering Rules Checks software (***amccerc***) is run.

This software performs many of the design rule checks required for design verification. The design rules for the Q20000 array series are summarized in Section 2 of this design manual.

Performing ***amccerc*** early in the design cycle clears the circuit of trivial errors, identifies loading problems (fan-out report), provides DC power computation results, checks circuit size against cells available by type (population report), and allows circuit clean-up before time and effort are expended on simulations. The report is named ***amccerc.lst*** and is submitted. Note that ***amccerc*** may be executed against a partial circuit capture or even a macro list (collection of unwired macros). A chip macro must exist but there are no other requirements.

Partial circuit error screening is highly recommended. It is part of structured, modular design.

amccerc produces the I/O list report, ***amccio.lst***, which includes all pads on the array regardless of use. This report is submitted. A third report, ***amccxref.lst***, is a cross-reference listing. It may be submitted.

AMCCPACKAGE

When ***amccerc*** runs successfully, then a new software program, ***amccpackage*** is executed. AMCC has long added package delays to the annotation files. ***amccpackage*** allows the size of the package to be checked against the circuit size (new) and provides more accurate package delay information through access to the package database. It produces the datafile ***output.dly.***

Package information for the array series is discussed in Section8 of this design manual.

AMCCANN

On the completion of ***amccpackage***, the AMCC Annotation software, ***amccann***, is executed. ***amccann*** prepares delay files that are used during simulation. These delay files are either Front-Annotation delay or Back-Annotation delay files, depending on the existence of Place & Route data files in the directory. For a circuit which has just been captured, Front-Annotation files are produced. The report ***amccpkg.lst*** is also produced and is submitted.

amccann can produce delay files for the Dazix, Mentor and Valid native simulators as well as for Verilog and LASAR 6.

AMCC requires that simulations be performed with delay annotation files.

Timing analysis including computation of net interconnect delays using k-Factors is discussed in Section 3 of this design manual. External set-up and hold computation is discussed in Section 4.

Simulations

Simulations required and vector rules and guidelines are discussed in Volume III. An overview of testing requirements is discussed in Section 10 of VOlume I.

All of the simulators which AMCC supports work with the ***amccann***-produced delay annoation files. You must match:

Library used for simulation
Annotation file
Commands issued

The designer must develop the functional, at-speed, parametric and AC test simulation test vectors.

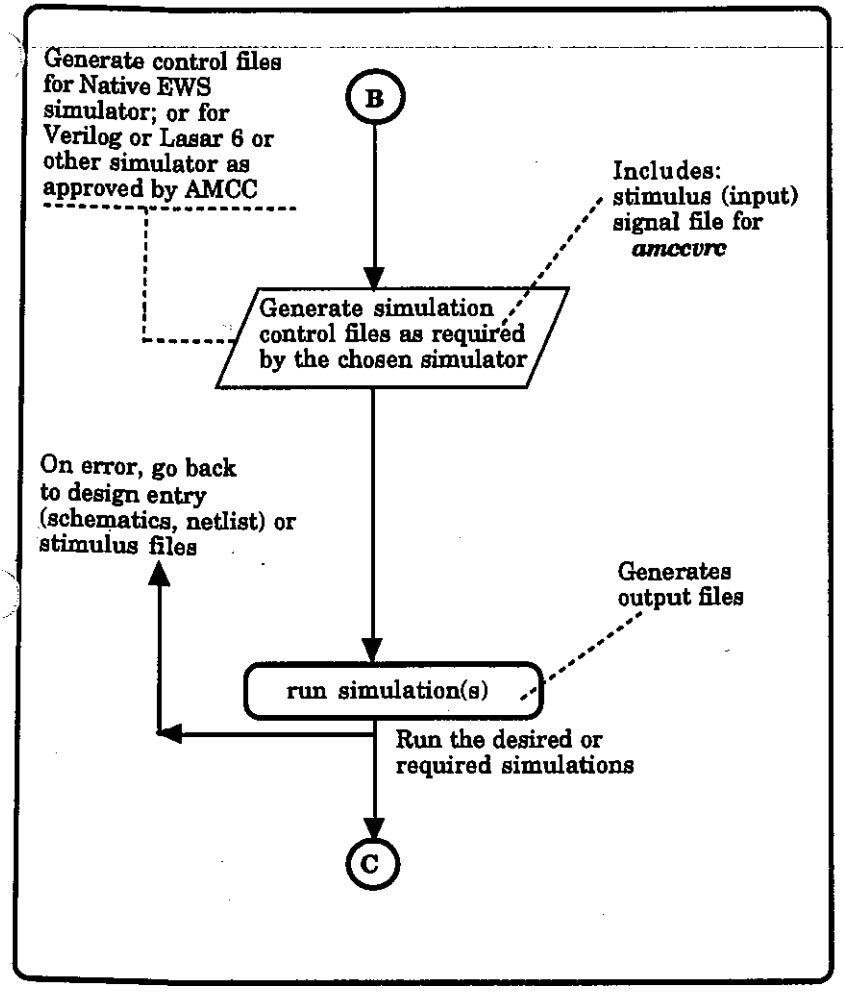

Figure 1.1c Simulations (Several are Required)

AMCCSIMFMT

Each simulator produces output files in a different format. Each simulation output file that is to be submitted to AMCC must be reformatted using ***amccsimfmt***. ***amccsimfmt*** converts the list output from the simulators into the list format recognized by AMCC vector software (***amccvrc***, ***amccsubmit***, ***RaceCheck***, and Test Transfer).

amccsimfmt is documented in Volume II of this design manual since it is system-specific.

RACECHECK

For functional vectors, both fault-grading (circuit coverage) and testability analysis (hardware coverability) are recommended steps. AMCC does not provide software to support these steps although several of the workstation vendors do. AMCC uses ***LASAR 6*** for Fault-Grading and will accept, on approval, fault grade scores from other simulator tools.

AMCC does provide ***RaceCheck***, which performs hazard and race checking on the functional vector sets. The use of ***RaceCheck*** is highly recommended by AMCC. It is not currently supplied as part of MacroMatrix. Contact your AMCC representative for information on obtaining ***RaceCheck*** for your system.

AMCCVRC

The maximum delay (worst-case maximum) sampled simulation output files, after reformatting with ***amccsimfmt***, must be processed through ***amccvrc***, the AMCC Vector Checking software. This applies to Functional, Parametric and AC-Test simulations. ***amccvrc*** supports the rules listed in the Vector Rules and Guidelines section.

AMCCSUBMIT

All of the design steps and the resultant files are documented prior to submission using ***amccsubmit***. This design submission support package replaces ***amcctest***, which was limited to AC test submission. New with this release, ***amccsubmit*** is intended to alleviate the paperwork required in performing a design submission.

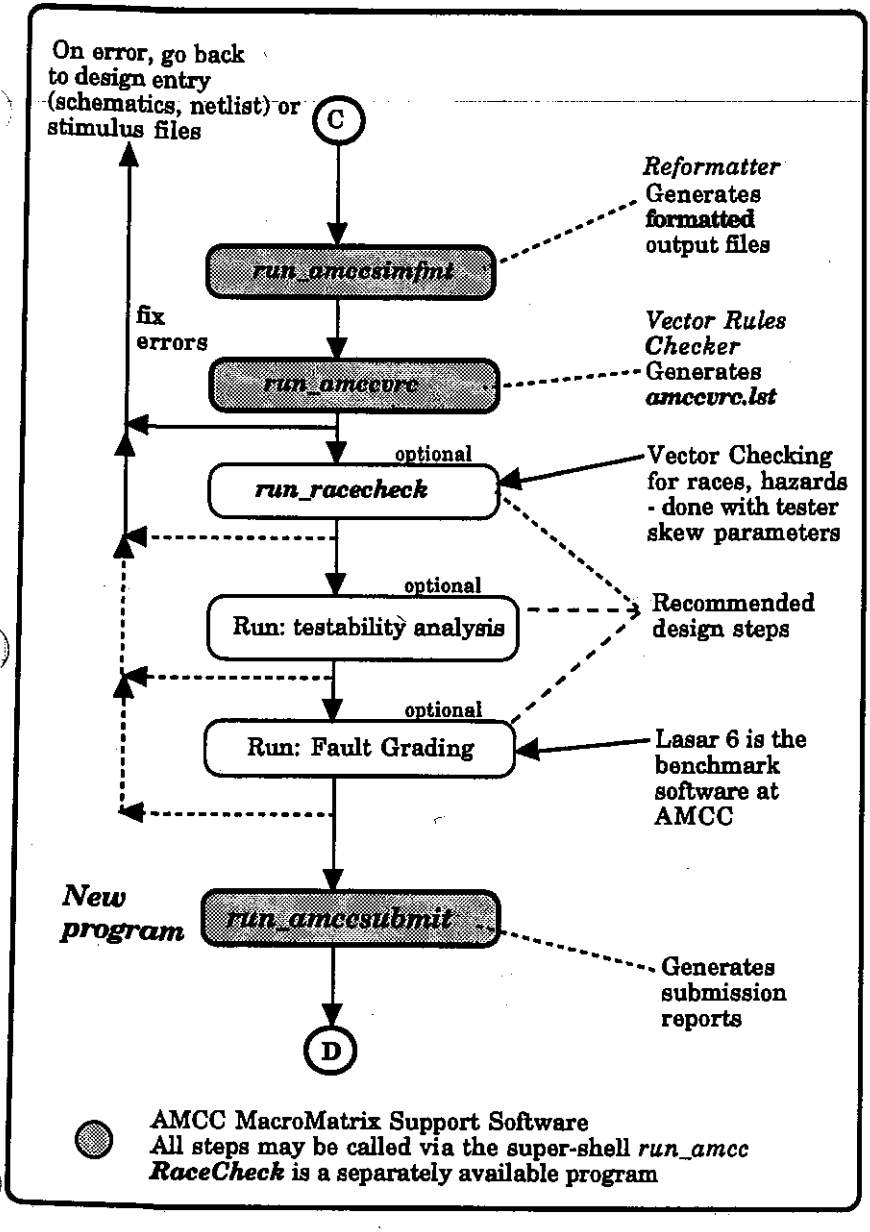

Figure 1.1d From Simulation Output Reformat to amccsubmit

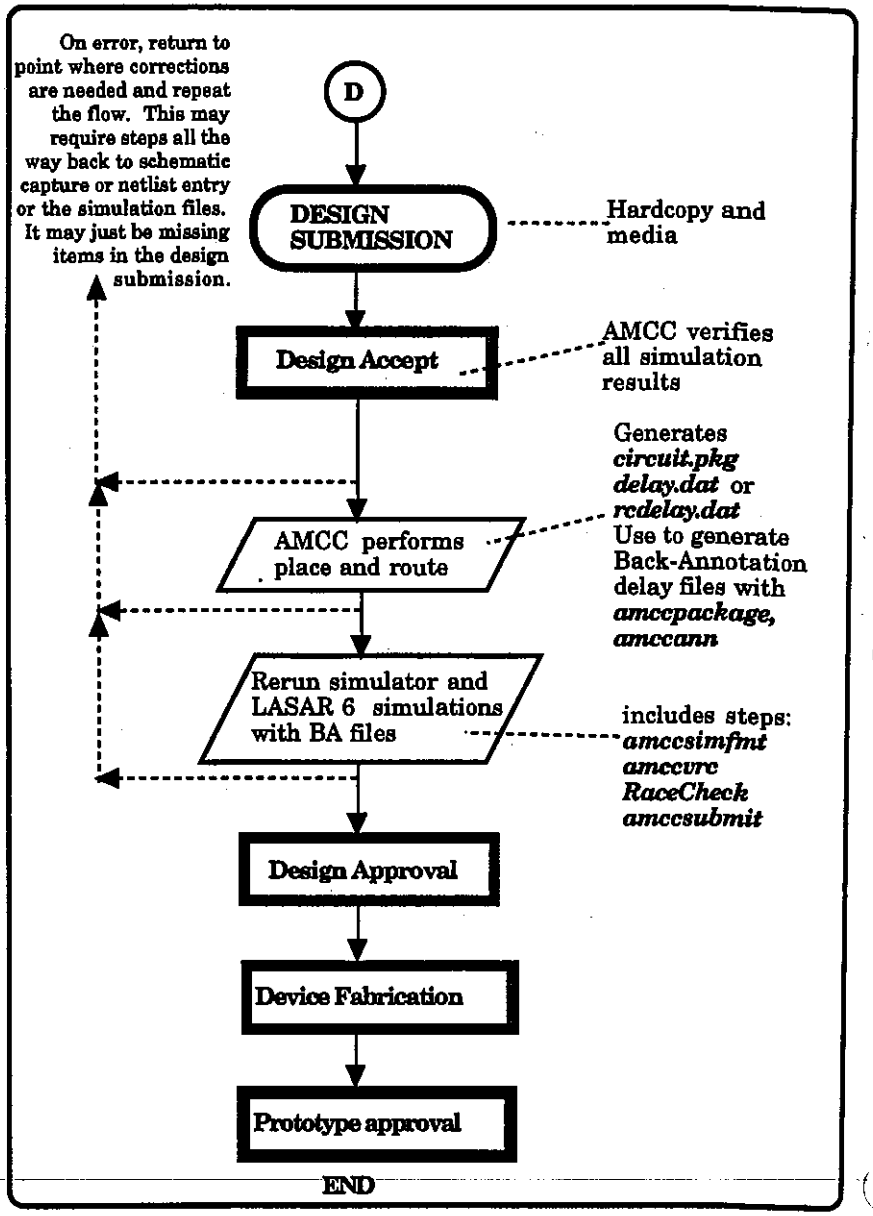

Figure 1.1e Design Submission Through Prototype Approval

Design Approval

Following design submission, AMCC Implementation or Field Application Engineers will re-execute all of the design steps and verify the design submission. They will be performed against the in-house library to ensure that the latest information on the macros is available.

Back-Annotation

On approval, the circuit will pass to layout using the AMCC Computer-Aided Design system, ***amccad***. After successful layout, the Back-Annotation delay files will be available for use in simulation. AMCC performs all simulations using Back-Annotation prior to prototype authorization.

Simulators

Note that AMCC performs all Back-Annotated simulations using the same simulator as was chosen by the customer. This is the "sign-off" simulator.

No "golden" simulator is employed. AMCC does, however, convert all designs and test vectors into the ***LASAR 6*** simulation environment for compre-hensive race and timing analysis.

LASAR 6 min-max simulation capabilities are used to identify test vector race conditions undetectable on the EWS simulator. These conditions would otherwise cause the device to fail in the actual ATE tester environment.

The test vector race conditions must be resolved prior to device fabrication.

Q20000 SERIES DESCRIPTION

The AMCC Q20000 Turbo Series Logic Arrays provide an optimized systems approach to very high performance ECL semi-custom applications. Mixed-mode I/O is combined with an advanced, interactive CAD system-based design approach to provide a quick and cost-effective solution to discrete IC replacement.

The Q20P025 and Q20P010 arrays incorporate an on-chip high-frequency phase lock loop (PLL). Frequency synthesis and clock recovery macros are available for these two arrays. This array list is being expanded with the addition of the Q20P001 PLL array.

Manufacturing advantages gained from the use of the AMCC logic arrays include:

- Increased circuit density
- Increased system speed
- Reduced power
- Higher reliability
- Lower system cost
- Operation over both military and commercial temperature ranges and power supplies

The AMCC Q20000 Turbo Series Logic Arrays Macro Library is supported on the DAZIX, Mentor Graphics and Valid Logic EWS, and the Lasar 6 simulator. Support for the Verilog logic simulator, the Synopsys Logic Synthesis System and the Cadence Design System are planned.

The designer can use any of these systems in conjunction with AMCC's MacroMatrix software package. to perform schematic capture, Engineering Rules Checking (***amccerc***), simulation, automatic test pattern formatting (***amccsimfmt***), AMCC Vector Rules Checking (***amccvrc***), Front-Annotation and Back-Annotation (***amccann***) and design validation and submission assist (***amccsubmit***).

Simulation, ***amccerc*** error checking, ***amccvrc*** rules checking, Front-Annotation and Back-Annotation are also supported on VAX/VMS systems with LASAR 6.

The Q20000 Turbo Series arrays are bipolar arrays. They can externally interface to either Schottky TTL, ECL 10K or ECL 100K. ECL 10K or ECL 100K may be standard-reference or +5V reference ECL.

As an added feature, the Q20000 Turbo Series provides the ability to mix ECL 10K and TTL or ECL 100K and TTL on the same array. ECL 10K and ECL 100K outputs are also allowed on the same array, regardless of the

ECL type used for input. For other combinations, please contact AMCC Marketing. (For specific output limits, refer to Volume I, Section 2.)

All the interface options are realized through the choice of appropriate macros, and personalized with the Metal and Via masks only.

Equivalent Gates - Relative Sizing

The number of equivalent gates possible is a sizing measure for the AMCC logic arrays, used to gauge the relative sizes of different arrays. An equivalent gate is loosely defined as a 2-input NOR gate for the bipolar arrays. A measure of design density is the number of these gates that would be required to construct the design in SSI logic.

To estimate the equivalent gate counts for the Q20000 Series arrays, a 3:1 MUX with a D F/F is defined as 11 gates and a full adder as 16 gates. The number of cells required for each of these macros and the number of cells available on the array lead to the equivalent gate count.

An I/O cell can be estimated as 2 gates but is not included in either of the gate counts shown in Table 1-2.

There is no AMCCERC check for equivalent gates. Equivalent gate counts may not be used in sizing for design submission.

Circuit Density

The actual circuit density obtained is a function of the design objectives, design approach and macros selected. The Q20000 Series uses 3-level series gating to maximize the logic density per switch.

A denser design is possible if the more complex macros are used first - start with cell-efficient, dense macros - keeping the use of SSI-level AND, OR, NOR, NAND gates to a minimum.

Designs with balanced delay path requirements use more cells than a minimized design; high-speed designs may use more cells if heavily loaded paths are to be broken up into parallel structures.

TABLE 1-2
SIZES OF THE AMCC BIPOLAR ARRAYS

ARRAY NAME	EQUIVALENT GATES	
↓	MUX F/F METHOD	Full Adder METHOD
Q20120	12500	17800
Q20080	8000	11000
Q20045	4500	6300
Q20P025	2150	3000
Q20025	2700	3800
Q20P010	650	900
Q20010	1000	1400

MACRO LIBRARY

The arrays in the Q20000 Turbo Series share a common macro function library that contains a wide selection of fully characterized logic functions varying from SSI to MSI densities. The higher functionality macros have correspondingly higher equivalent gate densities.

Examples of the basic logic functions include simple and complex gates, EXORs, latches, decoders, MUXs, buffered input, high-speed ECL input, buffers and output translation in the output macros, differential I/O, bidirectional I/O and 25 ohm ECL output drivers.

Many interface macros in the Q20000 Turbo Series macro library have high-speed (H) options in addition to the standard (S) option of the macro. Several macros have low-power (L) options. These macro options allow a designer to program critical paths with high-speed operation while implementing the remainder in lower power or standard-option macros.

TYPICAL APPLICATIONS

Typical applications include high-speed computers, graphics, communications, test equipment and instrumentation. Designed to operate in the full MIL-SPEC temperature and voltage range, the Q20000 Turbo Series also has applications in radar, EW, avionics, guidance, flight simulation and other military systems. The PLL arrays are designed for data communications, tele-communications and timing generation applications.

FEATURES

A summary of the features of the Q20000 Turbo Series includes:

- On-chip high-frequency phase lock loop with edge jitter as low as 50 ps
- Industry's first channelless Bipolar array
- Up to 3414 internal cells
- Up to 198 I/O cells
- One micron bipolar process incorporating polysilicon emitters, trench isolation, and an advanced base emitter structure
- 3-level metal interconnection allows 100% routing at > 95% cell utilization - PLL arrays up to 100%
- 3-level series gating
- High-speed < 100 ps equivalent gate delays
- Up to 1.2 GHz Operating Frequency
- Ft = 18 GHz
- High internal noise immunity
- Symmetrical rise and fall times
- Ultra low power < 0.5 mW/internal gate
- Speed-power programmability with S-, L- and H-options for the macros
- Power supply variation stability
- Unused cells do not dissipate power
- Fully voltage- and temperature-compensated internal logic
- No separate termination supply needed (e.q. -2 or -3.3V) for internal (core) operation, simplifing power supply and board design
- Single cell ECL 25 and 50 ohm parallel termination drive
- Low off-chip delay penalty
- TTL, ECL 10K and ECL 100K I/O compatibility
- Both ECL 10K and ECL 100K outputs may appear on the same array
- Dual supply mixed ECL/TTL I/O capability
- Standard reference ECL; VEE = -5.2V or -4.5V
- +5V reference ECL
- On-chip speed monitor
- On-chip thermal diode
- On-chip translators for mixed mode interface
- Full CAD support, including post-autoroute and worst-case timing analysis
- Autoplace and autoroute with up to 95% logic cell utilization
- Supported on leading EDA tools

DAZIX	Verilog (Future)
Valid Logic	Lasar
Mentor Graphics	

- Full Commercial and Military compatibility

Section 2
Design Methodology

Design Methodology

TECHNOLOGY

The Q20000 Turbo Series of ultra-high performance ECL/TTL logic arrays are fabricated using a one micron bipolar process incorporating trench oxide isolation (TOI) and an advanced base emitter structure.

The Q20000 Turbo Series incorporates an on-chip thermal diode pair and an on-chip AC speed monitor. These two circuits use a total of four fixed-location pads which must be connected to external package signal pins.

ARRAY ARCHITECTURE

The Q20000 Turbo Series is the first ECL logic array family to utilize a channelless architecture called Sea-of-Cells. Using triple-layer metal, there are no dedicated routing channels between cells, allowing core density to be increased by 40%. Internal cell utilization is maintained at greater than 95% due to three layer metal interconnect and AMCC's proprietary state-of-the-art place and route system.

The AMCC logic arrays are formed from a customer-specified design added to an AMCC pre-processed silicon base array. The base arrays for the Q20000 Turbo Series are composed of two types of cells, I/O and logic cells. Each cell consists of a number of uncommitted transistors and resistors.

First level metal is used for macro intra-connect, the construction of the macro logical function from the base array components. The second and third levels of metal are used for inter-macro routing, the macro interconnections to form the desired circuits. Power and ground distribution is also done on the first, second and third layers of metal.

The basic cell layout of the arrays is demonstrated with the Q20080 die plot, shown in Figure 2-1. Refer to Section 7, Placement, for other example array die plots.

Note: placement is not to be attempted using these drawings. If a placement worksheet is required, consult AMCC Applications Engineering.

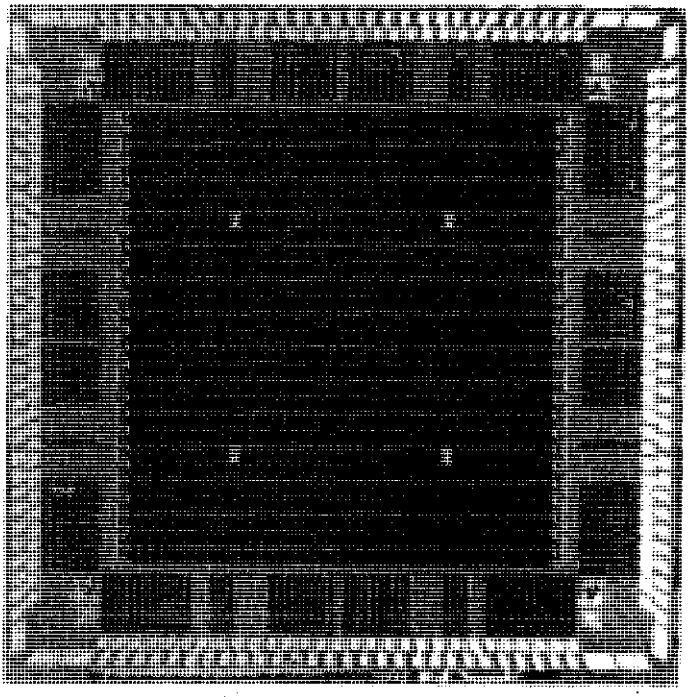

Figure 2-1 Q20080 Die Plot
Light squares in core area are reference generator cells. All internal core cells are called "L-cells". Groups of cells around the perimeter are the I/O cells.

PLL ARRAY DESCRIPTION

The AMCC Q20P010 and Q20P025 logic arrays are two products with densities of 928 and 3120 equivalent gates with a high frequency phase-locked loop on-chip. Combining a PLL with user-definable Q20000 series arrays, the Q20P010 and Q20P025 are tailored for high speed serial communication, video, and clock generation applications. (See Figure 2-2.)

Frequency synthesis and clock recovery macros are available for the on-chip phase-locked loop. Speed options ranging from below 200MHz to 1.25GHz are available for simulation on AMCC supported engineering workstations. Lock detect, local and link loopback features are also selectable options.

For the digital logic portion of the array, an extensive library of SSI and MSI macros is available as part of the AMCC MacroMatrix design kit. Latches, parallel-to-serial converters, encode/decode functions, high speed shift registers, bit error rate computation and divide-down counters can easily be assembled to operate in conjunction with the phase-locked loop to meet specific application needs.

Digital Logic

The Q20000 Series is the industry's first ECL logic array family to utilize a channelless architecture called **Sea-of-Cells**. The Sea-of-Cells organization eliminates the dedicated routing channels between cells thereby doubling the core density. Utilization is maintained at greater than 95% due to three layer metal interconnect and the AMCC proprietary state-of-the-art place and route system. A full complement of SSI and MSI macros is offered with low power, standard and high speed options.

To insure effective operation of the Q20P010 and Q20P025, especially in low jitter applications, the digital logic must operate synchronously with the PLL.

Phase-Locked Loop Macros

A selection of frequency synthesis and clock recovery macros are available for the on-chip phase lock loop. Speed options of 125, 132, 155, 200, 265, 311, 500, 531, 622, 1000, 1062 and 1244 MHz are selectable to operate synchronously with the logic in the digital portion of the array. Additional frequency options can be created to meet specific design requirements. AMCC defined loop filter components for each frequency option have been established for applications with divide ratios up to 64, transition densities of 30% - 70%, and run lengths up to 50 bit times. For different loop filter parameters contact AMCC. Lock detect, local and link loopback features are also available options.

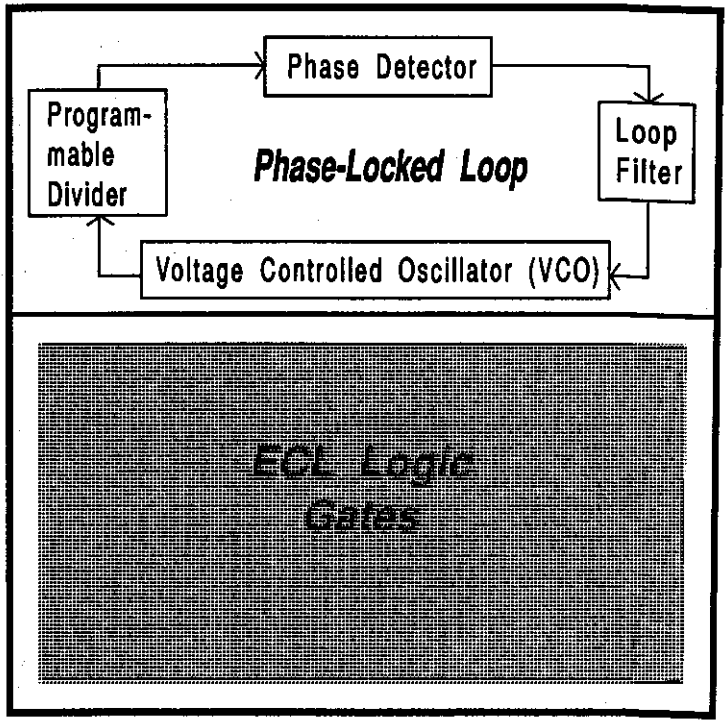

Figure 2-2 Phase-Locked Loop

Encoding/Decoding

High speed datacom and telecom applications frequently require a standard encoding scheme to ensure favorable bit stream characteristics and interoperability. AMCC initially offers two encoder/decoder schemes as standard macro options in the library. Popular in datacom applications, IBM's 8B/10B encoding scheme offers DC-balance and short run lengths in an efficiently architected implementation. Frequently used in fiber-based telecom systems, a 2^7-1 scrambler function is also offered. Other preferred encoding and decoding schemes can easily be designed using the digital portion of the Q20P010 and Q20P025.

Flexible I/O Structure

The Q20P010 and Q20P025 array I/O cells are configurable to provide a flexible range of interface options. The I/O cells are designed to interface with standard (-5.2V or -4.5V) and positive reference (+5V) ECL 10KH and ECL 100K or TTL thresholds. The mixed ECL/TTL capabilities allow interface to both technologies on a single chip without the use of external translators. On-chip 50W termination is provided to facilitate low jitter interfaces. For dual power supply devices, the I/O are also capable of a Darlington-type ECL output which provides significant improvement in drive capability, toggle frequency, and power dissipation over standard ECL outputs. TTL outputs selected for use with the Q20P010 and Q20P025 must be the slower edge-rate, 8 ma type to minimize noise injection into the PLL area and should be placed on the opposite side of the chip from the PLL to the extent possible.

ARRAY CELL RESOURCES

Table 2-1 summarizes the cell resources; Table 2-2 lists the fixed pads for the thermal diode and AC speed monitor, and Table 2-3 summarizes the power-ground resources for the Q20000 logic array series. Figure 2-2 provides a die plot for the Q20080 array.

Turbo Driver

To overcome the power problems of conventional ECL structures, AMCC developed a patented dynamic discharge circuit in place of the traditional static current source for the emitter follower. The power requirements of Turbo macros are significantly lowered from those with conventional circuitry.

Off-chip skews for ECL 10K and ECL 100K outputs are improved as are their extrinsic (t_{ex}) loading delays.

I/O cells can be configured with a Darlington output stage and Turbo to allow a single-cell 25-ohm ECL output for use on dual-power supply circuits.

TABLE 2-1
I/O AND INTERNAL CELL RESOURCES

Array Name	Internal Cells	I/O Cells (for signals)	I/O Cells (fixed) *	I/O Signals-PLL Related
Q20120	3414	198	4	N/A
Q20080	2044	162	4	N/A
Q20045	1233	128	4	N/A
Q20P025	595	51 **	4	12
Q20025	733	100	4	N/A
Q20P010	177	34 **	4	12
Q20010	267	66	4	N/A

* 2 pads are used by the AC Speed Monitor and 2 by the thermal diode.
** Only for the largest arrays, 100_LDCC for the Q20P010 and 132_LDCC for the Q20P025
Add last three colums to find total I/O cells and pads.

Array Name	ECL Outputs Limit	TTL Outputs Limit	PLL Power/ Ground	Digital Power/ Ground
Q20120	172	100	N/A	78
Q20080	130	80	N/A	52
Q20045	100	64	N/A	52
Q20P025	51	51	8	26
Q20025	80	48	N/A	36
Q20P010	34	34	8	20
Q20010	50	24	N/A	32

Add last two colums to find total number of fixed power and grounds.

TABLE 2-2
FIXED PAD NUMBERS FOR THERMAL DIODES AND AC-SPEED MONITOR

ARRAY NAME	THERMAL DIODE		AC SPEED MONITOR	
	CATHODE PAD #	ANODE PAD #	VEE PAD #	ECL PAD #
Q20120	207	208	12	34
Q20080	161	162	9	33
Q20045	136	137	4	25
Q20P025	97	93	3	26
Q20025	103	104	3	26
Q20P010	88	87	10	24
Q20010	74	75	10	24

TABLE 2-3
POWER-GROUND PAD RESOURCES *

I/O MODE: ↓ TOTAL PWR / GNDS:		Q20120	Q20080	Q20045	Q20025	Q20010
		78	52	52	36	32
100% ECL, single supply	core GND (*)	20	16	16	8	8
	core V- (**)	18	16	16	8	8
	I/O GND (*)	40	20	20	20	16
100% ECL dual supply	CORE GND (0V)	20	16	16	8	8
	CORE V- (**)	18	16	16	8	8
	I/O V+ (+5V)	8	4	4	4	4
	I/O GND (0V)	32	16	16	16	12
ECL/TTL MIX, dual supply	CORE GND (0V)	20	16	16	8	8
	CORE V- (**)	18	16	16	8	8
	I/O V+ (+5V)	8	4	4	4	4
	I/O GND (0V)	32	16	16	16	12
ECL/TTL MIX, single supply	CORE GND (0V)	18	16	16	8	8
	CORE V+ (+5V)	20	16	16	8	8
	I/O V+ (+5V)	28	16	16	16	12
	I/O GND (0V)	12	4	4	4	4

* For a detailed list, see AMCCIO.LST

TABLE 2-3
POWER-GROUND PAD RESOURCES *CONTINUED*

I/O MODE: ↓	TOTAL PWR/ GNDS:	Q20P025	Q20P010
		47	30
ECL/TTL	CORE GND (0V)	10	6
MIX	CORE V- (**)	16	11
DUAL	I/O V+ (+5V)	2	2
SUPPLY	I/O GND (0V)	19	11
ECL/TTL	CORE GND (0V)	10	6
MIX	CORE V+ (+5V)	16	11
SINGLE	I/O V+ (+5V)	19	11
SUPPLY	I/O GND (0V)	2	2

** CORE V: -5.2V for STD-REF ECL 10K
-4.5V for STD-REF ECL 100K
0V for +5V-REF ECL 10K or ECL 100K
* CORE GND: 0V for STD-REF ECL 10K or ECL 100K
+5V for +5V-REF ECL 10K or ECL 100K

Macro Configuration

A customer design is described via schematics using the macros contained in the released library for the array series. Macros are individually configured in an array by interconnecting the components within a cell with the first layer metal to form the customer-selected macro functions. Macro placement is performed automatically by the AMCC proprietary CAD software (***amccad***).

Interconnections and Routing

Interconnections between macros (routing) use both the second and third layers of metal, following specific routing tracks. Routing is performed automatically by AMCC proprietary CAD software.

Additionally, the AMCC CAD software has been designed to automatically transform a logic design implemented in AMCC macros into an efficient high performance layout design. If there are sensitive timing and/or skew constraints, AMCC can optionally offer preplacement of the macros implementing these critical areas.

The customization of the array is performed by adding the 3-layer metal interconnect, representing the macros and their interconnection, to the base array.

Logic Cells

The internal logic cells are organized to support high-level logic functions such as latches, multiplexors, decoders, etc. Simple and complex gates can also be made from these cells. The internal cells (L cells) support the Turbo circuitry, allowing internal Turbo macros to support an 18-load fan-out load limit.

I/O Cells

The interface to the arrays is accomplished in the input/output cells on the Q20000 Turbo Series Logic Arrays. The I/O cells are located around the perimeter of the array. For all arrays, ECL- and TTL-translators and most of the required buffers are included in the I/O cells for external interfacing to both ECL and TTL. Each individual I/O cell is configurable to be either TTL, ECL 10K or ECL 100K.

Overhead Circuitry

In addition to the cells, each array contains overhead circuitry: bias generators, voltage references and voltage regulators. Overhead circuitry is predefined by AMCC.

MACRO PAD NAMES - CHANGES

AMCC has changed its naming conventions for macro input and output pad names. Instead of "PAD", look for PI, PI2N, PO, PON and variations to indicate input, inverting input with more than one input on the macro, output, and inverting output respectively. Designers with designs-in-progress at this release will need to update their schematics.

INTERFACE OPTIONS

The array itself can be configured to be 100% ECL 10K, 100% ECL 100K, TTL/ECL 10K or TTL/ECL 100K, with dual power supplies, or 100% ECL or TTL/ECL 10K or TTL/ECL 100K with a single +5V supply. (See Table 2-4.) In addition, both ECL 10K and ECL 100K outputs may be used on any given array. Only one type of ECL is allowed for input, defined by the chip macro.

TABLE 2-4
POWER SUPPLY OPTIONS*

	SINGLE POWER SUPPLY			DUAL POWER SUPPLY	
	+5V	-5.2V	-4.5V	+5V/-5.2V	+5V/-4.5V
100% ECL 10K	Y	Y	Y	Y	Y
100% ECL 100K	Y	Y	Y	Y	Y
ECL 10K/TTL	Y	—	—	Y	Y
ECL 100K/TTL	Y	—	—	Y	Y

* ECL 10K can be operated at ECL 100K voltages and visa versa; consult AMCC concerning DC parametrics. For 100% TTL, consult AMCC

Interface Guidelines

A summary of the interface guidelines for the three I/O modes of operation is shown in Figure 2-3. Most of the I/O macros for the Q20000 Turbo Series include buffer functions, to simplify I/O selection. The designer should review the I/O options to determine where these options would enhance the circuit efficiency.

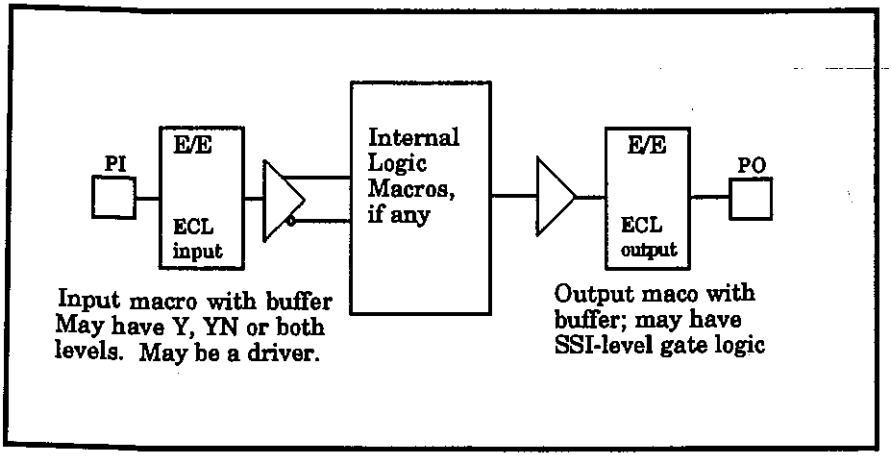

Figure 2-3a
Q20000 Series Interface Macro Guidelines
100% ECL Interface
Dual +5V And -5.2V
Or +5V And -4.5V Power Supplies
DECL

Q20000 SERIES INPUT

- Use ECL interface macros (IExx, UExx, UKxx)
- ECL input macros contain buffers
- Same macro for either +5V/-5.2V or +5V/-4.5V paring

Q20000 SERIES OUTPUT

- Use ECL interface macros (OExx, OKxx, UExx, UKxx)
- ECL available to drive 50 ohm and 25 ohm off-chip terminations
- ECL output macros contain necessary buffers
- Supports both ECL 10K (OExx, UExx) and ECL 100K (OKxx, UKxx)
- Supports single-cell 25 ohm output
- Supports Darlington outputs

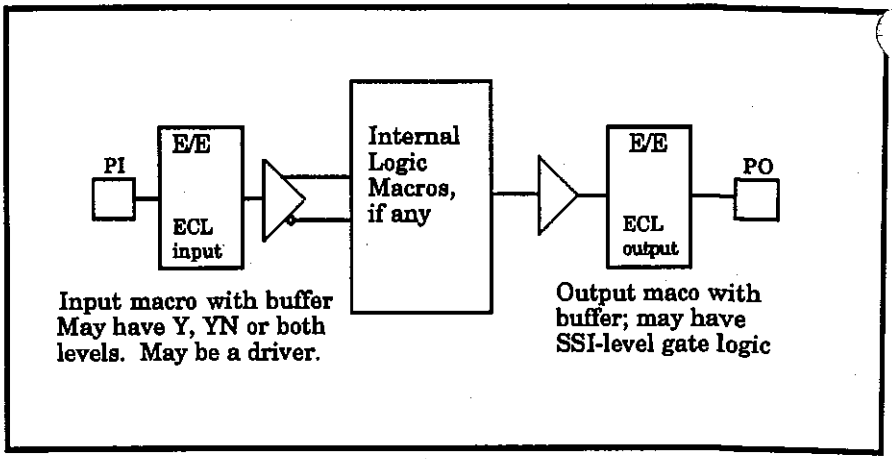

Figure 2-3b
Q20000 Series Interface Macro Guidelines
100% ECL Interface
-5.2V -4.5V Or +5V
Single Power Supply

Q20000 SERIES INPUT

- Use ECL interface macros (IExx, UExx, UKxx)
- ECL input macros contain buffers
- Same macro for either +5V, -5.2V or -4.5V single supply

Q20000 SERIES OUTPUT

- Use ECL interface macros (OExx, OKxx, UExx, UKxx)
- ECL available in 50 ohm and 25 ohm
- ECL output macros contain necessary buffers
- Supports both ECL 10K (OExx, UExx) and ECL 100K (OKxx, UKxx)
- Does NOT support single-cell 25 ohm output
- Supports 2-cell 25 ohm output
- Does NOT support Darlington outputs

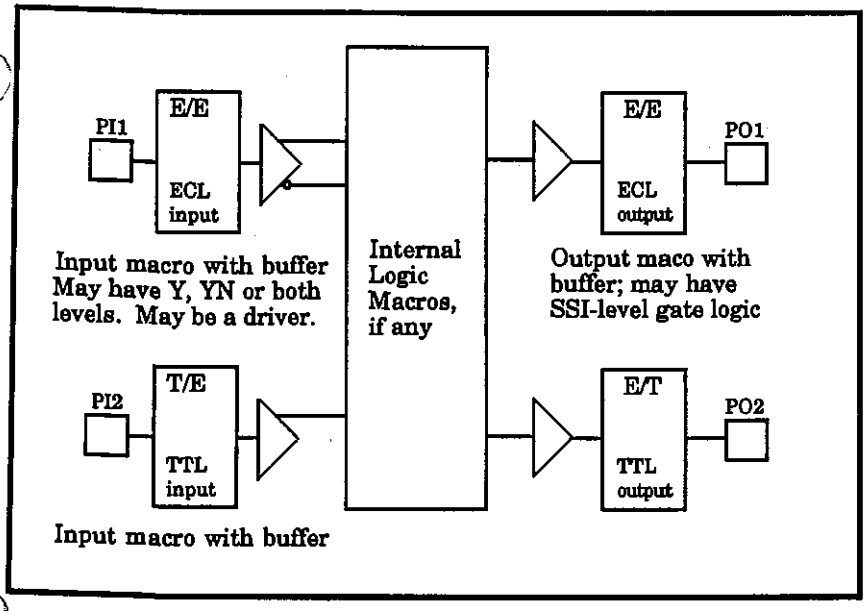

Figure 2-3c
Q20000 Series Interface Macro Guidelines
Mixed ECL/TTL Interface
Dual +5V and -5.2V
or +5V and -4.5V Power Supplies

Q20000 SERIES INPUT

- Use TTLMIX interface macros for TTL (ITxx, UTxx)
- Use ECL interface macros (IExx, UExx, UKxx)
- Input macros contain buffers
- Same macro for either +5V/-5.2V or +5V/-4.5V power supply paring

Q20000 SERIES OUTPUT

- Use TTLMIX interface macros for TTL (OTxx, UTxx)
- Use ECL interface macros (OExx, OKxx, UExx, UKxx)
- ECL available in 50 ohm and 25 ohm
- Output macros contain necessary buffers
- Supports both ECL 10K (OExx, UExx) and ECL 100K (OKxx, UKxx)
- Supports single-cell 25 ohm output
- Supports Darlington outputs

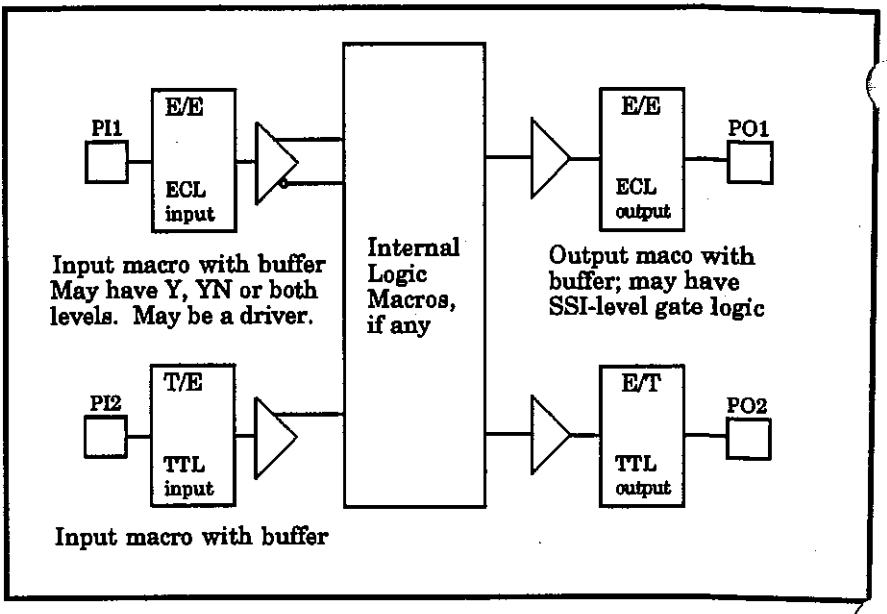

Figure 2-3d
Q20000 Series Interface Macro Guidelines
Mixed ECL/TTL Interface
Single +5V Supply

Q20000 SERIES INPUT

- Use TTL interface macros for TTL (ITxx, UTxx)
- Use ECL interface macros (IExx, UExx, UKxx)
- Input macros contain buffers

Q20000 SERIES OUTPUT

- Use TTL interface macros for TTL (OTxx, UTxx)
- Use ECL interface macros (OExx, OKxx, UExx, UKxx)
- ECL available in 50 ohm and 25 ohm
- Output macros contain necessary buffers
- Supports both ECL 10K (OExx, UExx) and ECL 100K (OKxx, UKxx)
- Does NOT support single-cell 25 ohm output
- Supports two-cell 25 ohm output
- Does NOT support Darlington macros

MACRO SUMMARY

Refer to the macro summary and index (Section 6) for a list of the macros available for the Q20000 Turbo Series Logic Arrays. The library and its summary sheets are for use during macro conversion or when creating a new design directly from the available functions. If other macro functions are desired, please consult AMCC.

The macro summary in Section 6 is divided into five segments: TTL Interface, TTLMIX Interface, ECL Interface, Logic Macros, and Special macros. The macros are in alphabetical order within those sections. The library is divided into two parts, the MIL5 library and the COM5 library, within each section.

I/O MACROS

Interface macros are documented in Sections 6-1, 6-2 and 6-3. All signals going on or off the chip require the use of an appropriate interface macro.

TABLE 2-5
I/O MACRO DOCUMENTATION INDEX

Section	Interface Macro Type
6-1	TTL for 100% TTL or ECL/TTL mix, single supply
6-2	TTL for ECL/TTL, dual power supplies
6-3	ECL, any

For dual power supply circuits, the TTL macros are selected from the TTLMIX section, Section 6-2. The ECL macros are selected from the ECL section, Section 6-3. The same ECL macros are available for use with standard reference voltage or for +5V reference voltage circuits, except for the Darlington ECL outputs which are allowed only on dual supply circuits.

TTL Input (ITxx macros)

Q20000 Turbo Series TTL input macros contain input buffers. TTL level detection is performed in this input macro. For circuits with a single +5V power supply, the buffer provides the signal buffering required to drive internal circuits. For dual power supply circuits, the buffer also provides signal translation from TTL input levels to the internal ECL signal level needed by the array, which operates between ground and the negative power supply.

TTL Output (OTxx macros)

The Q20000 Turbo Series arrays provide 20mA or 8mA current sink unless documented as otherwise in the individual macro documentation. (See Section 6.)

The Q20000 Turbo Series arrays handle TTL totem-pole, open-collector and 3-stated output options. The 3-state TTLMIX output macro enable pin may be driven by any internal-level logic signal (the output of an input or internal logic macro). The 3-state TTL output macro enable pin must be driven by a 3-state enable-driver macro signal. In either case, the signal driving the enable pin must be named on the schematic and must be listed in the simulation signal format.

- There is a limit on the number of TTL outputs that can be placed on the Q20000 arrays. Refer to the cell resource table for specific limits.
- The AMCC MacroMatrix ERC population report will show an error if more than the allowed TTL output macros are used for the Q20000 Turbo Series arrays.
- Only 8mA controlled edge rate TTL outputs may be used on PLL arrays. If you want to use other TTL output, you must consult AMCC and obtain pre-approval. For 8 mA controlled edge rate outputs, consult AMCC.

Bidirectional TTL (UTxx macros)

Bidirectional TTL I/O is supported. The input and output functions follow the same design methodology as the ITxx and OTxx macros. The TTLMIX bidirectional macro enable pin may be driven by any internal-level logic signal (the output of an input or internal logic macro). The TTL bidirectional macro enable pin must be driven by a 3-state enable-driver macro signal. In either case, the signal driving the enable must be named on the schematic and must be listed in the simulation signal format.

ECL Input (IExx macros)

ECL input macros contain an RC compensation network and an input buffer. ECL inputs function in the same manner on circuits which have +5V referenced ECL input with a single +5V power supply.

- ECL inputs are all either 10K or 100K.
- ECL inputs do not have pull-down resistors and must not float in any application.

ECL Output (OExx, OKxx macros)

All ECL outputs require a buffer, and the buffer is included in the output macro. The Q20000 Turbo Series ECL output buffers drive 50 or 25 ohm ECL outputs. If an output is designed for a different termination, it is referenced in the macro documentation.

ECL output macros are grouped by logic function in Section 6. A specific version of the macro (OExx or OKxx) is selected based on ECL type.

TABLE 2-6
ECL MACRO SELECTION Matrix

	ECL 10K		ECL 100K	
	+5V REF	GND REF	+5V REF	GND REF
INPUTS	IExx	IExx	IExx	IExx
OUTPUTS	OExx	OExx	OKxx	OKxx
Bi-direc.	UExx	UExx	UKxx	UKxx

- There are no placement restrictions due to both ECL 10K and ECL 100K outputs appearing on the same circuit.

- There may be parametric deviations when both ECL 10K and ECL 100K appear on the same circuit (due to non-standard voltages being used).

- There is a limit on the number of ECL outputs that can be placed on the Q20000 arrays. Refer to the cell resource table for specific limits.

- The AMCC MacroMatrix ERC population report will show an error if more than the allowed ECL output macros are used for the Q20000 Turbo Series arrays.

Darlington ECL outputs

The Q20000 Turbo Series allows for a special type of ECL output macro which incorporates a patented Darlington output configuration. These macros maintain standard ECL 10K/100K output levels, while netting an improvement in drive capability and toggle frequency over standard ECL outputs.

- Darlington ECL output macros require dual power supplies of +5 and either -5.2V or -4.5V.

- The Darlington output macros will accomodate 25 or 50 ohm loads in a single I/O cell.

A special chip macro, "DECL" for dual-supply ECL, should be used to allow AMCC MacroMatrix ERCs to provide error checking. Current drain on the VCC +5V supply in DECL is very minimal.

CML Outputs (Open Collector)

The Q20000 Turbo Series arrays allow differential CML outputs. Very high frequency signal paths (>600MHz up to 1.2GHz) should use CML (or Darlington) outputs. When terminated with 50 ohms to ground, these macros maintain a typical 500mV output swing under DC conditions. These outputs must be terminated off-chip.

On-Chip Series Terminated Outputs

On-chip series terminated outputs will be provided in a later release. Consult AMCC if they are required prior to their scheduled release.

Bidirectional ECL (UExx, UKxx macros)

Bidirectional ECL I/O is supported with two I/O cells. The input and output functions follow the same design methodology as the IExx and OExx/OKxx macros. The macro enable pin may be driven by any internal-level logic signal (the output of an input or internal logic macro). The signal driving the enable pin must be named on the schematic and must be listed in the simulation signal format.

The bidirectional macros may contain added power/ground (IEVCC).

+5V Reference ECL/TTL

AMCC offers the option of having ECL 10K or ECL 100K available with the use of a single +5V power supply in a 100% ECL or ECL/TTL mixed mode circuit. The ECL logic threshold levels are shifted, but retain their high-speed characteristics. This +5V referenced ECL mode allows the partitioning of a high-speed TTL design into multiple AMCC devices using a single +5V supply, while providing *high-speed ECL I/O between the arrays on the same PC board* and full system TTL compatibility.

Alternative ECL Terminations

The standard ECL termination is 50 ohms tied to VTT, where VTT = -2.0V for standard reference ECL. An alternative termination is 80 ohms to ground with 130 ohms to VEE where VEE = -5.2V. For other termination configurations, consult AMCC.

CHARACTERIZING THE ARRAY - THE CHIP MACROS

The AMCC EWS schematic convention for the specification of the array and its I/O mode, power supply, product grade, and circuit identification (MILitary or COMmercial) is through the use of a **chip macro.** The chip macros carry additional array-specific information used by AMCC MacroMatrix software in processing the design.

The chip macro ***power_supply*** parameter allows the user to specify single supplies of -5.2V (STD5), -4.5V (STD4) or +5V (5VREF) for 100% ECL circuits. The chip macro selection specifies the dual supplies of +5V and -5.2V or +5V and -4.5V, or single supply of +5V for ECL/TTL mixed circuits. For the Q20000 Turbo Series, the "DECL" chip macros identify a circuit as 100% ECL with dual power supplies. The ***power_supply*** parameter STD5 and STD4 values also apply to the DECL chip macros.

Refer to *EWS Schematic Rules and Guidelines* (Section 2 in Volume III) for placement and hook-up procedures. Volume I, Section 6-5 also documents the chip macros and their parameters.

Refer to Section 6-INDEX for a list of chip macros.

AMCCERC Technology Check

The AMCC MacroMatrix ERC technology report will list errors due to improper selection of macros based on the I/O mode selected via the chip macro.

Fixed Power and Ground Placement

amccio.lst (from ***amccerc***) and ***amccpkg.lst*** (from ***amccann***) provide a detailed listing of the fixed power and ground pad usage for the array and I/O mode. Signals cannot be placed on the pads designated as being fixed power or ground pads. All fixed power and ground pads must be used. Fixed power and ground pads provide the minimum number of power and grounds for the array.

Any power and ground pads added by the user are in addition to the fixed power and ground requirements.

TABLE 2-7
CHIP MACROS AND I/O MODES

CHIP MACRO	ALLOWED INPUT TYPE	ALLOWED OUTPUT TYPE	DEFAULT SUPPLY
QxxxxxECL10K *	ECL10K	ECL10K, ECL100K	-5.2V
QxxxxxECL100K *	ECL100K	ECL10K, ECL100K	-4.5V
QxxxxxDECL10K	ECL10K	ECL10K, ECL100K	-5.2V,+5V
QxxxxxDECL100K	ECL100K	ECL10K, ECL100K	-4.5V,+5V
QxxxxxMIX10K	ECL10K, TTL	ECL10K, ECL100K TTL	-5.2V,+5V
QxxxxxMIX100K	ECL100K, TTL	ECL10K, ECL100K, TTL	-4.5V, +5V
QxxxxxTTL	CONSULT AMCC		
QxxxxxTTL10K *	ECL10K, TTL	ECL10K, ECL100K TTL	+5V
QxxxxxTTL100K *	ECL100K, TTL	ECL10K, ECL100K, TTL	+5V

Substitute 20120, 20080, 20045, 20025 or 20010 for xxxxx.
For PLL arrays substitute 20PI010 or 20PI025
PLL arrays allowed I/O Modes: MIX10K, MIX100K, TTL10K, or TTL100K

POWER_SUPPLY ON THE ECL10K AND ECL100K CHIP MACROS CAN BE SET TO BE STD5 (-5.2V), STD4 (-4.5V) or 5VREF (+5V).

POWER SUPPLY ON THE DECL10K, DECL100K, MIX10K, AND MIX100K CHIP MACROS CAN BE SET TO BE STD5 OR STD4.

* Darlington macros cannot be used on single-supply circuits.

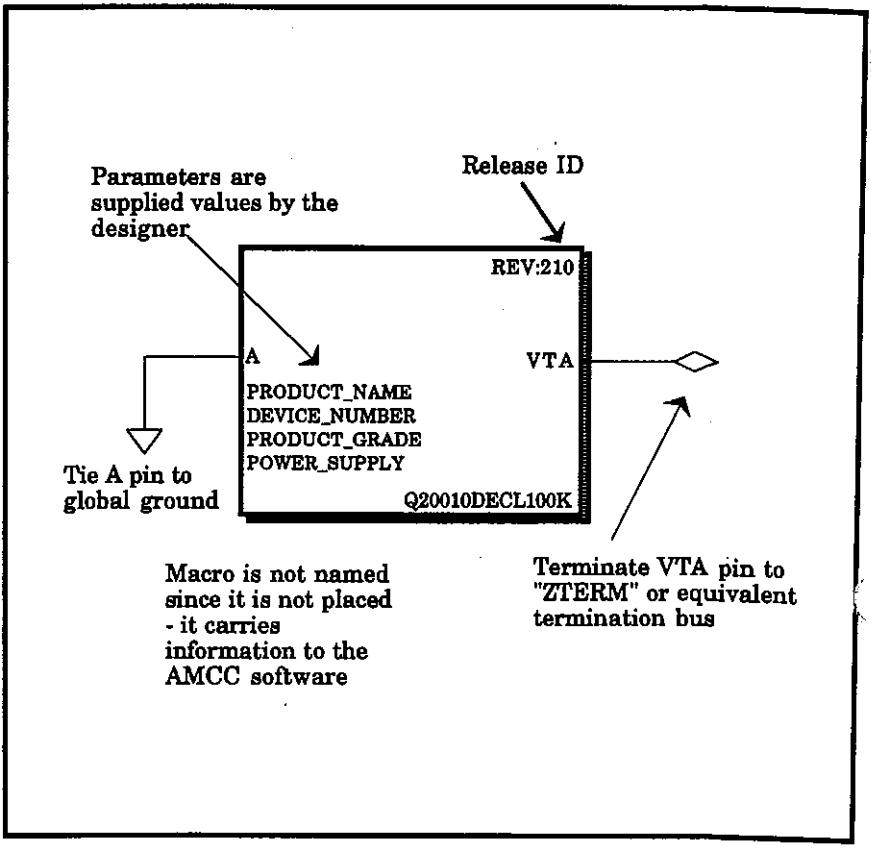

Figure 2-4 Sample Chip Macro (wired)

AC Speed Monitor Fixed Pads

The AC speed monitor is part of the base array and must be used. It requires two pads, supply and output, listed in ***amccio.lst*** and ***amccpck.lst***.

The monitor is built from the same cells used in the array core. A 9-stage ring oscillator followed by a 2-stage divide-by-4 counter forms the basis of the AC speed monitor as shown in Figure 2-5.

Each of the stages of the ring oscillator section incorporates over 100 mils of second and third layer metal in order to accurately include the effects of metal loading. The resulting output is simulated using annotated simulation models. [E.g., same as for any circuit modeled on the array.]

The automated test equipment used by AMCC is accurate to 0.005% up to 100 MHz. The AC monitor is designed to generate 40 MHz output signal well within the bounds of the tester's measurement tolerances. By using this counter and the AC speed monitor, AMCC can easily and quickly guarantee all projected AC delay paths in any customer implementation.

The pads from the monitor must be bonded out in the package. Allow two package signal pins for the monitor.

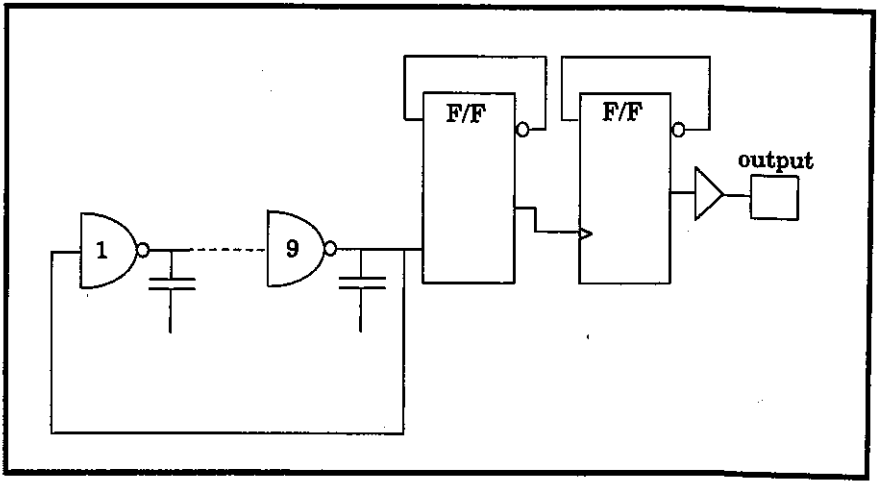

Figure 2-5 AC Speed Monitor

Thermal Diode Fixed Pads

The thermal diode that is part of the base array must be used. It requires two pads, anode and cathode, listed in ***amccio.lst*** and ***amccpkg.lst***. The pads from the thermal diodes must be bonded out in the package. Allow two package signal pins for the thermal diode.

POWER BUSSES AND ADDED POWER AND GROUND

The power busses supporting the internal array are isolated from the busses supporting the peripheral I/O cells to minimize the effect of noise coupling between the core and the I/O. The TTL and the ECL ground busses are kept isolated on the chip.

When necessary, there are macros available to provide extra TTL power (ITPWR), TTL ground (ITGND), and ECL power or ground (IEVCC), depending on the reference voltage.

Added power and grounds are required for output switching and for high-speed signal isolation, e.g., when a high-frequency CMOS signal is used to drive a TTL input. Use the IEVCC (ECL ground) for ECL isolation.

Adding Extra Power and Ground - IEVCC

The Q20000 Turbo Series Logic Arrays require that extra ECL VCC pads be added when the number of simultaneously switching ECL 50 ohm outputs exceeds four (4) for any output group. Add an IEVCC macro for each group of four (4) simultaneously switching ECL outputs after the first four (4). These must be interspersed within the switching group.

Non-50 ohm outputs are equated to 50 ohm outputs as follows:

- ECL 25 ohm outputs count as two (2) 50 ohm outputs.
- ECL 50 ohm differential outputs count as one (1) 50 ohm output.

The IEVCC pad should be placed to allow connection to the internal package plane and not to an external pin, when internal planes are available. Consult AMCC for IEVCC placement restrictions if you are doing preplacement.

The designer must use the SWGROUP macro parameter (property) on all simultaneously switching output macros and on the IEVCC macros added per the equation below. Failure to tag the added IEVCC macros can result in SSO error messages.

Use the following method to compute the number of IEVCC required:

$$\text{Estimate:} \quad \left| \frac{\text{number of equivalent ECL 50 ohm SSOs} - 1}{4} \right|$$

Note that in +5V ECL or ECL/TTL mixed circuits, IEVCC is considered to be power. It is considered to be ground for all other cases.

TABLE 2-8
ADDITIONAL IEVCC

	# OF SIMULTANEOUSLY SWITCHING ECL PER GROUP	ADD ECL VCC
50 ohm ECL in any system; 100% ECL or mixed mode	0 - 4	0
	5 - 8	1
	9 - 12	2
	13 - 16	3
	17 - 20	4

Adding Extra Power and Ground - ITPWR, ITGND

The Q20000 Turbo Series Logic Arrays require that extra TTL PWR and TTL GND pads be added when the number of simultaneously switching TTL 8mA outputs exceeds eight (8) for any output group. Add a TTL power-ground pair (ITPWR, ITGND) for each group of eight (8) simultaneously switching TTL outputs after the first eight (8). These must be interspersed within the switching group.

Non-8 mA outputs are equated to 8 mA outputs as follows:
- A TTL 20mA output counts as two (2) 8mA outputs.

The power-ground pads should be placed to allow connection to the internal package plane and not to an external pin, when internal planes are available. Consult AMCC for IEVCC placement restrictions if you are doing preplacement.

The designer MUST use the SWGROUP macro parameter (property) on all simultaneously switching output macros and on the ITPWR and ITGND macros added per the equation below. Failure to tag the added power and ground macros can result in SSO error messages.

Use the following to estimate the number of TTL power and ground pairs.

$$\text{Estimate:} \quad \frac{\text{number of equivalent TTL 8mA SSOs} - 1}{8}$$

TABLE 2-8 *continued*
ADDITIONAL ITPWR, ITGND

	# OF SIMULTANEOUSLY SWITCHING TTL PER GROUP	ADD TTL PAIRS:
50 ohm ECL in any system; 100% ECL or mixed mode	0 - 8	0
	9 - 16	1
	17 - 24	2

There are no quadrants on the Q20000 arrays.

Estimate one added ground or power pad between ECL and TTL groups and between ECL input and ECL output groups for isolation.

Q20000 arrays do not use "quadrant" grouping as applied to other AMCC array series.

Outputs are grouped together, SSOs or not.

Specifying Additional Power and Ground

When additional power and ground pads are desired, the power macros, ITPWR or IEVCC, and the ground macros, IEVCC or ITGND, are placed on the schematic in the quantity desired. IEVCC will be considered a power pad for +5V REF ECL circuits and a ground pad for STD REF ECL circuits.

Cell Efficient Macros

The added power and ground macros each occupy one I/O cell and use its pad. Inclusion of the requirements for extra power and ground is part of the required design submission documentation.

For cell efficiency, the TTL bidirectional macro UT31 is paired with an ITGND and the ECL bidirectional macro UE54 is paired with an IEVCC.

SWGROUP Parameter/Property

Whether or not added power and ground has been added for simultaneously switching outputs, use the macro parameter or property SWGROUP to tag these macros to the group to which they belong.

Refer to Volume II, Section 7 for the EWS-specific instructions on how to attach ***swgroup*** to a macro.

Added Power and Ground Placement

Added power and ground pads must be interspersed with the simultaneously switching signals during placement.

They should be placed on pads that allow connection to an internal package power or ground plane whenever physically possible, to avoid the use of an external package pin for these macros.

The ***amccerc.lst*** population report will list the maximum and minimum number of package signal pins that will be required by the circuit, the difference being the number of added power and ground macros. The actual number of package signal pins required will depend on the final placement.

MACRO PIN FAN-IN LOADING

The fan-in of the input pins on a macro are listed in the macro documentation in Section 6. Asterisks (*) are no longer used to indicate high fan-in. Always refer to Section 6.

INTERNAL FAN-OUT

Each internal macro output pin is specified to drive a maximum fan-out load. Maximum fan-out limits are specified for individual macros in the macro documentation in Section 6. The fan-out ERC checks for excessive fan-out loading.

Derating Fan-Out Limits

For clock or distortion-sensitive paths, at speeds up to 600 MHz, the maximum fan-out for each macro output pin in the path must be derated by 20%. For clock paths at speeds equal to or greater than 600 MHz, the maximum fan-out should be derated by 40%. The fan-out ERC will check for a derated fan-out load limit if the ***FOD*** net parameter (property) has been used.

AMCC requires the use of the ***FOD*** net parameter on all clock nets.

TABLE 2-9
DERATING GUIDELINE

OPERATING SPEED:	DERATE BY:	FOD VALUE
< 600 MHz	20%	20
≥ 600 MHz	40%	40

STATIC SIGNALS

When an internal macro has an unused input pin without hook-up restrictions, it can be tied to global ground or driven to a logical 1. Pins that are tied to global ground are tied low automatically by the AMCC CAD system. The transistor base is strapped to the emitter to assure that the device stays off (see Figure 2-6).

Pins that must be driven high can use either an L-option macro or a static driver.

Connection to global ground is not counted in the internal pin count. Connection to a static driver is counted.

To help the designer, the AMCC MacroMatrix ERC Hook-up check will detect improper interconnects made with global ground.

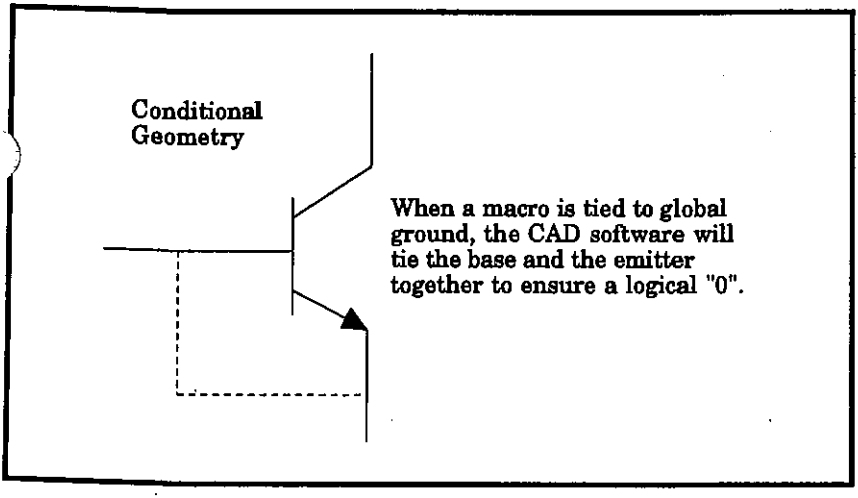

Figure 2-6 Effective Global Ground

INTERNAL CELL UTILIZATION

To insure routability, the recommended maximum internal cell utilization (cell population) for arrays in the Q20000 Turbo Series is 95%. Starting designs should target ~70% internal cell utilization to allow for ~20% design expansion during debug, re-design, enhancement, and testing logic additions.

Internal cell Utilization limit = 95%

Designs in excess of 95% internal cell utilization for these arrays are considered risky if their internal pin count also exceeds recommended limits or if other placement requirements exist that could cause conflicts.

Compute actual internal cell utilization by first summing the number of logic cells used by the circuit, and then by dividing that sum by the number of logic cells available for the particular array.

AMCC MacroMatrix ERC software computes the internal cell utilization. The software generates a warning if cell utilization exceeds recommended limits or an error if it exceeds 100%.

Note: Circuit sizing using "equivalent gates" may not be used in the design submission.

INTERNAL PIN COUNT LIMIT

The internal pin count is another measure of the routability of a circuit on a given array.

- Prior to schematic capture, the internal routable pin count should be estimated and used in the selection of the required array. A guideline for estimate limit is 80% of the captured circuit limit. See Table 2-10.
- After capture, the AMCC MacroMatrix ERC software provides a detailed report on the internal pin count of the circuit. For a captured circuit, refer to the limits in Table 2-10.

TABLE 2-10
MAXIMUM INTERNAL PIN COUNT LIMITS
I/O AND L CELLS

ARRAY	ACTUAL LIMIT	ESTIMATED LIMIT
Q20120	7548	6038
Q20080	4586	3668
Q20045	3097	2478
Q20P025	1555	1244
Q20025	1883	1507
Q20P010	453	362
Q20010	733	586

AMCC MacroMatrix Internal Pin Count ERC reports on the following conditions:

- A circuit with an actual internal pin count that is less than the limit is routable.
- A circuit with an actual internal pin count that is 1-10% over the limit is considered risky (may have problems).
- A circuit with an actual internal pin count of 11-18% over the limit is considered very risky and may not successfully route.
- A circuit with an actual internal pin count of 18% or more over the limit is considered unroutable and a redesign is required if a larger array cannot be used.

- Unused macro input pins - EWS convention is to ground any unused inputs unless the macro documentation indicates that a pin cannot be grounded. (Signals tied to global ground will be tied down via AMCCAD. The base input will be tied with conditional geometry to the emitter, assuring that the device stays off.)

- Hook-up restrictions - For those macros which must be driven, drive by a macro or use the static driver GT87 (50 loads).

- Pin connections - Make certain that all macro input and output pins are properly connected, including PAD connections.

- Bidirectional signals - Be certain that bidirectional macro pins have been connected to a bidirectional connector (EWS convention). Refer to the EWS-specific portion of the Design Manual for additional information. For VALID, use the work-around for simulations. Do not use the work-around pages when generating *circuit.sdi* or when running AMCCERC. Note: Mentor and Dazix simulators do not require a workaround.

- Grounded output pins - These are not allowed.

- Terminated input pins - These are not allowed.

- Macro type - Check that the proper TTL I/O macros were chosen based on the circuit type.

- Macro type - Check that the proper ECL versions of the ECL macros were chosen based on the circuit type.

- Macro type - Check that Darlington macros are used only on dual-supply circuits.

- Macro type - Use CML or Darlington ECL outputs for signals over 600MHz.

- PLL Macros - One and only one PLL macro may appear on a PLL array (Q20P025 or Q20P010)

- Differential ECL output - Use the dual-cell differential outputs when the speed is greater than 600MHz.

- TTL output on PLL arrays: Use edge-controlled 8mA TTL outputs. Consult AMCC for these outputs.

- Signal names - Check that all connections - intra-page, inter-page, off-chip and 3-state and bidirectional enables - have been properly named. Refer to Volume II, Section 3 for naming conventions and rules.

- 3-state enable drivers - The enable for TTLMIX and ECL BIDIs and TTLMIX 3-state output macros can be driven by any internal-level signal. TTL BIDIs and 3-state output macros require the use of 3-state enable-drivers.

- Cell utilization - Do not violate the internal cell utilization limit (95%) without AMCC approval.

- Internal pin count - Do not exceed the array internal pin count limit.

- Additional power and ground - Provide additional power and ground pads as needed by using the ITPWR, ITGND and IEVCC macros on the schematic.

- Simultaneously switching outputs - Use the SWGROUP macro parameter/property to allow the simultaneously switching output ERC check. Use SWGROUP on the output macros and the added power/grounds added to accomodate the group.

- Additional ground - When leaded chip carriers are to be used, care should be taken to supply sufficient ground pins to allow separation of any signals where cross-talk may be of concern, e.g., between input and output signals. Spare pins should be grounded.

- High frequency signals - Signals running at 400MHz and higher require specific placement and extra grounds for isolation. For specific package location and information on the pads to be used for the grounds consult AMCC.

- Overhead Current - Overhead current is based on I/O type and array. See Section 5.

- DC Power - Compute the maximum worst case DC power. Include any ECL static output power. See Section 5.

- AC Power - Compute the AC component of the worst-case power. See Section 5.

- Total Power - Combine the DC power dissipation of the interface macros with the power computed for the internal macros. See Section 5.

- Packaging - Verify that the package selected is appropriate for the operating environment and junction temperature (compute based on power).

- Packaging - Verify that the number of I/O signal pads, including any added power and grounds that cannot use an internal package power-ground plane, is less than or equal to the signal pins available on the package.

- Packaging - Verify that the thermal diode pads and AC speed monitor pads reach external package signal pins.

- Packaging - Verify that the selected heatsink is available for this array and package.

- Critical paths - Complete the description of and clearly identify the critical paths. Use the timing correlation report form.

- ***amccerc.lst, amccio.lst, amccpkg.lst*** and several (renamed) ***amccvrc.lst*** reports must be submitted. Design Submission.

- Complete simulation documentation must be submitted with the design, including source files.

- For guidance in constructing simulation vectors, refer to the AMCC document:
  Vector Submission Rules and Guidelines
  in the Design Manual.

- Placement - Consult with AMCC Applications prior to attempting a pre-placement file. Review restrictions for dual-cell I/O macros, simultaneously switching outputs and packaging-power/ground plane added power and ground macro placement.

- Test vectors - Limit the number of simultaneously switching outputs per vector to 8 for mixed ECL/TTL and 16 for 100% ECL circuits if no parametric vectors are used. Double the limits when parametric vectors are supplied with the design submission. These limits apply to functional and parametric vectors.

POWER BUS DISTRIBUTION AND DECOUPLING

Optimal power bus distribution and decoupling is dependent on a number of interactive device and system variables, including the package design used, the number of simultaneous switching outputs on the device, output loading, the amount of switching noise contributed by other system components, the number of power busses and the design of the system and module power distribution.

AMCC recommends the use of multi-layer PC boards that provide dedicated low impedence power and ground planes. Besides maintaining a constant characteristic impedence for transmission lines, the planes provide for a low impedence return path to the ECL or TTL circuitry and act as an electromagnetic shield for the signal lines. The distributed capacitance will also improve noise margins by minimizing "ground bounce" and crosstalk.

The 2-layer PC boards, on the other hand, may require successive approximations to optimize the system noise margins and reduce external noise from being fed back into the chip through the power and ground pins. This approach should only be attempted in lower performance systems.

The I/O ECL VCC and the Internal VCC package pins should be tied together as close to the chip as possible, using good high frequency practices. When mixed I/O is combined with multiple power busses, the TTL GND and ECL VCC (0V) can be tied directly together at the chip on multilayer boards.

For 2-sided boards, the location will be system dependent and may require some experimentation. The primary considerations are the amount of simultaneous switching, the signal/ground pin ratio and the isolation between the TTL and ECL signal lines (and return paths).

Low frequency power-supply decoupling is generally provided in the range of 0.5 to 2.0 μf/WATT, while high frequency bypassing should be 100 to 1,000 pF/side. The bypass capacitors are generally placed as close to the chip as possible using high frequency techniques to minimize the inductance in the leads, traces, feed-throughs and components.

The AMCC Q20000 performance boards use a 1 μf tantalum capacitor in parallel with a 470 pf ceramic chip capacitor for each of the Internal VEE/VCC pairs. This same combination is used for any VCC or additional VCC package pins with excellent results.

PHASE-LOCKED LOOP

The basic phase-locked loop components are shown in the PLL block diagram in Figure 2-7. The loop consists of a phase detector, which compares the phase difference between the VCO and the reference input, a loop filter, which converts the phase detector output into a smooth DC voltage, and the VCO, which generates a frequency based on its input voltage.

AMCC-provided PLL building blocks differ for frequency synthesis and clock recovery, primarily in the phase detector design. This is due to the differences in reference inputs to the phase detector. In the case of the clock synthesis PLL, the reference input is a very stable crystal-based source.

For clock recovery from a serial data stream the reference input has varying transition density; i.e., different run lengths of 1's and 0's with short term frequency variations.

The loop filter generates a control voltage for the VCO input based on the output of the phase detector. Different sets of loop filter components must be specified for both the clock synthesis and clock recovery applications.

Appropriate filter components may be required for different encoding schemes, acquisition time requirements and system noise environments.

AMCC provides on-chip selected sets of resistors and capacitors appropriate for specific system conditions. One off-chip, pre- specified "clean-up" capacitor is provided by AMCC either inside the cavity or on the heatsink side of the package.

A representative transmitter block diagram is shown in Figure 2-8 and the clock synthesis macro diagram is shown in Figure 2-9. A representative receiver diagram is shown in Figure 2-10. and the clock recovery macro diagram is shown in Figure 2-11. Local Loopback and link loopback block diagram are shown in Figures 2-12 ans 2-13 respectively.

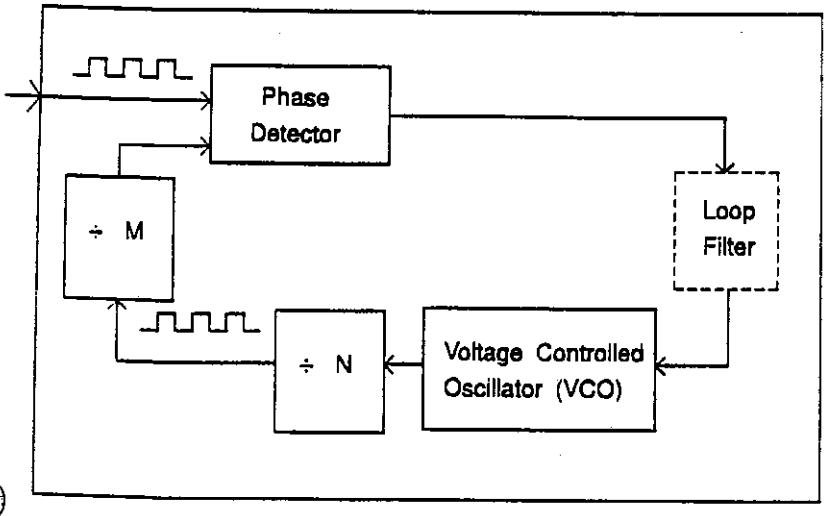

Figure 2-7 Phase-Locked Loop Diagram

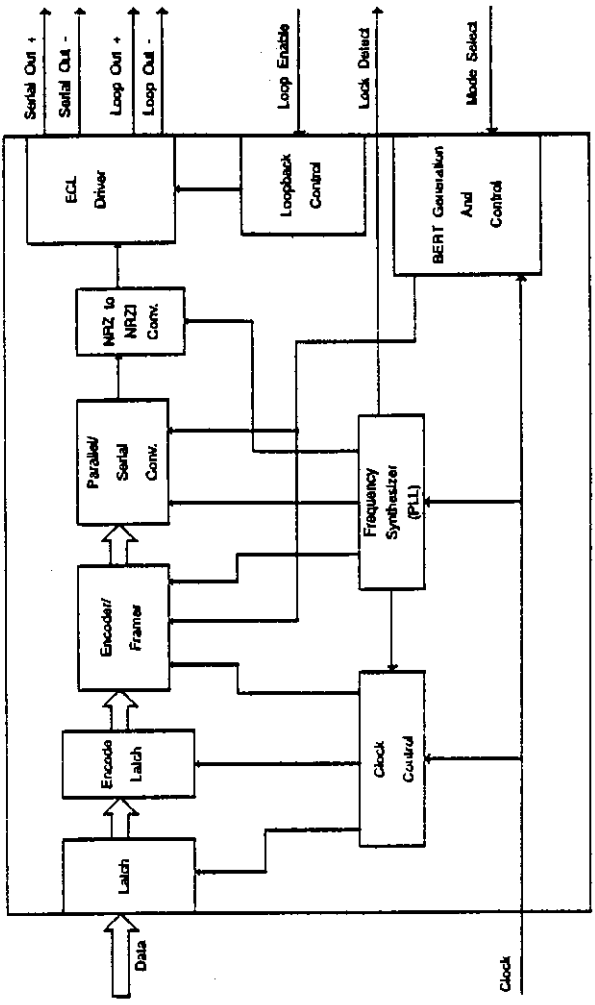

Figure 2-8 Representative Transmitter Block Diagram

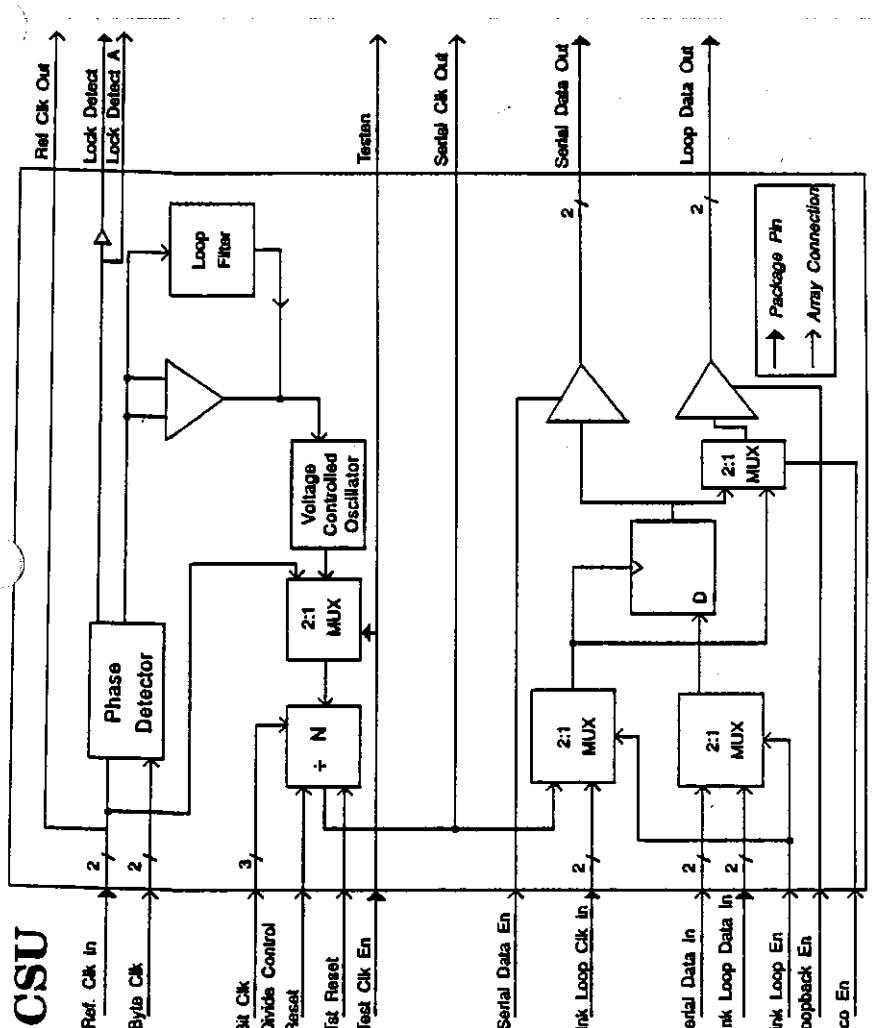

Figure 2-9 Clock Synthesis Macro Diagram

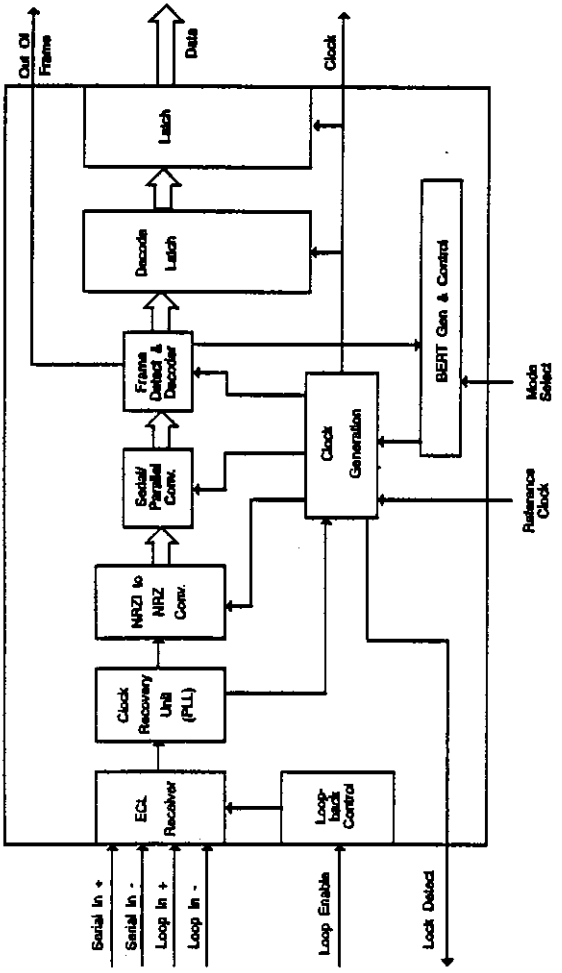

Figure 2-10 Representative Receiver Block Diagram

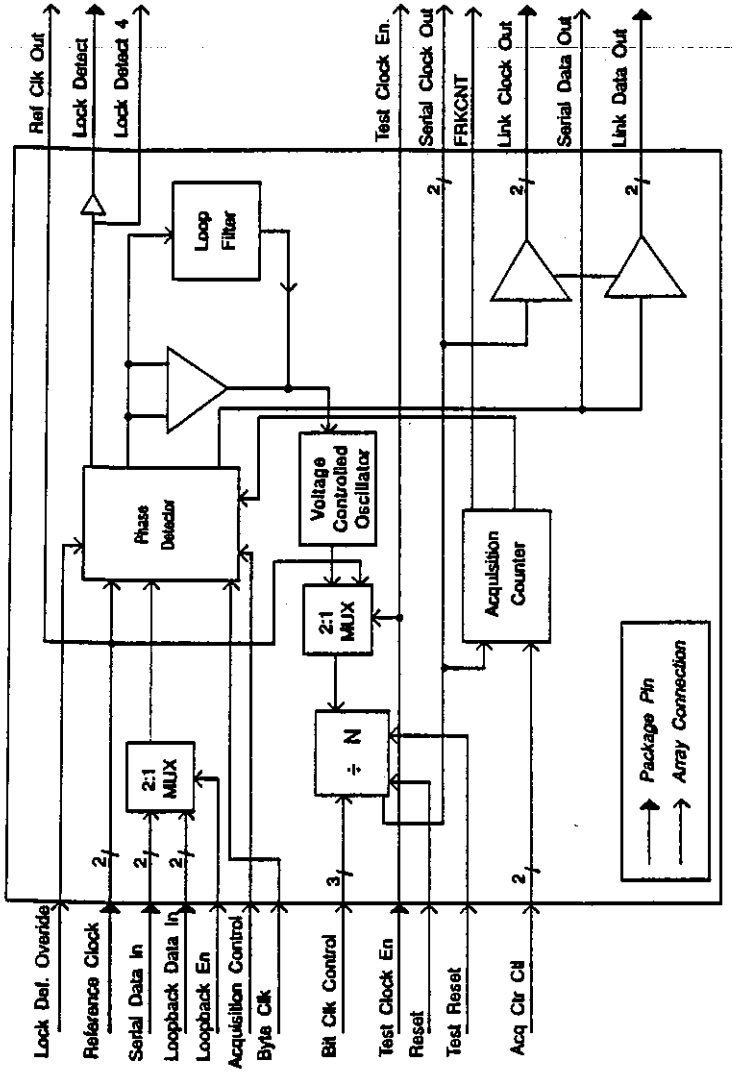

Figure 2-11 Clock Recovery Macro

SPECIAL FEATURES

Bit Error Rate Test (BERT)

As a macro option, transmitter and receiver designs will be capable of performing BER measurement to verify fiber optic link integrity. BER testing can be periodically performed to check for laser diode and/or fiber optic connector degradation. When enabled, the BER test will cause psuedo random data to be sent from the transmitter chip to the receiver chip where it will be checked against an identical psuedo random data generator. The psuedo random data will be generated/checked using an 8 bit linear feedback shift register. The psuedo random data may be encoded and decoded. The bit error count can be read by the subsystem via the receive chip. Consult AMCC regarding this feature.

Loopback Mode

Local Loopback

For datacom or telecom applications, local and link loopback is supported. Local loopback requires both a transmit chip and a receive chip. When enabled, serial encoded data from the transmit chip is sent to the receive chip where the clock is extracted and the data decoded. The parallel data is then sent to the subsystem for verification. This loopback mode provides the capability to perform offline testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium, and allows system diagnostics. Refer to Figure 2-12.

Link Loopback

Link loopback provides a means for link testing. When link loopback mode is enabled, the transmitter accepts serial clock and data from the receiver chip. The serial data is reclocked using the link loopback clock to minimize the data distortion and then transmitted via the serial data output pins. Link loopback can also be used to implement a repeater function, with clock jitter and data distortion determining the number of repeaters allowed. Refer to Figure 2-13.

Test/Bypass Mode

CRU and CSU macros have testability input pins to aid in functional testing or as a PLL clock bypass. *TestClockEnable* places the macro into test mode. An externally generated clock can then be input via the reference clock input.

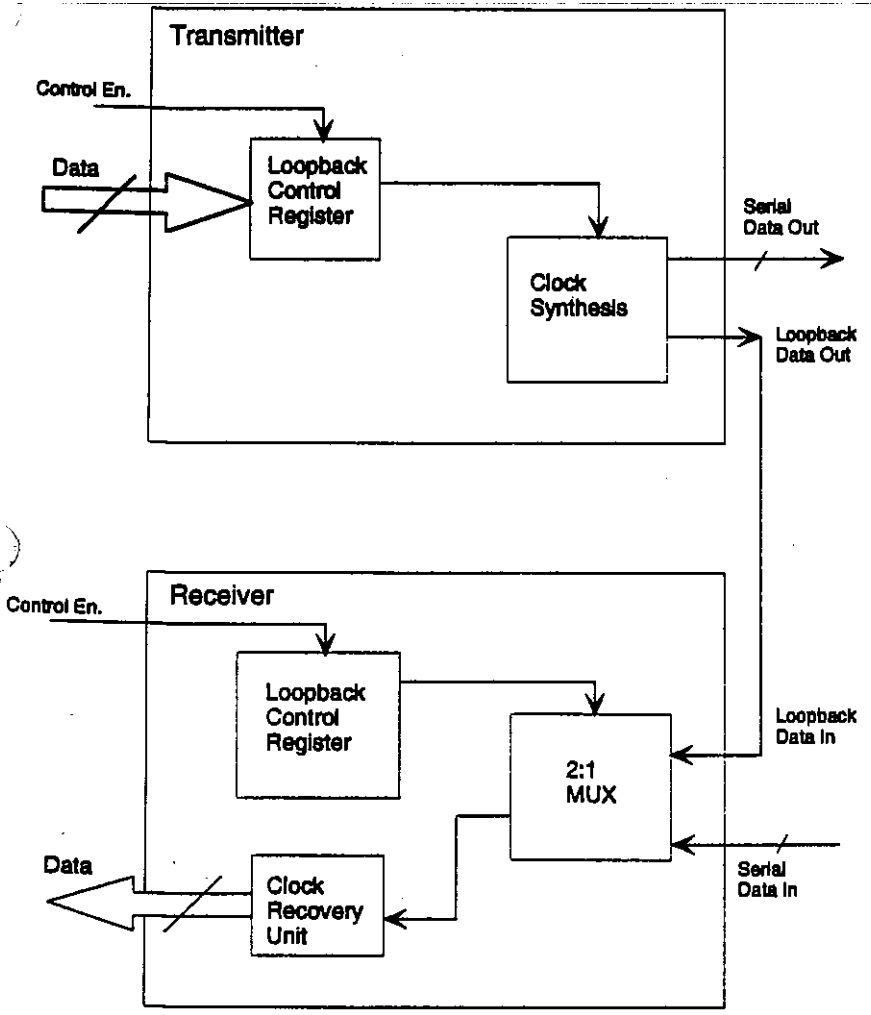

Figure 2-12 Local Loopback Block Diagram

(210)

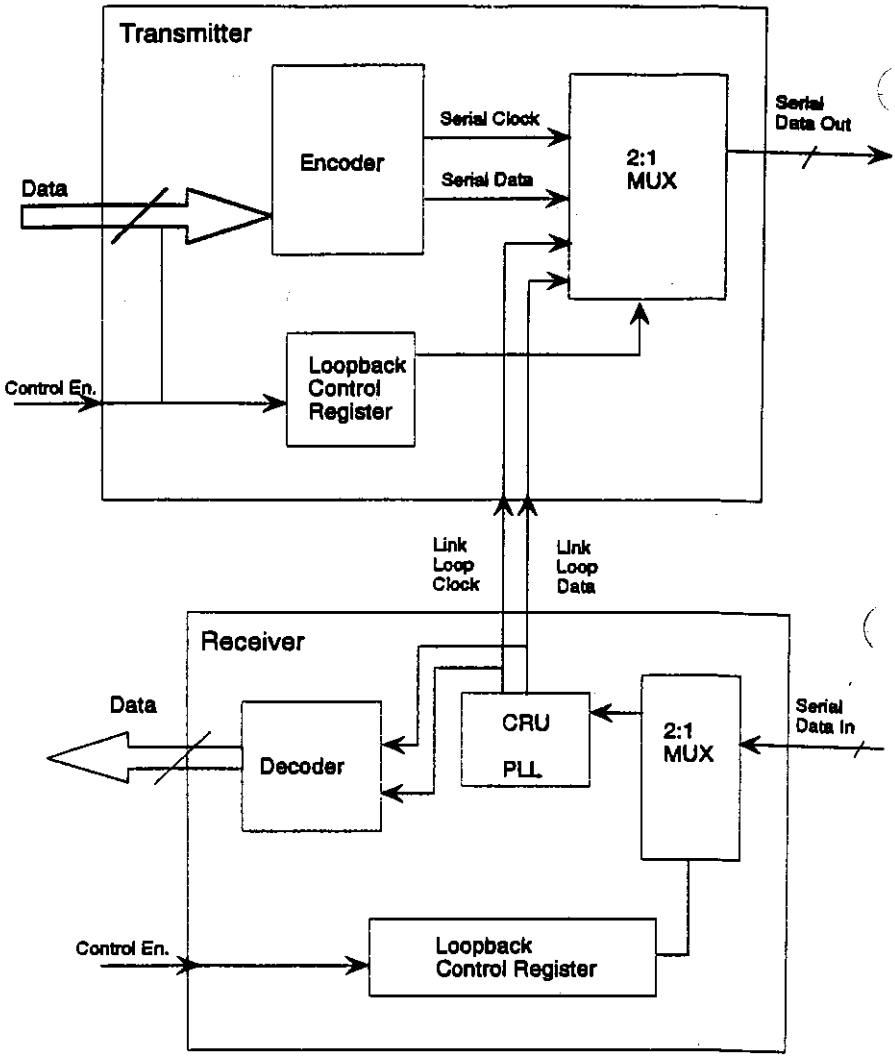

Figure 2-13 Link Loopback Block Diagram

Lock Detect

For CRU macros, lock detect indicates the phase state of the PLL relative to the incoming data stream. Control pins from the core logic area permit lock detect to be indicated after 512, 1024, 2048, or 4096 bit times depending upon loop filter parameters. On CRU macros, if the serial data inputs have an instantaneous phase jump, the CRU will not indicate out-of-lock state, but will recover correct phase alignment within the pre-loaded bit times.

For the CSU macro, lock detect indicates the phase state of the PLL relative to the incoming reference clock.

FREQUENCY SYNTHESIS MACROS

The frequency synthesis PLL will align the phase and frequency of the byte clock and the reference clock The serial clock will be a multiple of the reference/byte clock. A typical frequency multiplication factor is 20, with extension as high as 64. Bit (+M, +N) controls are provided to permit flexible selection of desired operating frequency. Critical parameters for the clock synthesis PLL are jitter and accuracy. AMCC loop filter components are set to optimize the loop for minimum phase jitter and maximum accuracy, with less emphasis on acquisition time. For variations on loop filter parameters contact AMCC.

Specifications

Input Reference Frequency - The input reference frequency can be a selected divide ratio of the synthesized clock frequency. The maximum divide ratio is 64.

Reference Clock Jitter - The reference clock needs to be generated from a stable source such as a crystal oscillator. The allowable rms jitter cannot exceed .04 % of the reference clock pulse width.

Input Reference Stability - The reference clock stability should be less than 100 ppm.

Acquisition Time - The loop acquisition time will depend on the loop filter parameters. (1.0 µs to 250 µs values are typical)

Edge jitter - The output edge jitter will depend on the loop filter parameters. (50 to 100 ps pk-pk values are typical)

Supply Voltage Sensitivity - Power supply noise rejection will be between 40 and 60 dB depending on the noise spectrum.

CLOCK RECOVERY MACROS

The clock recovery PLL will generate a clock which is at the same frequency and 180 degrees out of phase with the serial data input. This generates clock and data outputs from the incoming serial bit steam which feeds the subsequent parallel conversion. An external clock reference is used to reduce initial acquisition time and to provide stability in the absence of serial data. The filter parameters are set to optimize the loop for the anticipated serial data input characteristics. These include: maximum run length and transition density of 1's or 0's, and the jitter associated with the fiber optic link. For variations of loop filter parameters contact AMCC.

TEST VECTORS FOR PLL-BASED ASSP'S

The following vector sets must be submitted as part of initial test transfer for every PLL array based design. Items 1 through 3 are for every PLL array based design, and 1 through 6 are for every PLL array based design that will be a standard product.

1. **Functional vectors** are to be executed in bypass mode (TESTCLKEN high), with clock input through REFCLKP/N.

2. **VCO test**(TESTCLKEN low). The divide ratio should be explicitly defined to produce an output less than 90 MHz, and the signal should be directed to output which can support this data rate. The stop location (i.e., final vector) should leave TESTCLKEN low.

3. **Parametric tests.** A parametric gate tree approach is preferred. If not possible, then the vector set should generate the minimum number of outputs switching.

4. **AC vectors** which exercise all specifications in the datasheet or objective specification. (Tpd's consistent with [K datasheet or objective specification. (Tpds consistent with current AMCC array guidelines, set-up and hold tests as specified). A list of stop locations for every AC test must be provided. Also needed is a list of tSKEW test [x =(tPD test y - tPD test z)]. (This is a common characteristic test for PLL chips that generate a WORDCLK.)

5. IOZH/L vectors with stop locations for bidis and tristates.

6. tENA and tDIS stop locations within the IOZH/L vector set.

Distributed Capacitive Load and High Frequency Loading Effects

by R. W. Spehn

One of the principal challenges facing a digital design engineer at either the device or system level is that of assuring that high speed/high bandwidth signals actually pass through the packaging interface in a usable form. The edge rates achievable with Bipolar and BiCMOS I/O structures combined with VLSI and ULSI packages supporting 200 to 300 pins require transmission line techniques to be considered at the die to package and package to board boundaries. At the same time, TTL clocks and data busses are now pushing into the 50 to 100 MHz range. Using the inherently unsymmetrical TTL outputs at the frequency range that was previously the domain of relatively well behaved ECL only adds to the challenges for the designer.

These challenges are similar to those faced by microwave transmission line designers for more than a decade. Fortunately, the nature of digital signals allows for some simplification of the analysis techniques. After some review of the available literature, I have found some tools that only require moderate algebraic manipulation and your scientific calculator and are sufficient for signals through the 500 MHz regime. For signals of 1 GHz and greater, the digital simplifications (uniform high and low levels, pulse duration greater than 3x the transition time, etc.) no longer apply. Here the full treatment, Smith Charts and all, is needed.

Transmission Line Discontinuities.

Any conductor having a length and effective propagation delay greater than the transition time of the signal it carries should be considered a transmission line. For a 1 nsec transition time and dielectric materials such as FRP, this length is on the order of 15 cm or 5.9 inches. The exact form is:

$$L = \frac{c \times T}{\sqrt{\varepsilon_{eff}}} \qquad (1)$$

Where T is the transition time, L is the length, c is 2.997 x 10**8 m/sec and ε_{eff} is the dielectric permittivity of the surrounding medium.

Transmission lines are usually described in terms of their characteristic impedance, Z_0. This impedance can be described in terms of the distributed inductance and capacitance as:

$$Z_0 = \sqrt{\frac{Ld}{Cd}} \qquad (2)$$

If two transmission lines of differing impedances are joined, a portion of the energy of a signal encountering the discontinuity will be reflected. The ratio of the reflected signal to the incident signal is the reflection coefficient:

$$\rho = \frac{Z_2 - Z_1}{Z_2 + Z_1} \qquad (3)$$

Where Z_1 is the impedance of the incident transmission line, and Z_2 is the impedance of the second line or the load. This expression can be used directly in the time domain if the impedances are not frequency dependent. For frequency dependent impedances caused by lumped inductive or capacitive reactances, a similar expression is used in the complex frequency domain (S):

$$\rho(s) = \frac{Z_2(s) - Z_1(s)}{Z_2(s) + Z_1(s)} \qquad (4)$$

Distributed Loading

A typical analysis problem is that of determining the loading effect of a series of capacitive loads distributed at regular intervals along a transmission line. This configuration is most frequently encountered in the form of a device output driving an address or data line to an array of memory devices.

If the arrangement of the memory devices is reasonably regular, the driven circuit can be approximated as a transmission line with additional distributed capacitance. If the load capacitances are spaced close together relative to the transition time of the signal, the resulting combined structure is again a transmission line but with a new, lower impedance, Z_3 It is in effect a delay line with reduced phase velocity and significant filtering or rise time degradation at the far end.

If we assume that the added capacitance has little effect on the distributed inductance of the line, the new impedance is:

$$Z_s = \sqrt{\frac{Ld}{Cd + CD}} \qquad (5)$$

Where CD is the distributed capacitance of the load. Equations (2) and (5) can be combined and an expression for Zs without the inductance term can be formed as:

$$Z_s = \frac{Z_o}{\sqrt{1 + \frac{CD}{Cd}}} \qquad (6)$$

This new impedance is the one that is seen by the output of the source device. If the package trace was optimized for the assumed unloaded transmission line Zo, equation (3) can be used to analyze the mismatch at that boundary.

The propagation delay of the combined structure can be represented as:

$$tD = td \times \sqrt{1 + \frac{CD}{Cd}} \qquad (7)$$

Where tD is the loaded time delay per unit length and td is the unloaded delay. This equation also suggests an experimental way of evaluating the radical in equation (6) by use of easily measured delay times.

The impedance and capacitance of the unloaded line can be derived either experimentally or analytically. Typical Cd values for representative transmission lines are:

Zo	Cd	w/h
50 Ohms	1.30 pF/cm, 3.3 pF/in	1.50
75 Ohms	0.83 pF/cm, 2.1 pF/in	0.75
100 Ohms	0.61 pF/cm, 1.5 pF/in	0.36

These values have been calculated assuming FR4 material with a relative permittivity, ε, of 5.0. The width to thickness ratio , w/h, has been included for reference. The structure is assumed to approximate a microstrip, i.e. a trace of width w over a ground plane at separation h through the referenced board material.

If the added loads are evenly positioned and their spacing meets the rise time and prop delay criteria described above, this loaded line model is valid. The impedance of the resulting structure, and thus the load it presents to the output, can be predicted. Unfortunately this structure is still only an approximation of a transmission line. The new "line" does not have the uniform TEM (Transverse ElectroMagnetic) propagation that is characteristic of the ideal line. The structure is a delay line and low pass filter with a cutoff frequency that decreases as the load capacitance increases.

The degradation of rise time resulting from this filter occurs even if the driving output is perfectly matched to the resulting "line" impedance. As an example, for a 50 Ohm line, a distributed load of 1.3 pF/cm (effectively doubling the unloaded distributed capacitance) limits the rise time to 1 nsec after 20 cm. By comparison, a distributed load of 10 pF/cm on a 50 Ohm line would result on a rise time of 2.4 neec after 20 cm.

Although a precise analysis of the rise time degradation is complex, It appears that a relationship similar to that for propagation delay can be successfully used for added distributed capacitances up to 10 times the unloaded line capacitance:

$$RT = rt \times \sqrt{1 + \frac{CD}{Cd}} \qquad (8)$$

Here RT is the resulting rise time degradation per unit length of the combined structure and rt is the rise time degradation of the unloaded line. This relationship is only approximate and appears to work best at points located four or more "load stations" down the line from the source.

Lumped Loading

If the spacing between the added capacitances is irregular, but still closer than a rise time propagation delay, the resulting structure will have a varying and difficult to predict impedance. This is definitely not a recommended structure for critical signal transmission.

If the propagation delay spacing of the added loads is greater than the transition times of the signal, the effective impedance of the line reverts to Z_0, the unloaded impedance, during the actual transition. Each point load capacitance is, however, a point of impedance discontinuity, and thus a source of reflection.

Since the load is capacitative, the reflections are negative, and can cause errors in any input that precedes a large discrete load. A survey paper written by P. G. Tumms developed a useful example of a finite rise time signal encountering a discrete capacitive load.

The signal is a simple linear rising edge starting from 0 (logic low level) and reaching a stable level of E (the logic high level) at t_r, the rise time for the signal, and remaining at E after that time. This signal can be expressed as:

$$e^+(t) = (E/t_r)t\ u(t) - (E/t_r)(t - t_r)\ u(t - t_r) \qquad (9)$$

The expression is the difference of two ramp functions, one starting at time 0 and the other starting at time t_r.

The reflected pulse in terms of r from equation (3) is:

$$e^-(t) = e^+(t)\ \rho \qquad (10)$$

Since the discrete load is capacitive reactance, the complex frequency for ρ in equation (4) should be used. The $Z_1(s)$ is the transmission line impedance Z_0. The load impedance $Z_2(s)$ is the parallel of the discrete load capacitive reactance, $1/Cs$, and the rest of the transmission line, Z_0.

After appropriate algebraic manipulations, the complex reflectance is:

$$\rho(s) = \frac{-s}{s + 2/(Z_0 C)} \qquad (11)$$

and the input signal transforms to :

$$E^{+}(s) = \frac{E}{t_r s^2}(1 - e^{-t_r s}) \qquad (12)$$

If these two expressions are inserted in equation (10), simplified, and inverse transformed back to the time domain, the reflected pulse is:

$$e^{-}(t) = (E/a\, t_r)\,[-(1 - e^{-at})\, u(t) + (1 - e^{-a(t - t_r)})\, u(t - t_r)] \qquad (13)$$

where (a) is defined as 2/(Zo C).

According to Tumms, the maximum amplitude of this reflected signal occurs at $t = t_r$ and is:

$$|e^{-}(t)|_{max} = (E/a\, t_r)(1 - e^{-at_r}) \qquad (14)$$

and for many applications, $at_r \geq 2.3$, implying that the rise time of the input signal is greater than or equal to the ZoC time constant of the line impedance and load capacitance. Under this condition, equation (14) may be approximated as:

$$|e^{-}(t)|_{max} = (E/at_r) \qquad (15)$$

The duration of the reflected signal (between half amplitude points) can be derived from equation (13) as:

$$W = (1/a) \ln \frac{e^{at_r} - e^{-at_r}}{1 - e^{-at_r}} \qquad (16)$$

and for the condition $at_r \geq 2.3$, this reduces to:

$$W = t_r \qquad (17)$$

This maximum amplitude and half-amplitude pulse width character-ization is very useful in determining the signal energy available to force a logic input to the opposite state or to constructively or destructively interfere with a periodically repeating signal at the output.

Note that if the rise time to time constant condition is met, the reflected signal maximum is less than 40% of the original step amplitude. For values of at_r near 1.5, the reflected signal reaches the half logic swing value at its maximum. At the extreme, at_r values near 0.1, implying ZoC time constants 20 time the rise time, the reflected signal reaches 95% of the logic swing.

The effect of such a large pulse on the originating output would be the equivalent of a switching contention. If the output was in the TTL high state, the reflected low pulse would appear as a short to logic low through impedance Zo for a duration of W.

Tumms continues the analysis to develop the transmitted signal to additional loads and inputs further down the line. The transmitted signal is the sum of the incident and reflected signals. The form is:

$$e(t)T = e^{+}(t) + e^{-}(t) \tag{18}$$

The resulting time domain expression, in spite of its complexity, can be seen to be the linear combination of equations (9) and (13) :

$$e(t)T = (E/a\ t_r)\ \{\ [at + (e^{-at} - 1)\ ]\ u(t) + [-1 + a(t - t_r)\ e^{-a(t - t_r)}]\ u(t - t_r)\} \tag{19}$$

which indicates for $0 < t < t_r$:

$$e(t)T = (E/a\ t_r)\ [at + (e^{-at} - 1)\ ] \tag{20}$$

and for $t > t_r$:

$$e(t)T = (E/a\ t_r)\ [at_r + e^{-at}\ (1 - e^{+at_r})\ ] \tag{21}$$

These equations can be used to develop simpler expressions for the rise time and delay of the transmitted signal. In the extreme case of the time constant much larger than the rise time, the input signal approaches a step function and the added delay to the half logic swing level would be:

$$\Delta t = 0.693 / a \tag{22}$$

and the rise time from 10 % to 90% logic swing of the transmitted signal would be:

$$tR = 2.2 / a \tag{23}$$

In actual practice the input rise times can be comparable to or greater than he load time constant. If the input signal rise time is more than four times the load time constant, equation (20) gives:

$$t_{ro}/2 = t_r/2 + 1/a \quad (24)$$

where $t_{ro}/2$ is the time required for the output signal to reach half swing. The delay due to the discrete load is thus:

$$\Delta t = t_{ro}/2 - t_r/2 \quad (25a)$$

or $$\Delta t = 1/a \quad (25b)$$

Although equation (19) indicates that the output wave form is actually a summation of exponentials, the simplifications of digital logic can come to our rescue. If we approximate the output as a ramp which has the same half amplitude rise time as the pulse described by equation (19), the rise time of the proposed output ramp function would be:

$$t_{ro} = 2(t_{ro}/2) \quad (26a)$$

or $$t_{ro} = t_r + (2/a) \quad (26b)$$

We now have a simple tool that can approximate the delay and rise time degradation effects of the successive discrete loads in terms of the arriving signal rise time and the ZoC time constant of the load.

Note that this technique can be used in the package to circuit board interface to account for transitional parasitics of the package pin.

As an example of the use of this distributive load equivalent impedance technique, we will examine a design problem of specifying, matching, and terminating a TTL output. The TTL signal is driving the address line of an array of memory devices.

The specified input capacitance of the memories is 10 pF and they are distributed at 2 inch intervals on the circuit board. The ASIC macro library specifies the capacitive drive capability of the TTL output macro as a function of frequency.

For typical circuit board material and line widths the 2 inch (5 cm) spacing represents a time delay of 300 to 400 psec. Since this is significantly less than the rise/fall times of a TTL output, the reduced impedance delay line model is the appropriate one to use.

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Section 3
Timing Analysis

Timing Analysis

There are two types of timing analysis: path propagation delay and set-up and hold time analysis. Path propagation delay is covered in this section. External set-up and hold time is covered in Section 4. It is critical that timing analysis with tracking be fully comprehended for each design.

COMPUTING PROPAGATION DELAY

The macros selected, the options of those macros, the loading on the macros, and the final layout of the circuit are all factors in the propagation delay of any path. The loading may be the interconnect capacitance or the external load capacitance due to system loading and package pin capacitance.

There are two approaches that can be used to compute propagation delay: Front-Annotation, where a statistical estimate (averaged value) of metal delays based on net sizes is used; and Back-Annotation, where the actual metal delay is used in the computation.

• Preliminary Computation - Prior to Capture

Path delays are composed of the intrinsic (internal to the macro) delays specified for the macros, the path propagation delays for the macro interconnect (macro-to-macro routing) and the output macro capacitive load.

The path propagation delays can be estimated using the statistical wire delay tables (L_{net}), fan-out loading (L_{fo}) and the appropriate k-factors (k) for the macros chosen. The equation for the extrinsic (load) delay for a single internal net is shown below and discussed in detail on the following pages.

$$t_{ex_{int}} = k_{fo} * L_{fo} + k_{net} * L_{net}$$

The equation for the extrinsic (load) delay for a single output net is shown below and discussed in detail on the following pages.

$$t_{ex_{out}} = k * (C_{system} + C_{package})$$

The sum of all intrinsic macro delays in the path:

(Tpd in the macro documentation)

and all extrinsic loading (t_{ex}) is the path delay.

• **Front-Annotation - After Capture**

After schematic capture, Front-Annotation software is available to provide the designer with a file of rising and falling edge delays per net (expressed as NOM, MIN and MAX) for specific operating conditions. By incorporating this file into the simulation database, the designer can obtain a statistical estimate of circuit performance.

Front-Annotation uses a metal load delay computed as the average of metal delays that might be expected for the specific net size on a specific array. Front-Annotation uses the actual electrical load delay. Front-Annotation cannot be guaranteed.

• **Back-Annotation - After Layout**

The most accurate method of computing a circuit propagation delay requires that the circuit be completed through layout. Back-Annotation software adds the actual metal delay and fan-out delays into the path for internal nets and the actual capacitive load delay for output nets. Back-Annotation must be run and accepted as final prior to the generation of the actual arrays. The Back-Annotation program provides a file which includes the actual metal and package pin delays in a net along with the actual electrical load delays.

AMCC guarantees that the silicon will meet (will not be slower than) the results of the maximum worst-case Back-Annotation.

INDIVIDUAL MACRO PROPAGATION DELAYS

AMCC macro documentation specifies unloaded macro path propagation delays (Tpd) for each path through a macro for two operating conditions: COMMERCIAL and MILITARY with either a +5V or -5.2V ECL power supply (COM5 and MIL5). Each specification provides a MIN/MAX range for the operating condition. Adjustment factors are provided to convert COM5 timing specifications to COM4 (-4.5V ECL supply) or MIL5 to MIL4 (see Table 3-1).

TABLE 3-1
MACRO SPECIFICATIONS PROVIDED IN THE DESIGN MANUAL

Supplied		Compute	
COM5MAXmax	COM5MINmin	COM4MINmin	COM4MAXmax
MIL5MAXmax	MIL5MINmin	MIL4MINmin	MIL4MAXmax

Some macro specifications include a different delay for a rising edge (Tpd-+) than for a falling edge (Tpd+-). Three-state macros have specifications for high-Z switching delays TPHZ, TPZH, TPZL and TPLZ.

The AMCC macro specifications have been expanded to show the model behavior in more detail. The specifications are interpreted as follows (see Figure 3-1):

Non-inverting:

Tpd++ rising edge input; rising edge output
Tpd-- falling edge input; falling edge output

Inverting:

Tpd+- rising edge input; falling edge output
Tpd-+ falling edge input; rising edge output

All AMCC EWS simulation models are accurate to within 5 ps (three decimal place accuracy when measured in ns).

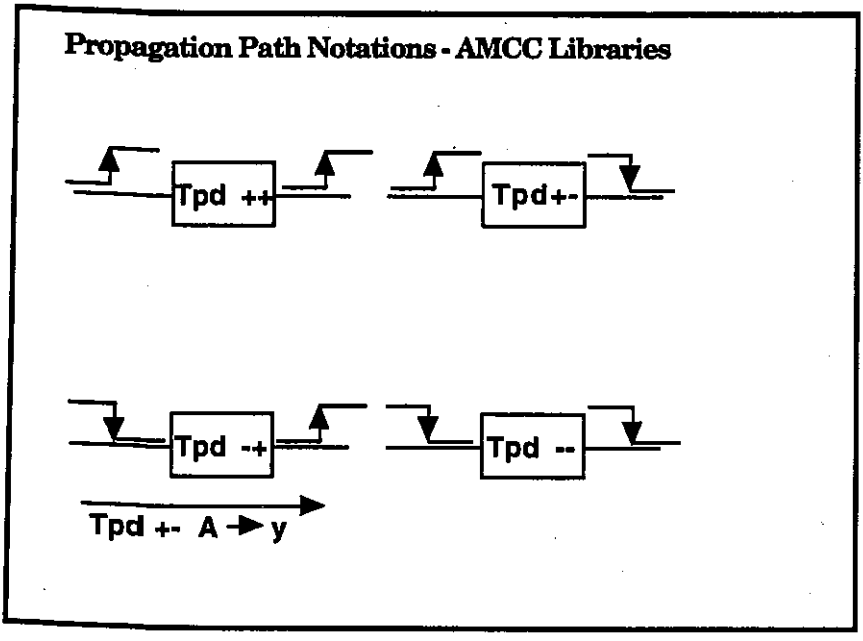


Figure 3-1 T_{pd} Specification Conventions

INTRINSIC SET-UP AND HOLD TIMES

The intrinsic set-up and hold times for the latches, flip/flops and MSI macros that include one or more of these types of devices, are specified in the macro summary in Section 6. The parameters represent the behavior of the macro as observed at its input and output nodes.

Set-up time (Tsu) is the time that a data signal must be stable prior to the active clock edge.

Hold time (Th) is the time that a data signal must be held after the active clock edge. Set-up and hold times are not specified with a range. Use the same number for MAX and MIN analysis.

Set-up and hold times are specified as worst-case values within the operating conditions of the library [e.g., xxxxMAXmax, xxxxMINmax]. Refer to Section 4 for a discussion on external set-up and hold time.

RECOVERY TIME

Recovery time (Trec) is specified for any latch or flop/flop which has a set or reset. It is the length of time that a reset/set signal has to have been inactive prior to an active clock edge. Clocking within the recovery time period will result in unpredictable behavior.

Recovery time is specified as a worst-case value within the operating conditions of the library.

PULSE WIDTH

Minimum pulse width is the length of time that a signal must remain stable in order to be recognized by the macro. Flip/flop and latch documentation in Section 6 includes pulse width specifications. Pulse width is computed based on a 40% duty cycle. Minimum pulse width (PW) is specified for all macros in the Maximum Frequency and Minimum Pulse Width table.

AMCC libraries check for pulse width violations within a given simulation for flip/flops, latches, input and output macros only. Manual checks must be performed for all other macros. Pulse width distortion with tracking must be performed on all clock or high-speed data paths. Insuffcient margin may delay the design. Normal EWS simulators will not account for tracking. Therefore, it is recommended that true min/max simulations or timing verifiers be used.

Pulse width violation will cause error messages during simulation if timing checks are enabled. Pulse width checking only confirms that a given operating condition min or max simulation is or is not correct. No simulation for min/max across the libraries is performed (e.g., no simulation is performed using COM5MAXmax and COM5MINmin). A MAXmax-MINmin computation and comparison should not be required.

The MINmin and MAXmax specifications account for all voltage, temperature and process variations that can occur over the entire range of Commercial or Military operating conditions.

Minimum pulse width is specified as a worst-case value within the operating conditions of the library.

Note: For macros other than flip/flops, latches and the interface macros, there are no timing errors generated by the timing analysis programs when a Q20000 macro is driven faster than its specified toggle frequency or when its minimum pulse width specification is violated. The most common violation is the use of L-option macros in paths that are operating above L-option speeds.

MAXIMUM OPERATING FREQUENCY

The maximum operating frequency (fmax) is specified as the maximum I/O switching rate for an I/O macro or the maximum internal toggle rate for an internal macro. A signal may not exceed the maximum frequency specified for the macro.

The actual speed at which a circuit may operate must be computed from a worst-case maximum critical-path timing analysis and must include intrinsic macro delays (specified as "Tpd" in the documentation) and the extrinsic loading delays as computed using Front-Annotation (estimate) or Back-Annotation (specification).

For I/O macros, the toggle frequency should be documented via the AMCCANN user interface. AMCCANN produces AMCCPKG.LST. Document TTL running faster than 50MHz and all ECL over 400 MHz.

TABLE 3-2
MAXIMUM OPERATING FREQUENCY
PULSE WIDTH GUIDELINES

	OPTION	fmax in MHz	PW in ns	Comments
TTL INPUT	L	30	14.0	
	S	60	7.0	
	H	100	4.2	
TTL OUTPUT	L	20	20.0	
	S	45	9.0	
	H	90	4.5	
ECL INPUT *	S	600	0.65	single ended
	H	800	0.50	differential
	D ***	1.2 GHz	0.38	differential
ECL OUTPUT *	S	350	1.15	single ended
- standard	S	800	0.50	differential
- on-chip series				
termination:	S	250		
- Darlington *	S	600	0.65	
- CML: **	S	1.2 GHz	0.35	differential
INTERNAL	L	600	0.65	all single ended
	S	800	0.50	internal macros,
	H	1.2 GHz	0.35	including
	D	1.2 GHz	0.35	flip/flops
	L	350	1.15	complementary
	S	650	0.62	macros - all
	H	900	0.45	except flip/flops
	D	900	0.45	

* Maximum frequency may be limited by specific package selection.
** 50 ohm termination; 200mV peak to peak swing qualified by package type.
*** 1.2GHz ECL inputs require a 45-55% duty cycle.

Note: These are guidelines - not the specifications. Refer to the macro documentation for the frequency specified for a specific macro.

COMPUTING LOADING DELAY - OUTPUT NET - FRONT-ANNOTATION

ECL and TTL output macros are specified with no capacitive loading on the macros. The method for manual computation of the effect of load units on the propagation path is:

For each output net:

$$t_{ex_{out}} = k_{cap} * (C_{system} + C_{package})$$

where

k_{cap} = the k-factor for output macro as listed in Section 6.
C_{system} = the system capacitive load as seen by the pin
$C_{package}$ = the package pin capacitance for that pin

Section 6 macro documentation and the examples in Table 3-3 show a min/max range for k_{cap} values.

The AMCCANN user interface on the workstation allows the specification of the package, the package pin capacitance and the system load. Both package pin and system load capacitances may be specified as default values (all pins identical) or on an individual pin or group of pins basis. The output loading delay is automatically computed and added to the annotation files. All simulations are performed with annotation delay files.

For TTL or ECL output loads over 100 pf consult AMCC.

TABLE 3-3
EXAMPLE K-FACTORS - COM5MAX LIBRARY
kfo = knet; kcap**

Macro Type	Description	min/max	units
ECL input, Bidi and	rising	2.3/5.1	ps/LU
internal macros - L option	falling	3.9/8.5	ps/LU
ECL input, Bidi and	rising	1.8/3.9	ps/LU
internal macros - S option	falling	3.0/6.5	ps/LU
ECL input, Bidi and	rising	1.4/3.1	ps/LU
internal macros - H option	falling	2.4/5.2	ps/LU
ECL input, Bidi and	rising	1.1/2.3	ps/LU
internal macros - drivers	falling	1.5/3.3	ps/LU
ECL output - 50 ohm	rising	16.0/36.0	ps/pF
standard	falling	20.0/44.0	ps/pF
ECL output - 25 ohm	rising	13.0/30.0	ps/pF
Darlington	falling	15.0/34.0	ps/pF
ECL output - 50 ohm	rising	13.0/30.0	ps/pF
Darlington	falling	21.0/46.0	ps/pF
TTL input and Bidi (Non-	rising	3.0/6.5	ps/LU
-Turbo) S, L, H options	falling	6.0/13.0	ps/LU
TTL input and Bidi (Turbo)	rising	1.4/3.1	ps/LU
S, L, H options	falling	2.4/5.2	ps/LU
TTL output - 20 mA	rising	33.0/72.0	ps/pF
	falling	33.0/72.0	ps/pF
TTL output - 8 mA	rising	33.0/72.0	ps/pF
	falling	54.0/117.0	ps/pF

** Individual macro k-factors are specified in the macro library documentation in the Design Manual, Volume I, Section 6.

COMPUTING LOADING DELAY - INTERNAL NET - FRONT-ANNOTATION

The method for manual computation of the effect of load units on the propagation path is:

For each internal net:

$$t_{ex_{Int}} = k_{fo} * L_{fo} + k_{net} * L_{net} = k * (L_{fo} + L_{net})$$

where kfo = k_{net} = the k-factor for the series and the macro option as listed in Section 6. An overview of k-factors is listed in Table 3-3. Refer to Section 6 for the actual k-factors of the macro in use. kfo is for fan-out load; knet is for metal load. Be consistent in the selection of max or min k-factors and max or min Tpd delays.

L_{fo} = the sum of the electrical fan-out loads in a net. (Pins with a fan-in of 2 count as 2 electrical loads)

L_{net} = the estimated metal delay from Table 3-4, indexed by the sum of the number of pins driven (i.e., index by [net size - 1]) (Pins with a fan-in of 2 count as 1 physical load)

- **Computing L_{net}**

Compute the statistical metal estimate load L_{net} by counting the physical pins in the net (driving or source pins and destination pins), subtracting one (1), and using this number as the index to the following table. The number listed under a specific array is the estimate for the load units due to metal in the net. It is independent of the operating conditions (adjustments are carried in the specific k-factors).

- **Computing L_{fo}**

Compute L_{fo} by adding the sum of the electrical load of all loads driven. If a destination pin has a fan-in of 2, it counts as two electrical loads and as one physical pin. A destination may appear to have two physical loads internal to the macro. In these cases, the macro documentation will clearly identify the fan-in load represented by that pin. Physical fan-out internal to the macro does not affect the physical pin count.

TABLE 3-4
FRONT-ANNOTATION ESTIMATED METAL LOADS
Lnet

PINS DRIVEN	Q20120	Q20080	Q20045	Q20025	Q20010
1	12.00	11.00	9.00	7.50	6.00
2	19.49	18.12	15.14	13.06	10.82
3	25.89	24.26	20.52	18.06	15.27
4	31.67	29.85	25.46	22.74	19.49
5	37.02	35.05	30.09	27.18	23.57
6	42.06	39.96	34.50	31.45	27.52
7	46.85	44.65	38.73	35.57	31.37
8	51.45	49.16	42.81	39.59	35.14
9	55.87	53.51	46.77	43.50	38.84
10	60.14	57.73	50.61	47.32	42.48
11	64.29	61.83	54.36	51.07	46.06
12	68.33	65.83	58.03	54.75	49.60
13	72.27	69.73	61.62	58.37	53.09
14	76.12	73.55	65.14	61.94	56.54
15	79.88	77.30	68.60	65.45	59.96
16	83.57	80.98	72.00	68.92	63.34
17	87.20	84.59	75.35	72.35	66.69
18	90.76	88.14	78.65	75.73	70.01
19	94.26	91.64	81.90	79.08	73.30
20	97.70	95.09	85.12	82.39	76.56
21	101.10	98.49	88.29	85.67	79.81
22	104.44	101.84	91.42	88.92	83.03
23	107.74	105.16	94.52	92.14	86.22
24	111.00	108.43	97.59	95.33	89.40
25	114.22	111.66	100.62	98.49	92.56
26	117.40	114.86	103.63	101.63	95.69
27	120.54	118.03	106.60	104.75	98.81
28	123.65	121.16	109.55	107.84	101.91
29	126.72	124.26	112.47	110.91	105.00
30	129.77	127.33	115.37	113.96	108.07
31	132.78	130.37	118.24	116.99	111.12
32	135.76	133.38	121.09	120.00	114.16
33	138.72	136.37	123.92	122.99	117.19

Where pins driven = the internal net physical pin count minus 1. For the Q20000, netsize - 1 = number of macro pins driven. Electrical fan-out loading is taken care of in the Lfo term.

TABLE 3-4 *CONTINUED*
FRONT-ANNOTATION ESTIMATED METAL LOADS
Lnet

PINS DRIVEN	Q20P025	Q20P010
1	7.50	6.00
2	13.06	10.82
3	18.06	15.27
4	22.74	19.49
5	27.18	23.57
6	31.45	27.52
7	35.57	31.37
8	39.59	35.14
9	43.50	38.84
10	47.32	42.48
11	51.07	46.06
12	54.75	49.60
13	58.37	53.09
14	61.94	56.54
15	65.45	59.96
16	68.92	63.34
17	72.35	66.69
18	75.73	70.01
19	79.08	73.30
20	82.39	76.56
21	85.67	79.81
22	88.92	83.03
23	92.14	86.22
24	95.33	89.40
25	98.49	92.56
26	101.63	95.69
27	104.75	98.81
28	107.84	101.91
29	110.91	105.00
30	113.96	108.07
31	116.99	111.12
32	120.00	114.16
33	122.99	117.19

- **Result**

Find the total intrinsic (Tpd-internal) and extrinsic (tex-internal) delays for the macros in the path. Sum the results to find the total path propagation delay for the selected operating condition.

$$t_{path} = (Tpd_{sum} + tex_{sum})$$

where

Tpd_{sum} = sum of all macro Tpd delays

tex_{sum} = sum of all extrinsic net delays for nets driven by macros

Refer to Section 4 for external set-up and hold time analysis equations.

MACRO SPECIFICATION - MAX/MIN
COMPUTING COM5MINmax FROM COM5MINmin, ETC.

- **The Adjustment Factors**

The macro specifications for Tpd and k-factors in the COM5 portion of Section 6 show COM5MAXmax and COM5MINmin for the COM5 libraries. To find COM5MAXmin, multiply COM5MAXmax by the number shown in Table 3-5A. To find COM5MINmax, multiply COM5MINmin by the number shown in Table 3-5A. The numbers vary with the macro outputs. Use the same methods for the MIL5, COM4 and MIL4 libraries.

- **Converting COM5 to COM4; Converting MIL5 to MIL4**

To convert the timing and k-factor specifications supplied in Section 6 from COM5 to COM4 or from MIL5 to MIL4, use the adjustment factors in Table 3-5b.

For a path delay under MIL4 or COM4 operating conditions:

$$t_{path} = \frac{(Tpd_{sum} + tex_{sum})}{adjustment\ factor}$$

Note that ALL data is represented in the workstation libraries.

TABLE 3-5A
TIMING ADJUSTMENT FACTORS
MAXmin, MINmax from MAXmax, MINmin
INTRINSIC DELAYS ONLY

COMMERCIAL		
For Single-Ended Macros		
COMnMAXmin	=	0.76 * COMnMAXmax
COMnMINmax	=	1.24 * COMnMINmin
For Complementary Output Macros		
COMnMAXmin	=	0.70 * COMnMAXmax
COMnMINmax	=	1.30 * COMnMINmin
MILITARY		
For Single-Ended Macros		
MILnMAXmin	=	0.64 * MILnMAXmax
MILnMINmax	=	1.36 * MILnMINmin
For Complementary Output Macros		
MILnMAXmin	=	0.54 * MILnMAXmax
MILnMINmax	=	1.46 * MILnMINmin

n = 5 or 4

TIMING ADJUSTMENT FACTORS
MAXmin, MINmax from MAXmax, MINmin
EXTRINSIC DELAYS ONLY

xxxnMAXmin	=	0.76 * xxxnMAXmax
xxxnMINmax	=	1.24 * xxxnMINmin

xxx = MIL or COM n = 4 or 5

TABLE 3-5B
TIMING ADJUSTMENT FACTORS
COM4, MIL4 FROM COM5, MIL5
INTRINSIC AND EXTRINSIC DELAYS

COM4MINmin	=	COM5MINmin	*	1.05
COM4MAXmax	=	COM5MAXmax	*	1.03
MIL4MINmin	=	MIL5MINmin	*	1.09
MIL4MAXmax	=	MIL5MAXmax	*	1.00

- **Using the Libraries**

Simulations are performed using the maximum and minimum extremes for a given set of operating conditions. Select the library, then select the min or max data within the library.

TABLE 3-6
LIBRARY SELECTION

	POWER SUPPLY	PRODUCT GRADE	EXTREME	LIBRARY NAME	DATA RANGE
COMMERCIAL	+5V	COM	MAX	COM5MAX	min/max
	-5.2V	COM	MAX	COM5MAX	min/max
COMMERCIAL	-4.5V	COM	MAX	COM4MAX	min/max
COMMERCIAL	+5V	COM	MIN	COM5MIN	min/max
	-5.2V	COM	MIN	COM5MIN	min/max
COMMERCIAL	-4.5V	COM	MIN	COM4MIN	min/max
MILITARY	+5V	MIL	MAX	MIL5MAX	min/max
	-5.2V	MIL	MAX	MIL5MAX	min/max
MILITARY	-4.5V	MIL	MAX	MIL4MAX	min/max
MILITARY	+5V	MIL	MIN	MIL5MIN	min/max
	-5.2V	MIL	MIN	MIL5MIN	min/max
MILITARY	-4.5V	MIL	MIN	MIL4MIN	min/max

Example: When a COM5 (Commercial with a +5V or -5.2V supply) analysis is to be performed, use the COM5MAX library and the max data within the library for the maximum worst-case and use the COM5MIN library and the min data within the library for the minimum worst-case. Note that the COM5MAX library does have min data and the COM5MIN library has max data. Simulations can be run using these selections if desired but those simulations are not part of design submission.

Design Submission Extremes

Design submission requires simulation at two extremes for the given operating conditions. Choose one pair:

- COM5MINmin and COM5MAXmax
- COM4MINmin and COM4MAXmax
- MIL5MINmin and MIL5MAXmax
- MIL4MINmin and MIL4MAXmax

AMCCANN File Names

Both the internal net delays and the output net delays are computed by AMCCANN and files generated for use with the simulation software. AMCCANN is described in Volume III.

TABLE 3-7
AMCCANN DELAY FILE NAMES

MINIMUM	MAXIMUM	PRODUCT GRADE	POWER SUPPLY
FNTC4MN.ews	FNTC4MX.ews	COMMERCIAL	-4.5V
FNTC5MN.ews	FNTC5MX.ews	COMMERCIAL	-5.2V or +5V
FNTM4MN.ews	FNTM4MX.ews	MILITARY	-4.5V
FNTM5MN.ews	FNTM5MX.ews	MILITARY	-5.2V or +5V
BCKC4MN.ews	BCKC4MX.ews	COMMERCIAL	-4.5V
BCKC5MN.ews	BCKC5MX.ews	COMMERCIAL	-5.2V or +5V
BCKM4MN.ews	BCKM4MX.ews	MILITARY	-4.5V
BCKM5MN.ews	BCKM5MX.ews	MILITARY	-5.2V or +5V

ews = (dsy, men, val, tim, lsr, lsr-rc, ver)
where

dsy	=	Dazix
val	=	Valid
tim	=	Valid Timing Verifier (when available)
lsr	=	LASAR 6
lsr-rc	=	LASAR 6 (RC tree) (Back-Annotation only)
ver	=	Verilog

ASYMMETRY IN THE WORST-CASE PATH

Each potentially critical path must be evaluated for worst-case conditions. Both the propagation delay of a rising edge input signal and that of a falling edge input signal must be computed and compared for pulse stretch and pulse shrink. The worst potential circuit behavior represented by the macro specifications must be reviewed.

Minimum pulse-width requirements must be verified and the minimum path delay adjusted as necessary to meet these requirements.

In some cases the minimum delay may be the worst case.

AMCC design submission requirements include the simulation of the circuit for both the maximum worst-case and the minimum worst-case for the operating conditions chosen for functional, at-speed, AC test and parametric simulations.

It is up to the designer to provide simulation vectors that will exercise the correct worst-case conditions for the macros in the critical path.

If there is a difference in the functional, parametric or AC test simulation results between the maximum and the minimum worst-case timing, hazard and race conditions are indicated and must be evaluated.

Internal Signal Tracking Guideline

Many factors affect the signal delay tracking within the array. These factors include such things as relative position within the device, process variations, power supply variations, operating temperature and the characteristics of the various macros. The following may be used as a guideline when signal tracking is being estimated.

For all structures, for any edge, and with a random placement, the tracking will depend on the product grade (MIL or COM) and the macro outputs (single-ended or complementary) as shown in Figure 3-2a and Figure 3-2b.

Delta for single-ended macro in MIL5 library is ±18%

Tpd TRACKING FOR MILITARY LIBRARIES

Delta for complementary-output macro in MIL5 library is ±23%

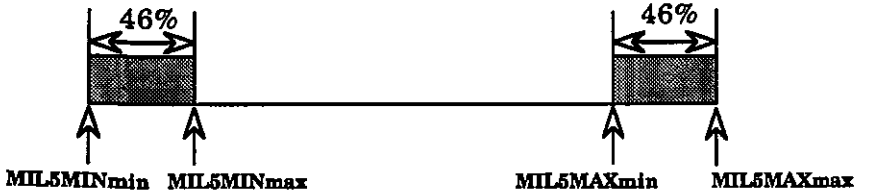


Figure 3-2a Example Of Tracking For Mil5 Operating Conditions - Intrinsic Delays Only

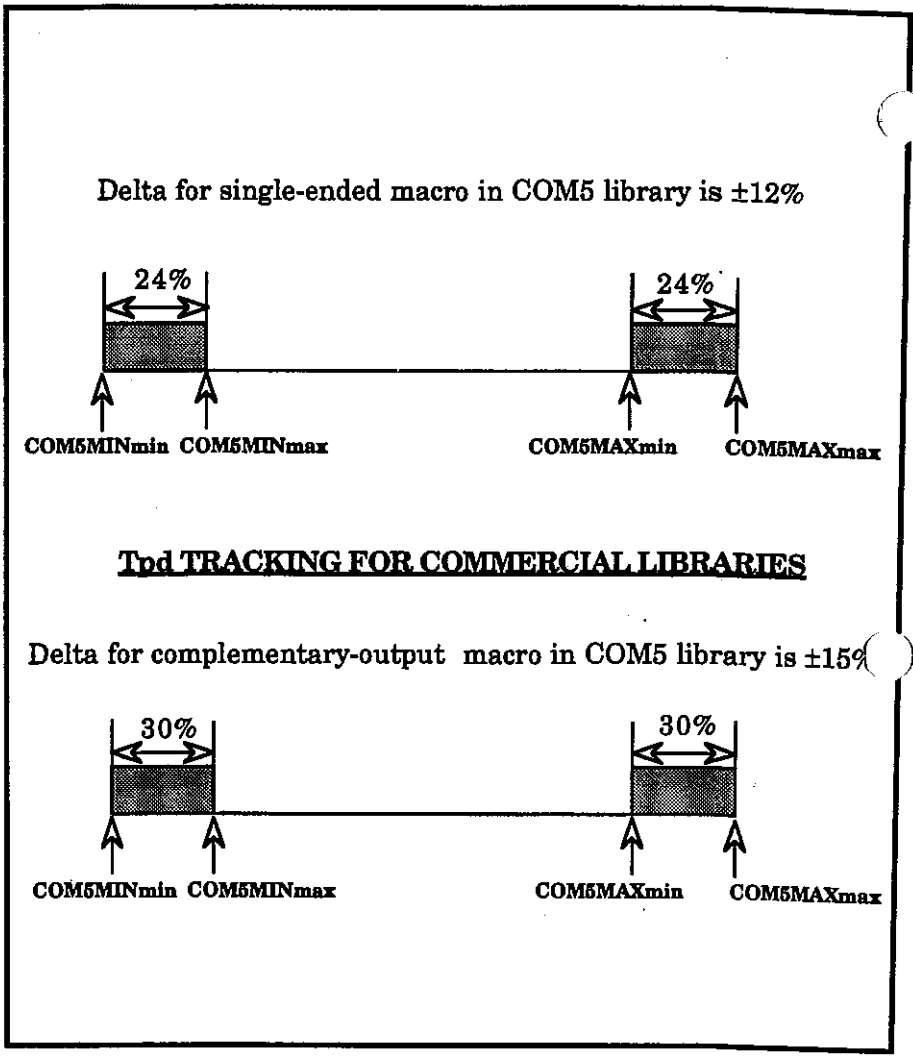


Figure 3-2b Example Of Tracking For Com5 Operating Conditions, Intrinsic Delays Only

Signal Balancing Distortion Minimization

The case where two paths are required to be identical in performance is common. The best results are obtained when the macros are identical macros and are identically loaded, including wire load, and the total load is kept small. Since placement cannot be assumed to be able to solve all problems in all cases, the judicious use of parallel structures (such as buffer trees) to reduce loading in a path and the use of pulse distortion minimization techniques, such as inversion of the signal at each macro, will help.

For ECL output operation at 100MHz and above, pulse distortion minimization methods should be used. These include: 1) signal inversion on alternating macros; 2) short interconnect, a function of fan-out and metal length; and 3) balanced rising-edge and falling-edge k-factors.

The final analyses for pulse stretch, pulse shrink and balanced path delays must be performed using Back-Annotation.

FRONT-ANNOTATION LOAD UNITS

The Front-Annotation statistical wire load units table was calculated using the following :

$$LU = a * (\text{pins driven})^{**} b$$

TABLE 3-8
ESTIMATED
FRONT-ANNOTATION LOAD UNITS

ARRAYS	b	a
Q20120	0.70	12.00
Q20080	0.72	11.00
Q20045	0.75	9.00
Q20P025	0.80	7.50
Q20025	0.80	7.50
Q20P010	0.85	6.00
Q20010	0.85	6.00

used to generate estimated wire load table

The Front-Annotation delay files are derived using this data.

BACK-ANNOTATION LOAD UNIT CONVERSION FACTORS

The Back-Annotation delay file is derived using the following:

TABLE 3-9
BACK-ANNOTATION LOAD UNITS:
CONVERSION FACTORS
LU/mm

	RISING	FALLING	
Metal 2	10	10	c2
Metal 3	10	9	c3

LnetBA = LU = (M3 * c3) + (M2 * c2)

where:

M3 = length of metal 3 in mm
M2 = length of metal 2 in mm
c3 = conversion in LU/mm
c2 = conversion in LU/mm

LU = load units due to actual metal, used as Lnet

Annotation Differences

Differences between the Front-Annotation simulations performed at the customer's site and the Back-Annotation simulations performed at AMCC include the differences between:

1) the estimated net delay due to estimated metal length and the actual delay due to actual metal length,
   and
2) the estimated delay due to package pin capacitance, using estimated or averaged package pin capacitance and the actual delay due to package pin capacitance. The actual pin capacitance for each output signal is found using the placement file and package database.

Differences between the release macro library and the internal macro library at AMCC may also exist due to on-going development and refinement of the library. AMCC periodically releases library updates to keep differences between the field and in-house versions to a minimum. If you have questions on possible differences that might affect a critical path, consult AMCC.

AMCC will perform Back-Annotation simulations using the internal library. Back-Annotation source files are available to allow you to perfrom Back-Annotated simulation at your site.

Section 4
External Set-Up and Hold Times

External Set-Up and Hold Times

INTRODUCTION

When the input to the data or the clock or both pins on a flip/flop or a latch are supplied from an external signal, then the external set-up and hold times must be computed. These computations must be for the worst-case and account for processing skew.

To meet design submission requirements, both the maximum worst-case and the minimum worst-case equations need to be computed to determine the worst-case window for external set-up and hold times for the specified operating conditions. Both rising edge and falling edge input path propagation must be evaluated. (For deeply-nested paths, consult AMCC applications.)

Note: Results computed or derived from simulations using Front-Annotation data cannot be considered as the circuit specification.

Figure 4-1 illustrates the delay paths. The *data delay path* is T_D; the *clock delay path* is T_C.

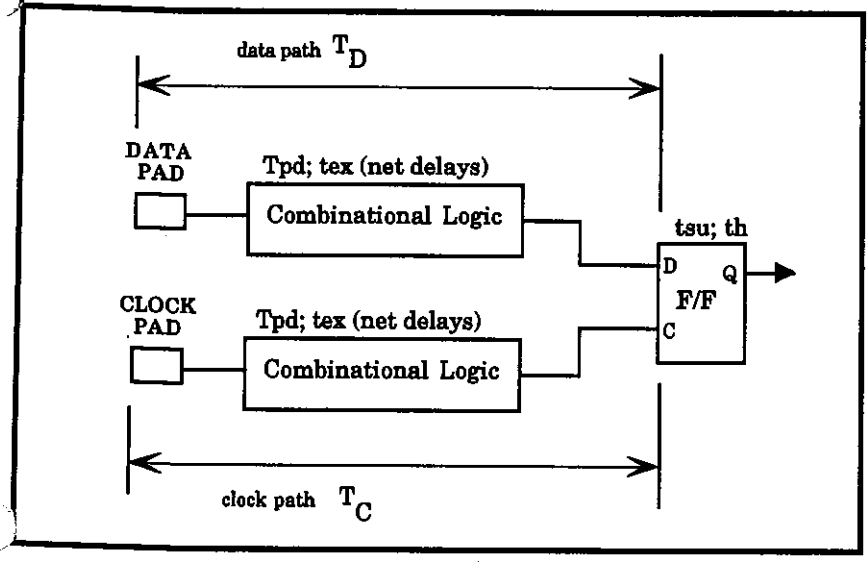


Figure 4-1 External Set-Up and Hold Paths

SET-UP TIME - GENERIC EQUATION
COM5 and MIL5 LIBRARIES

When computing the set-up time, it is desirable to assume that the data propagation path delay is the worst-case maximum and that the clock path propagation delay is a worst-case minimum for the operating conditions. The generic external set-up time equation is:

$$tsu_{external} = tD_{max} - tC_{min} + Tsu_{macro_{max}}$$

Given the MAX and MIN libraries, the external set-up time equation becomes as shown in Table 4-1 for the MIL5 and COM5 libraries.

TABLE 4-1 SET-UP TIME EQUATIONS *

MILITARY:

$$tsu_{MIL5MAX} = tD_{MIL5MAXmax} - tC_{MIL5MAXmin} + Tsu_{MIL5MAX}$$
$$tsu_{MIL5MIN} = tD_{MIL5MINmax} - tC_{MIL5MINmin} + Tsu_{MIL5MAX}$$

COMMERCIAL:

$$tsu_{COM5MAX} = tD_{COM5MAXmax} - tC_{COM5MAXmin} + Tsu_{COM5MAX}$$
$$tsu_{COM5MIN} = tD_{COM5MINmax} - tC_{COM5MINmin} + Tsu_{COM5MAX}$$

Both MIL5MAX and MIL5MIN or both COM5MAX and COM5MIN set-up times must be computed and the largest external set-up time noted on design submission. Refer to Table 4-3 for the definitions of the terms used in the equations.

HOLD TIME - GENERIC EQUATION
COM5 and MIL5 LIBRARIES

When computing the hold time, it is desirable to assume that the data propagation path delay is the worst-case minimum and that the clock path propagation delay is a worst-case maximum for the operating conditions.

The generic external hold time equation is:

$$th_{external} = tC_{max} - tD_{min} + Th_{macro_{max}}$$

Given the MAX and MIN libraries, the external hold time equation becomes as shown in Table 4-2 for the MIL5 and COM5 libraries.

TABLE 4-2 HOLD TIME EQUATIONS *

MILITARY:
$th_{MIL5MAX} = tC_{MIL5MAXmax} - tD_{MIL5MAXmin} + Th_{MIL5MAX}$ $th_{MIL5MIN} = tC_{MIL5MINmax} - tD_{MIL5MINmin} + Th_{MIL5MAX}$
COMMERCIAL:
$th_{COM5MAX} = tC_{COM5MAXmax} - tD_{COM5MAXmin} + Th_{COM5MAX}$ $th_{COM5MIN} = tC_{COM5MINmax} - tD_{COM5MINmin} + Th_{COM5MAX}$

Both MIL5MAX and MIL5MIN or both COM5MAX and COM5MIN hold times must be computed and the largest external hold time noted on design submission. Refer to Table 4-3 for the definitions of the terms used in the equations.

TABLE 4-3
TERMINOLOGY DEFINITIONS

Defining a "memory macro" as a latch, a flip/flop or an MSI containing one or the other, the terms used in the equations for the MIL5MAX and COM5MAX libraries are defined below. Terms for the other libraries (MIL5MIN and COM5MIN) would be similarly defined.
$^{t}D_{MIL5MAXmax}$ data path propagation delay from the circuit input and up to the memory macro data input pin; computed using Front-Annotation methodology prior to layout, Back-Annotation after layout; computed with the maximum values of the Tpd delays and the k-Factors from the MIL5MAX library.
$^{t}D_{COM5MAXmax}$ data path propagation delay from the circuit input and up to the memory macro data input pin; computed using Front-Annotation methodology prior to layout, Back-Annotation after layout; computed with the maximum values of the Tpd delays and the k-Factors from the COM5MAX library.
$^{t}D_{MIL5MAXmin}$ data path propagation delay from the circuit input and up to the memory macro data input pin; computed using Front-Annotation methodology prior to layout, Back-Annotation after layout; computed with the minimum values of the Tpd delays and the k-Factors from the MIL5MAX library.
$^{t}D_{COM5MAXmin}$ data path propagation delay from the circuit input and up to the memory macroo data input pin; computed using Front-Annotation methodology prior to layout, Back-Annotation after layout; computed with the minimum values of the Tpd delays and the k-Factors from the COM5MAX library.

TABLE 4-3 Continued
TERMINOLOGY DEFINITIONS

$^{t}C_{MIL5MAXmax}$ clock path propagation delay from the circuit input and up to the memory macro clock input pin; computed using Front-Annotation methodology prior to layout, Back-Annotation after layout; computed with the maximum values of the Tpd delays and the k-Factors from the MIL5MAX library.
$^{t}C_{COM5MAXmax}$ clock path propagation delay from the circuit input and up to the memory macro clock input pin; computed using Front-Annotation methodology prior to layout, Back-Annotation after layout; computed with the maximum values of the Tpd delays and the k-Factors from the COM5MAX library.
$^{t}C_{MIL5MAXmin}$ clock path propagation delay from the circuit input and up to the memory macro clock input pin; computed using Front-Annotation methodology prior to layout, Back-Annotation after layout; computed with the minimum values of the Tpd delays and the k-Factors from the MIL5MAX library.
$^{t}C_{COM5MAXmin}$ clock path propagation delay from the circuit input and up to the memory macro clock input pin; computed using Front-Annotation methodology prior to layout, Back-Annotation after layout; computed with the minimum values of the Tpd delays and the k-Factors from the COM5MAX library.
Tsu_{macro} = Tsu as specified in Section 6 Th_{macro} = Th as specified in Section 6

CONVERTING COM5 TO COM4, MIL5 TO MIL4

The adjustment factors to convert the COM5 and MIL5 data to COM4 and MIL4 were provided in Section 3. They would also be applied to the computation for external set-up and hold times as shown in Tables 4-4 and 4-5.

Table 4-4 Set-Up Time Equations

MILITARY:

$$tsu_{MIL4MAX} = tD_{MIL4MAXmax} - tC_{MIL4MAXmin} + Tsu_{MIL4MAX}$$
$$tsu_{MIL4MIN} = tD_{MIL4MINmax} - tC_{MIL4MINmin} + Tsu_{MIL4MAX}$$

COMMERCIAL:

$$tsu_{COM4MAX} = tD_{COM4MAXmax} - tC_{COM4MAXmin} + Tsu_{COM4MAX}$$
$$tsu_{COM4MIN} = tD_{COM4MINmax} - tC_{COM4MINmin} + Tsu_{COM4MAX}$$

Both MIL4MAX and MIL4MIN or both COM4MAX and COM4MIN set-up times must be computed and the largest external hold time noted on design submission.

TABLE 4-5 HOLD TIME EQUATIONS

MILITARY:

$$th_{MIL4MAX} = tC_{MIL4MAXmax} - tD_{MIL4MAXmin} + Th_{MIL4MAX}$$
$$th_{MIL4MIN} = tC_{MIL4MINmax} - tD_{MIL4MINmin} + Th_{MIL4MAX}$$

COMMERCIAL:

$$th_{COM4MAX} = tC_{COM4MAXmax} - tD_{COM4MAXmin} + Th_{COM4MAX}$$
$$th_{COM4MIN} = tC_{COM4MINmax} - tD_{COM4MINmin} + Th_{COM4MAX}$$

Both MIL4MAX and MIL4MIN or both COM4MAX and COM4MIN hold times must be computed and the largest external hold time noted on design submission.

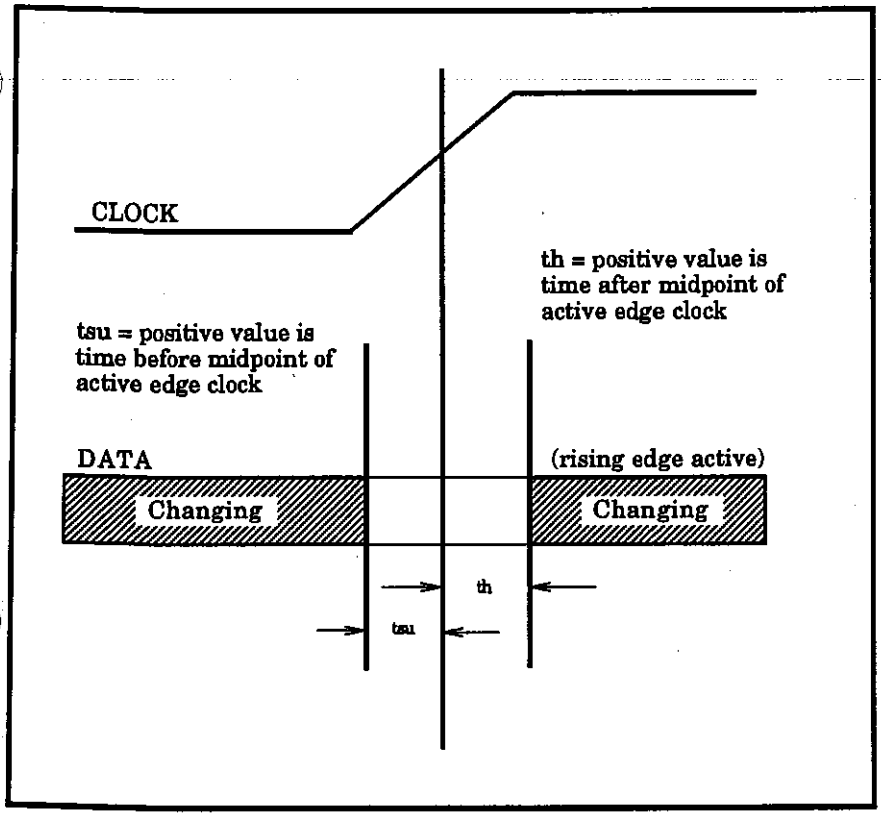


Figure 4-2 External Set-Up and Hold Times - Interpretation

Figure 4-2 diagrams the definitions of positive set-up and hold times. Data must be held stable relative to the associated clock during these times. The time span indicated by the set-up and hold time is referred to as a timing "window". This diagram is for positive set-up and positive hold times in relation to a rising edge active clock.

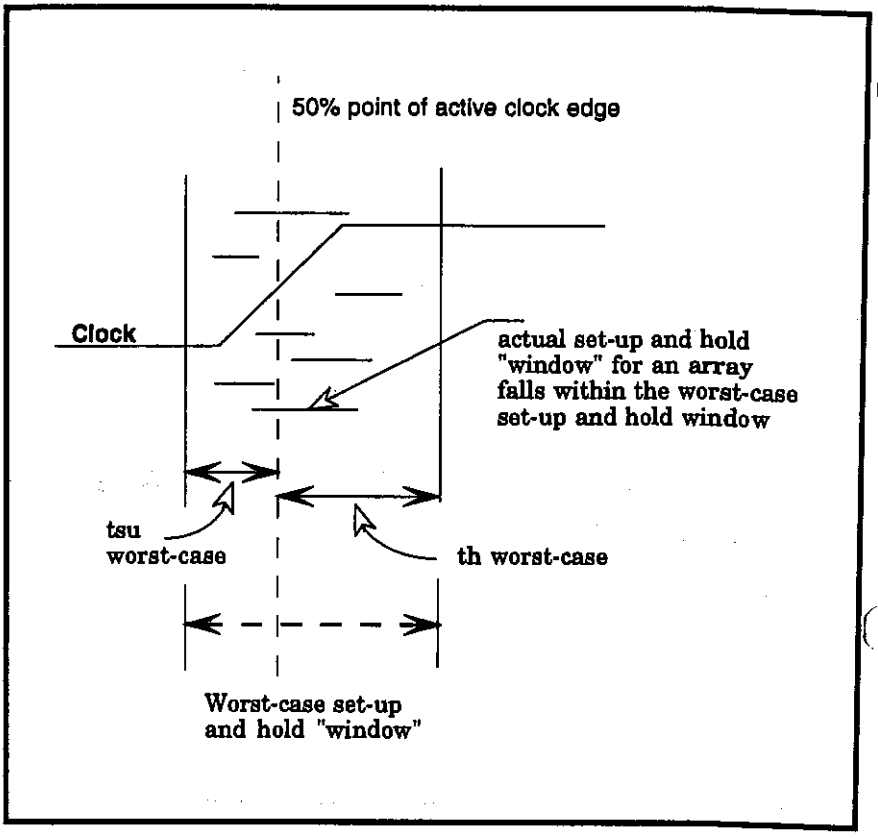


Figure 4-3 Worst-Case Range

Figure 4-3 diagrams the worst-case window produced from the maximum set-up time and the maximum hold time. The conditions under which these two values are computed are inconsistent and contradictory with each other thereby ensuring that the set-up and hold time timing "window" for any single array is contained within the computed worst-case range. This diagram is for rising edge active clock and positive set-up and positive hold times.

Computing External Set-Up and Hold Using the Q20000 Libraries

Assume that external set-up time for the MIL5MAX library is to be computed.

$$tsu_{MIL5MAX} = tD_{MIL5MAXmax} - tC_{MIL5MAXmin} + Tsu_{MIL5MAX}$$

To compute the data path, TD, find the Tpd delays for all macros in the path, reading the values from the design manual. Find the net delays using the k-factors specified in the design manual. The values used are the ones on the right or the MAXmax values from the MIL5 library.

$tD_{MIL5MAXmax}$ = sum of all Tpd delays and all net delays computed using the k-factors read as MAXmax from the manual.

To compute the clock path, TC, find the MAXmax Tpd and net delays as specified in the design manual as was done for the data path. In this case, however, each macro must be examined to determine if it is a single-ended or a complementary output macro. For all single ended macros, the MAXmax value of Tpd is multiplied by 0.64. For all complementary-output macros, the MAXmax value of Tpd is multiplied by 0.54. For all internal net delays, regardless of the type of driving macro, multiply by 0.76. (Refer to Section 3, Table 3-5A.)

$tC_{MIL5MAXmin}$ = sum of all Tpd delays read as MAXmax from the manual, with each multiplied by 0.54 or 0.64 depending on the macro output configuration, and all net delays computed using the MAXmax k-factors and multiplied by 0.76.

The macro set-up time is read from the manual (no adjustment).

Assume that external set-up time for the MIL5MIN library is to be computed.

$$tsu_{MIL5MIN} = tD_{MIL5MINmax} - tC_{MIL5MINmin} + Tsu_{MIL5MAX}$$

To compute the data path, TD, find the Tpd delays for all macros in the path, reading the values from the design manual. Find the net delays using the k-factors specified in the design manual. The values used are the ones on the left or the MINmin values from the MIL5 library.

In this case, each macro must be examined to determine if it is a single-ended or a complementary output macro. For all single ended macros, the MINmin value of Tpd is multiplied by 1.36. For all complementary-output macros, the MINmin value of Tpd is multiplied by 1.46. For all internal net delays, regardless of the type of driving macro, multiply by 1.24. (Refer to Section 3, Table 3-5A.)

$^{t}D_{MIL5MINmax}$ = sum of all Tpd delays read as MINmin from the manual, with each multiplied by 1.36 or 1.46 depending on the macro output configuration, and all net delays computed using the MINmin k-factors and multiplied by 1.24.

To compute the data path, TC, find the Tpd delays for all macros in the path, reading the values from the design manual. Find the net delays using the k-factors specified in the design manual. The values used are the ones on the left or the MINmin values from the MIL5 library.

$^{t}C_{MIL5MINmin}$ = sum of all Tpd delays and all net delays computed using the k-factors read as MINmin from the design manual

The macro set-up time is read from the manual (no adjustment).

Section 5
Power Computation

Power Computation

The total current (internal cells and I/O interface cells) is used to compute the worst-case power dissipated by the logic array. The worst-case power as it relates to junction temperature is used to examine the packaging and the heat-sink requirements of the final product.

The total current is a function of: 1) the interface and internal macros used; 2) the options selected for those macros; 3) the overhead current, which is a function of the array chosen and the I/O mode; 4) the output terminations; and 5) the frequency of operation, which determines the AC current used by ECL inputs and ECL Darlington outputs, and all internal macros. The total worst-case current for interface macros, internal macros and overhead is found by using the correct worst-case current multipliers.

The total power dissipated by a device is a function of: 1) the total worst-case interface, internal and overhead current; 2) the worst-case power supply; 3) the ECL terminations, and 4) the AC power dissipated by the ECL input, Darlington outputs and internal macros.

AMCCERC will compute the DC power for a captured circuit. The computation may need adjustments as defined in this section.

MACRO OPTIONS

Once the design is blocked and the macros selected, review the timing requirements and adjust the macros by option. Most of the macros for the Q20000 Series come with options. The L-option macros are slower than the S-option macros. They have a lower maximum frequency of operation and lower dissipated power. The H-option macros are faster than the S-option macros and have higher dissipated power.

S-, L- and H-option macros drive 18 loads. The TTLMIX bidirectional macro drives 9 loads. The driver macros drive 32 loads. Because of Turbo, fan-out drive will not be a major factor in choosing macro options; speed requirements and power considerations will be the major considerations.

During design, H-option macros, high fan-out drivers and other high-current macros should be used judiciously to avoid unnecessarily high current/power dissipation. The use of L-option macros when available can help balance the use of high-current macros providing speed/power programmability if and only if the minimum pulse widths are not violated.

To estimate power prior to schematic capture, create a macro occurrence table of all interface and internal macros used, differentiated by option, and list the current dissipated by each. Keep I_{CC} and I_{EE} currents separate.

STATE-DEPENDENT CURRENT

For some interface macros (as defined in Section 6, Macro Library documentation), the current is state-dependent. The I_{CC} and I_{EE} values for many of the interface macros are specified for *high* and *low* input. The 3-state outputs and bidirectionals are specified for enabled and disabled states.

To compute actual power for any given state of the circuit, the state and operating duty cycle of each I/O would have to be known, requiring a detailed vector analysis.

Without specific and unique operating duty cycles, the following procedure is recommended:

For 2-state outputs (*high, low*), calculate I_{EE} and I_{CC} as the average of the two values (50% *high*, 50% *low*).

For 3-state outputs (*high, low, Z* or *input*) calculate as 50% disabled high impedance Z state or input mode, 25% enabled *high* and 25% enabled *low*.

PART 1: MACRO DC POWER DISSIPATION

COMPUTING THE MAXIMUM WORST CASE DC POWER- SUMMARY

To compute the worst-case power, perform the following steps.

Sum all interface macro currents and multiply by the interface macro worst-case current multiplier, 1.3. Keep I_{EE} and I_{CC} separate.

Sum all internal macro currents and multiply by the internal macro worst-case current multiplier, 1.25. Keep I_{EE} and I_{CC} separate.

Find the I_{EE} and I_{CC} overhead currents and multiply them by the overhead worst-case current multiplier, 1.25. Keep I_{EE} and I_{CC} separate.

Add all I_{EE} currents together.

Add all I_{CC} currents together.

Find the worst-case V_{CC} and V_{EE} voltages.

Multiply $I_{EE} * V_{EE}$.

Multiply $I_{CC} * V_{CC}$.

Compute ECL static power dissipation:

Peo = 1.3 * termination current * number of outputs

Add all items together.

This is the worst-case DC power dissipated by the circuit.

MACRO OCCURRENCE TABLE

A macro occurrence table can be constructed prior to design capture to assist in the computation of interface current and power dissipation. A macro occurrence table should provide the data necessary to compute the worst-case DC power dissipated by the circuit.

WORST-CASE MAXIMUM CURRENT MULTIPLICATION FACTORS

The Q20000 Series uses three worst-case current multipliers, one for core macros, one for interface macros and one for overhead current.

TABLE 5-1
WORST-CASE MAXIMUM CURRENT MULTIPLIERS

CORE WCCM1	INTERFACE WCCM2	OVERHEAD WCCM3
1.25	1.3	1.25

COMPUTE THE TOTAL TYPICAL INTERFACE MACRO CURRENT

Compute the total current used by all occurrences of each interface macro and sum these totals to find:

$I_{interfaceEE}$ = SUM OF Interface MACROS I_{EE} CURRENT
$I_{interfaceCC}$ = SUM OF Interface MACROS I_{CC} CURRENT

Unless the circuit uses a single-power supply these two sums must be kept separate. Note: ICC will only exist in +5V REF ECL circuits (100% ECL or ECL/TTL MIX with a single +5V supply).

Compute the Worst-Case Interface Current

Multiply both sums by the worst-case current multiplier for the interface macros, 1.30, to obtain the worst-case current due to interface macros.

$I_{interfaceCC_{wc}}$ = 1.30 * interface I_{CC}
$I_{interfaceEE_{wc}}$ = 1.30 * interface I_{EE}

COMPUTE THE TOTAL TYPICAL INTERNAL MACRO CURRENT

Compute the total current used by all occurrences of each internal macro and sum these totals to find:

$I_{internalCC}$ = SUM OF Internal MACROS I_{CC} CURRENT
$I_{internalEE}$ =SUM OF Internal MACROS I_{EE} CURRENT

Unless the circuit uses a single-power supply these two sums must be kept separate. Note: ICC will only exist in +5V REF ECL circuits (100% ECL or ECL/TTL MIX with a single +5V supply).

Compute the Worst-Case Internal Current

Multiply both sums by the worst-case current multiplier for the internal macros, 1.25, to obtain the worst-case current due to internal macros.

$I_{internalCC_{wc}}$ = 1.25 * internal I_{CC}
$I_{internalEE_{wc}}$ = 1.25 * internal I_{EE}

COMPUTE THE TOTAL TYPICAL OVERHEAD CURRENT

Compute the total overhead current used by the circuit.

$I_{overheadCC}$ = Table 5-2
$I_{overheadEE}$ = Table 5-2

Unless the circuit uses a single-power supply these two terms must be kept separate. Refer to Table 5-2 for the current. The overhead current is fixed regardless of I/O cell or internal cell usage.

TABLE 5-2
TYPICAL OVERHEAD CURRENT (IN MA)

ARRAY	ECL MODE (1) IEE,mA	ECL MODE DECL (2) IEE/ICC,mA	ECL/TTL MIXED MODE (1) IEE/ICC,mA	ECL/TTL MIXED MODE (2) ICC
Q20120	410	410/26	410/26	410
Q20080	220	220/26	220/26	220
Q20045	187	187/26	187/26	187
Q20P025	Not Allowed	Not Allowed	101/26	101
Q20025	128	128/26	128/26	128
Q20P010	Not Allowed	Not Allowed	63/13	63
Q20010	67	67/13	67/13	67

(1) DUAL SUPPLY
(2) SINGLE SUPPLY

Note: the DECL and the MIXED ECL/TTL dual supply arrays dissipate the same overhead current. In the case of the DECL circuit, some of the macros which require the use of two power supplies will dissipate an ICC current component.

The macro occurrence ERC includes overhead current in the power dissipation computation.

Compute The Worst-Case Overhead Current

Multiply both I_{CC} and I_{EE} by 1.25 to determine the worst-case maximum overhead current.

$$I_{overheadCC_{wc}} = 1.25 * Ioverhead\ CC$$
$$I_{overheadEE_{wc}} = 1.25 * Ioverhead\ EE$$

SUM THE I_{CC} AND I_{EE} CURRENTS

Sum the internal macro, interface macro and overhead worst-case currents, keeping ICC and IEE separate.

$$I_{CCwc} = I_{internalCC_{wc}} + I_{interfaceCC_{wc}} + I_{overheadCC_{wc}}$$
$$I_{EEwc} = I_{internalEE_{wc}} + I_{interfaceEE_{wc}} + I_{overheadEE_{wc}}$$

MULTIPLY BY THE WORST-CASE VOLTAGE

The worst-case voltage is dependent on whether the circuit is *commercial* or *military*. The typical variation is shown in Table 5-3. For commercial circuits, with a -5.2V or a +5V supply, the voltage variation is usually ±5%.

For military circuits, the voltage variation is usually ±10%. Note the worst-case voltage for the -4.5V supply as listed in Table 5-3 and on the data sheet, where -4.5V supply varies from -4.5V to -4.8V for military and from -4.2V to -4.8V for commercial.

TABLE 5-3
WORST-CASE VOLTAGES

NOMINAL	COMMERCIAL	MILITARY
+5.0V	+5.25V	+5.5V
-5.2V	-5.46V	-5.72V
-4.5V	-4.8V	-4.8V

Multiply the worst-case DC current by the appropriate worst-case voltage:

$$PEE_{DC} = IEE_{wc} * VEE_{wc}$$
$$PCC_{DC} = ICC_{wc} * VCC_{wc}$$

ECL STATIC POWER P_{eo}

The equation used by the AMCC ***MacroMatrix amccerc*** software to compute ECL static power dissipation for ECL outputs is:

$$P_{eo} = XXmA * 1.3V * NUMBER\_OF\_ECL\_OUTPUTS$$

where XX is the current based on the termination.

The 1.3V term represents the average between V_{OH} and V_{OL}. This is considered to be the statistical worst-case for this function.

If there is more than one termination, the power for each type of termination is computed and summed to find the total ECL outputs.

ECL OUTPUT TERMINATION CURRENT

The ECL termination current I_{OEF} is a function of the actual load. When a macro is selected it should be capable of driving a resistive load equal to or greater than its rating. The ERCs will assume the load to be equal to the rated load.

The ECL output termination currents shown in Table 5-4 are used by the AMCC MacroMatrix ***amccerc*** software. The currents shown are the average current (average of I_{OH} and I_{OL}) and represent 50% terminations active.

TABLE 5-4
ECL 10K/100K TERMINATION CURRENT*

25 ohm	28.0 mA
50 ohm	14.0 mA

* the average current (average of I_{OH} and I_{OL}) for termination to -2V

Note: I_{OEF} is sourced from the termination voltage, -2V, for standard reference ECL. For +5VREF ECL, I_{OEF} is sourced from the +5V supply. This changes the I_{CC} maximum for the array to be equal to total DC power divided by V_{CC}.

- **When 50 OHM or 25 OHM Terminations Not Used**

The ERC software cannot detect when a load does not match that for which the macro is rated. Therefore, if other ECL output load resistances are used, the actual current value must be computed for use in this equation.

For a termination voltage of -2V, to find the average current in mA use:

$$I(\text{in mA}) = \frac{0.7}{R*(10^{-3})} \quad \text{for any R}$$

For the Q20000 Series arrays, the macro occurrence ERC uses either a 50 ohm or a 25 ohm to -2V termination, depending on the macro.

- **When $V_T \neq$ -2V**

For other termination voltages, an adjustment to the power dissipation computation must be made by the designer. For a termination voltage V_T, to find the average current in mA use:

$$I(\text{in mA}) = \frac{(-1.3V - VT)}{R*(10^{-3})} \quad \text{for any R}$$

- **ECL Termination Current - Darlington ECL Output**

Darlington ECL outputs are treated as a standard ECL output for power computations.

- **ECL Termination Current - Series Termination; CML Macros**

There is no I_{OEF} output current for on-chip series termination or CML outputs. The current specification for these macros includes any load-dependent dissipation.

SUM THE RESULT - TOTAL DC POWER

Sum the results of the macro and overhead current power computations with any ECL output macro static power dissipation to obtain the total worst-case DC power dissipation for the circuit:

$$Pd_{DC} = P_{CC_{DC}} + P_{EE_{DC}} + Peo$$

The result is the total worst-case DC power dissipated by the circuit on the target array.

MACRO OCCURRENCE AND DC POWER DISSIPATION AMCCERC REPORT- ADJUSTING THE DC POWER RESULT

For tbose I/O macros having state dependent I_{CC} and I_{EE} values, the MacroMatrix ***amccerc*** program will use the worst-case value. Manual computation is required if a more representative evaluation is required.

For macros with two dissipation values (I_{CC} input *high*/I_{CC} input *low*), the numerical average of the two values in Section 6 should be used, assuming a 50% duty cycle or data mix.

For 3-state or bidirectional macros, the assumption should be 50% high-Z (or input), 25% output *high* level, and 25% output *low* level.

If the actual application is known to have signal statistics significantly different from these assumptions, the calculations should reflect the more accurate state mix.

amccerc also uses the maximum (military or commercial) voltage in the power computations. Initial evaluations done by the customer or AMCC may use nominal voltage in the power calculations for consistancy with industry practice. When this approach has been used, it should be noted on the Power worksheet or other appropriate design submission document.

PART 2: AC POWER DISSIPATION

MACRO OCCURRENCE WORKSHEET

A macro occurrence worksheet for interface and internal logic macros can be constructed prior to design capture to assist in the computation of AC power dissipation. An AC Power macro occurrence worksheet for the interface and internal logic should provide:

- A list of the different macros differentiated by option;
- The number of times each macro appears on the schematics;

amccerc produces a BiCMOS/Bipolar Power Computation Worksheet which lists macros and their occurrences and which can be used for AC power analysis.

COMPUTING AN ESTIMATE OF AC POWER DISSIPATION

The equations used to compute internal cell AC power dissipation are:

For all ECL Darlington output macros:

$$Pd_{darAC} = f * n * 15 \text{ microwatts}$$

where
f = maximum frequency of the Darlington outputs in MHz
n = number of ECL Darlington output macros toggling at frequency *f*

The number of Darlington outputs can be determined from the I/O statistics ***amccerc*** report and from the AC Bipolar/BiCMOS Macro Occurrence worksheet.

Count the number of Darlington output macros switching at the fastest frequency and compute the power due to those macros. Count the number of Darlington output macros switching at the next fastest frequency and compute their power. Repeat for all Darlington output macros.

For all ECL inputs and all internal macros:

$$Pd_{IAC} = 0.2 * f * n * 3.25 \text{ microwatts}$$

where
f = maximum frequency of operation in MHz
n = number of ECL input macros and number of internal macros
0.2 represents the assumed 20% of macros switching at one time

The number of internal macros can be found from the Population report in ***amccerc***. The number of ECL input macros can be found in the Population I/O Statistics report.

Sum the two results together and convert to watts (or to the same units as was used for DC power). This equation provides an estimate of the worst-case AC power dissipation for the Q20000 array.

$$Pd_{AC} = Pd_{IAC} + Pd_{darAC}$$

Use the same equation for military and commercial computations.

PART 3: FINAL RESULT

Add the DC power computation result to the AC power computation result.

$$Pd = Pd_{DC} + Pd_{AC}$$

The result is the worst-case power dissipation to be used in computing junction temperature.

If the unloaded trace is a 100 Ohm line (w/h = 0.36), the capacitance per unit length, Cd, is 0.61 pF/cm. The added capacitance of 10 pF every 2 inches or 5 cm gives an effective CD value of 2 pF/cm. If we insert these values in equation (6):

$$Z_3 = \frac{100 \text{ Ohms}}{\sqrt{1 + \frac{2 \text{ pF/cm}}{0.61 \text{ pF/cm}}}} \qquad (27)$$

$$= 100/2.07 = 48 \text{ Ohms}$$

This is the effective impedance of the combined delay line structure. Additionally, the original nominal propagation delay of 350 psec/5cm or 70 psec/cm is now 145 psec/cm or 725 psec/5cm.

Since the drive capability of the output macro is given as capacitive load as a function of frequency, the effective impedance should be considered as an equivalent capacitive reactance at a specified frequency. If a 100 nsec period for the address line is assumed, the effective frequency is on the order of 10 MHz. For this frequency the equivalent capacitive load is:

$$C = \frac{1}{2 \, p \, f \, X_C} \qquad (28)$$

$$= 1/(2 * 3.1459 * 10 \text{ MHz} * 48 \text{ Ohms})$$

$$= 330 \text{ pF}$$

As a comparison, if the frequency of operation were 30 MHz, the effective load capacitance would be:

$$C = 1/(2 * 3.1459 * 30 \text{ MHz} * 48 \text{ Ohms}) \qquad (29)$$
$$= 110 \text{ pF}$$

If the spacing of the 10 pF capacitors is increased to 10 cm, the resulting impedance is 61 Ohms. At 10 MHz the effective capacitance drops to 261 pF.

If the distance to the first added capacitive load is increased such that the round-trip delay is greater than the rise time of the signal, the model is one of two sections of transmission line, the first of unloaded impedance (100 Ohms), and the second of loaded impedance (48 Ohms). The first section presents a load on the TTL output of:

$$C = 1/(2 * 3.1459 * 10\ \text{MHz} * 100\ \text{Ohms}) = 160\ \text{pF}. \quad (30)$$

For these impedances, the reflected signal from the discontinuity is approximately 35%. If the distance just meets the risetime criteria (2 x Tpd = 3 nsec), then the reflected signal represents an additional load component phase shifted by approximately 10 degrees. This phase shift slightly decreases the additional loading effect to 34%.

As the distance (and phase shift) increases, the additional loading effect will drop off until there is actually an increase in the effective impedance at 180 degrees (and at 360 degree multiples thereafter). This area of operation for TTL outputs begins at approximately 9 inches of line length before the added loads.

The 180 degree shift point at 10 MHz operation would require over 160 inches (13 feet) of line length, so the cancellation effects (not to mention the multiple resonance points) are not likely to be observed in a practical system application.

For TTL outputs and moderate frequencies this distributed load equivalent impedance method is reasonably accurate. This procedure allows the user to determine whether a desired load configuration complies with capacitive load limits established to assure signal integrity or device reliability. While they do give some idea of resultant risetime degradation, a detailed analysis for wave shape requires simulation techniques such as SPICE ™.

Section 7
Introduction to Placement

Introduction to Placement

Partial or full placement may be performed by the customer. The AMCC Placement document should be obtained from AMCC and AMCC Applications and Implementation Engineering consulted before any placement is attempted. The following are Q20000-specific rules which are an addendum to **AMCC Placement Rules and Guidelines**.

HIGH-FREQUENCY GUIDELINES

For the Q20000 Series, high-frequency is 400MHz and higher. Any I/O signal operating at ≥400MHz should follow placement restrictions (package dependent), use differential I/O macros and follow added ground guidelines.

As the input frequency becomes higher, the signal amplitude becomes smaller and therefore more susceptible to. noise. The noise signal is usually coupled from an adjacent I/O signal.

Placement - High-Frequency Pins

Certain pins on the Q20000 Series packages will be designated as high-frequency pins. For a large PGA, the substrate traces vary in geometry, yielding a wide range of associated parasitics. *For your design needs, consult AMCC Applications Engineering.*

Differential Interface - When Recommended

To maintain low timing jitter and high common mode rejection, a differential interface is recommended. The effective output edge rate of a differential signal is twice that of a single-ended signal.

Isolation with Ground

To reduce coupling, the high-frequency I/O signal should be surrounded by AC grounds.

In this case, the package pin must also be isolated, not just the array pad carrying the high-frequency signal. The specific package database will need to be consulted along with the package diagram (available from AMCC) to determine where the added grounds should be placed to provide grounds on the required package pins.

TTL outputs must always be isolated from an ECL input by either a fixed or added ground pad. Estimate one added ground or power pad between ECL and TTL groups and between ECL input and ECL output groups for isolation. These arrays do not use "quadrant" grouping as applied to other AMCC array series. Outputs are considered to be grouped together, SSOs or not. Use the IEVCC (ECL ground) for ECL isolation (standard-reference circuit). High-Speed CMOS inputs must be isolated from ECL I/O.

PLL ARRAYS - PLACEMENT OF PLL MACRO

One and only one PLL macro may be placed on any one PLL array, Q20P010, or Q20P025. It will be placed in a specific pre-defined location on the array occupying I/O and core cell resources. This location is the top of the array. (For the Q20P025, for example, the PLL macros occupies pads numbered from 58 through 111.) The PLL macro will be placed as a *hard macro* —not as individual elements or macros. ***Consult AMCC if you are attempting placement on a PLL array.***

ADDED POWER AND GROUND MACROS

Requirements for the addition of added power and ground are given in Section 2. For standard reference ECL, the IEVCC macro provides ECL I/O ground. The ITGND macro provides TTL ground for output drivers and input clamps. The ITPWR macro provides additional TTL VCC for output drivers. These macros should be placed on pads that allow them to be connected to the internal package power and ground planes. Consult AMCC for the pad restrictions for the particular array-package-I/O mode combination.

DUAL I/O CELL MACROS

Dual I/O cell macros must be placed on physically adjacent I/O cells. Consult AMCC if you are placing any dual I/O macros.

DIE PLOTS

The following pages provide example die plots for reference only. Do not attempt placement with these figures. Power pad designations and placement worksheets should be obtained from AMCC if you wish to perform any placement functions. Refer to *AMCCPKG.LST* for information on fixed power and ground location.

Figure 7-1 Q20010 Floor Plan

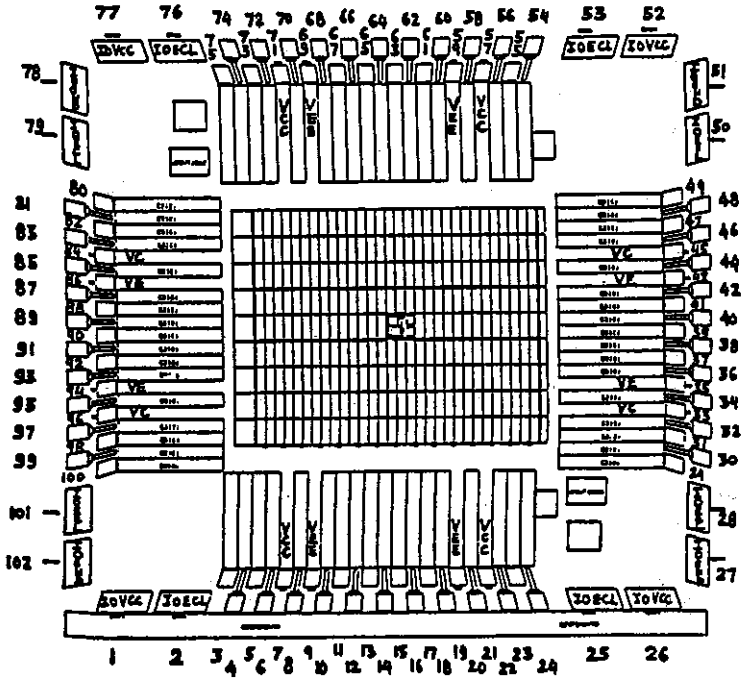


Figure 7-2 Q20010 Power Pad Designation - 100% ECL

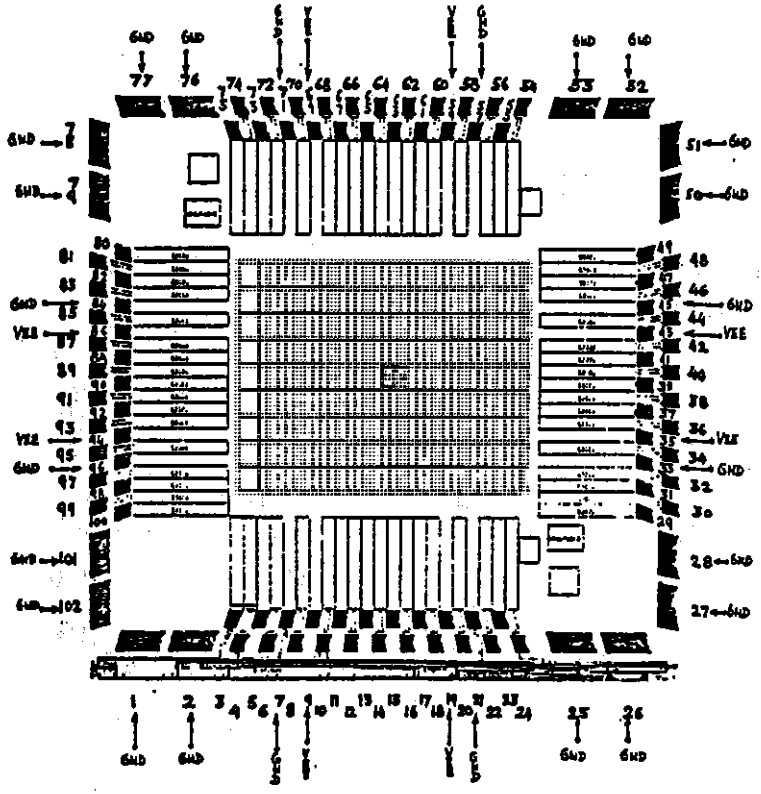


Figure 7-3 Q20010 Power Pad Designation - Mixed TTL, ECL Mode

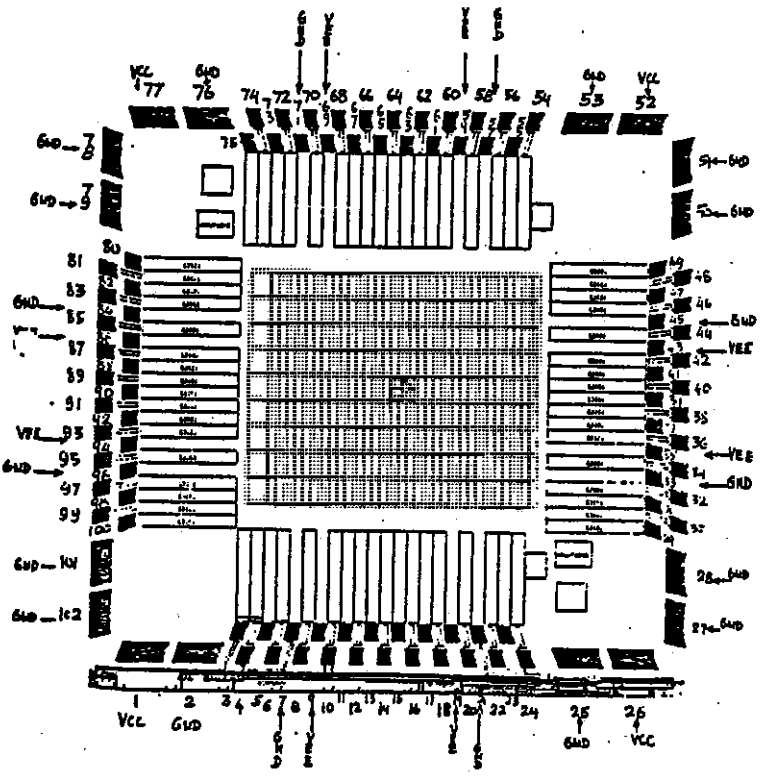


Figure 7-4 Q20080 Chip Floor Plan

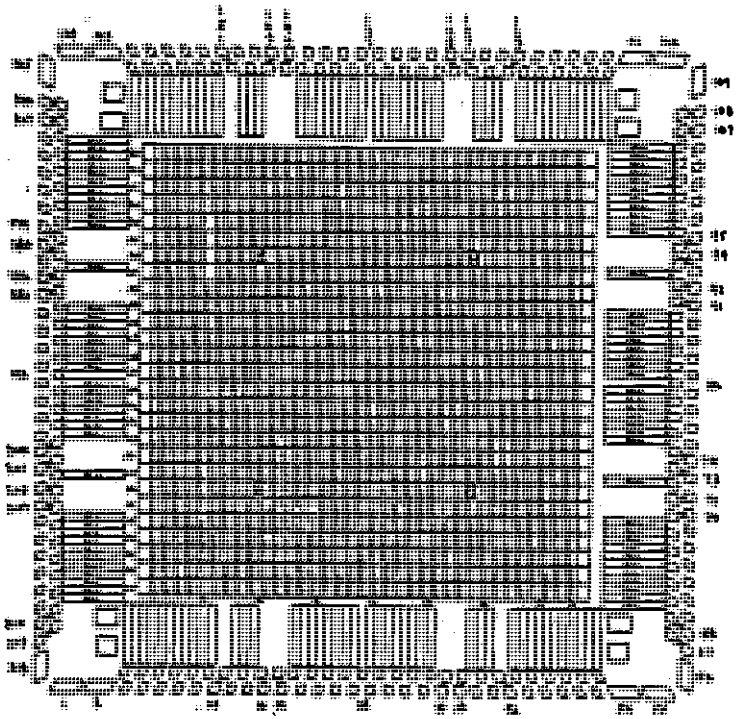


Figure 7-5 Q20080 Power Pad Designation - 100% ECL Mode

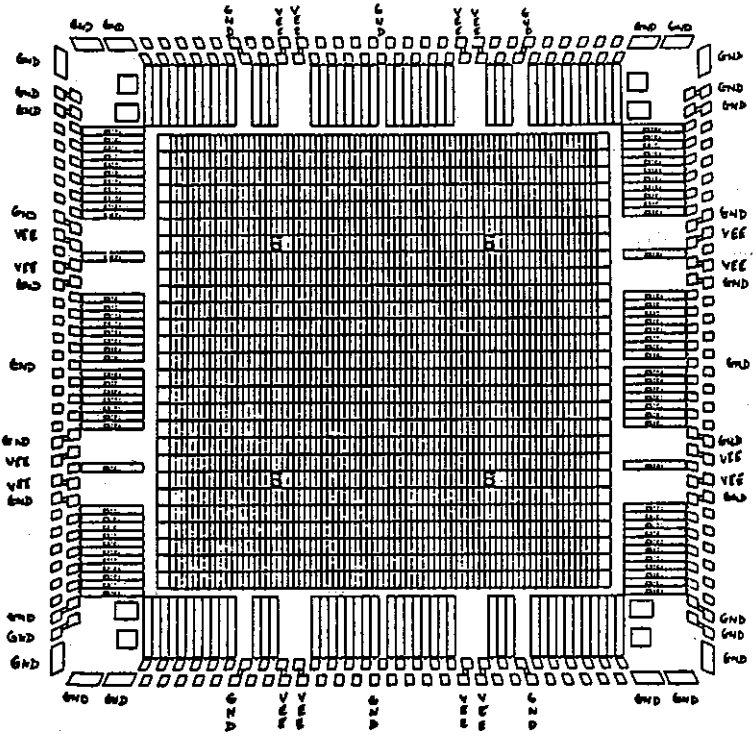
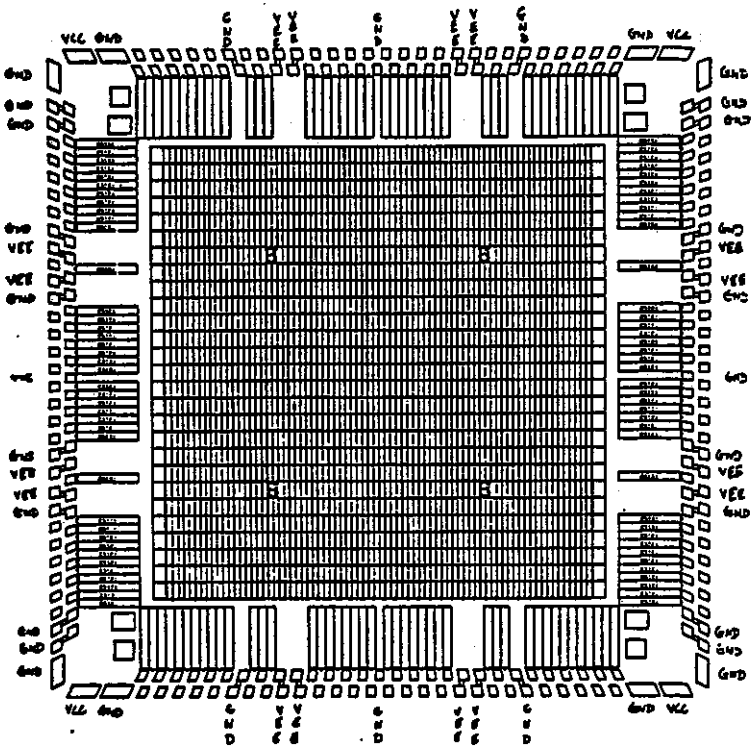


Figure 7-6 Q20080 Power Pad Designation - Mixed TTL, ECL Mode



Section 8
Package Selection

Package Selection

INTRODUCTION

Thermal and electrical considerations can affect the selection of the package and heatsink. Package and heatsink selection should always be a consideration from the beginning of the design process. It should be a factor in the initial selection of the array series and the array within the series.

This section covers the mechanics of junction temperature computation, package selection, cooling, heatsink selection, and documents package signal pins, the junction-case thermal coefficient and power/grounds. To assist the designer in understanding the default package pin capacitance used by Front-Annotation mode ***amccpackage***, the default capacitances are also documented. To understand **amccpackage**, refer to Volume III, Section 5, the ***AMCCPACKAGE User's Guide.***

REQUIRED TO START

Package selection requires that the designer have two computations completed:

1) the total maximum worst-case power dissipation (from Section 5, ***Power Computation***);

and

2) the total number of I/O signal pads required.

Prior to design start, preliminary estimates should be calculated as part of the feasibility task. Final verification can be performed with reports generated by the **AMCC MacroMatrix Design Kit software.**

AMCCERC.LST POPULATION REPORT - REQUIRED PACKAGE PINS

The ***amccerc.lst*** population report provides both the maximum and minimum required package signal pins.

Minimum Package Signals Pins Required

MINIMUM PACKAGE SIGNAL PINS REQUIRED assumes that all added power and grounds will be placed to connect to the internal power and ground planes. It is the optimal solution. It is the sum of all I/O signals, including PLL signals, and the four fixed I/O signals for the thermal diode and AC Speed Monitor.

TABLE 8-1
ARRAY PAD COUNT LIMIT *

ARRAY NAME	ARRAY SIGNAL PADS (1)	ARRAY FIXED POWER /GROUND PADS	TOTAL ARRAY EXTERNAL PADS
Q20120	202/198	78	280
Q20080	166/162	52	218
Q20045	132/128	52	184
Q20P025	55/51 + 12 PLL	26 + 8 PLL	96/92
Q20025	104/100	36	140
Q20P010	38/34 + 12 PLL	20 + 8 PLL	68/64
Q20010	70/66	32	102

(1) Four (4) are required for AC speed monitor; thermal diode. The lower number is the number of other I/O signals that may be on the array. PLL arrays have 12 I/O positions dedicated to the PLL macro; which are not available for other signals.

* The number of I/O pads useable depends on the package.

Maximum Required Package Signal Pins

MAXIMUM PACKAGE SIGNAL PINS REQUIRED is equal to the total of all I/O signal pins, the PLL signals, the four (4) fixed pins for the thermal diode and the AC speed monitor, and all added power and grounds. Maximum package signal pins required should be used to select the packages that could be used for the array. Total package signal pins available should equal or exceed the maximum required package signal pins. (See Table 8-2.)

Actual Required Package Signal Pins

Once placement has been completed, reduce the maximum required package signal pin count by the number of added power and grounds that can be placed to use internal package power and ground planes. This is the actual number of package signal pins required.

MINIMUM REQUIRED PACKAGE SIGNAL PINS (AMCCERC supplies)	≤ ACTUAL REQUIRED PACKAGE SIGNAL PINS (Computed Value)	≤ MAXIMUM REQUIRED PACKAGE SIGNAL PINS (AMCCERC supplies)

AMCC offers an assortment of packages for the Q20000 Series Logic Arrays as shown in Table 8-2. Using the *MAXIMUM SIGNAL PINS REQUIRED* count produced by ***amccerc***, and the specific array, the matrices in Table 8-2 allow the correct package to be selected.

TABLE 8-2
AMCC Q20000 STANDARD PACKAGING MATRIX

PACKAGE	I/O SIGNAL PINS	PLL SIGNALS	FIXED I/O SIGNALS	TOTAL I/O SIGNALS	ARRAY
Leaded Chip Carriers					
68-LDCC	23	12	4	39	Q20P010
100-LDCC	66		4	70	Q20010
100-LDCC	34	12	4	50	Q20P010
100-LDCC	45	12	4	61	Q20P025
132-LDCC	92		4	96	Q20025
132-LDCC	51	12	4	67	Q20P025
196-LDCC	128		4	132	Q20045
196-LDCC	132		4	136	Q20080
Pin Grid Arrays					
100-PGA-CD	66		4	70	Q20010
149-PGA-CD	100		4	104	Q20025
209-PGA-CD	128		4	132	Q20045
251-PGA-CD	162		4	166	Q20080
301-PGA-CD	198		4	202	Q20120

I/O Signal Pins is the number of I/O signals allowed.

PLL Signals represents the 12 PLL signals allocated for the PLL macros on the PLL arrays. These pins are not available to other I/O macros.

Fixed I/O Signals is the four dedicated pins for the thermal diode and the AC Speed Monitor.

Total I/O Signals - this is the number to compare to the *maximum package signal pins required* number computed by ***amccerc***.

PACKAGE SELECTION AND AMCCANN

The package selected is used by the ***amccpackage*** program to supply package pin capacitance. Front-Annotation uses one package pin value for all package pins; Back-Annotation uses pin-specific values of capacitance, available only after placement has been completed and signed-off by the designer.

Table 8-3 is a guide to the default package pin capacitances. For further information on the operation of ***amccpackage*** or for information on the override of default values, refer to the ***AMCCPACKAGE User's Guide.*** Always check the table date and use the latest information available. For those with close tolerances, consult AMCC.

TABLE 8-3
TYPICAL RANGE OF PACKAGE PIN CAPACITANCE BY PACKAGE

PACKAGE LDCC	MIN pf	MAX** pf	Tolerance %	ARRAY
68-LDCC	2.00	4.10	±5%	Q20P010
100-LDCC	1.03	2.67	±5%	Q20P010; Q20010; Q20P025
132-LDCC	1.58	3.57	±5%	Q20025; Q20P025
196-LDCC	2.77	6.17	±5%	Q20045; Q20080
PGA				
100-PGA-CD	3.50	7.8	±5%	Q20010
149-PGA-CD	4.04	6.43	±5%	Q20025
209-PGA-CD	4.64	10.15	±5%	Q20045
251-PGA-CD	7.50	13.20	±5%	Q20080
301-PGA-CD	5.01	9.96	±5%	Q20120

** For Front-Annotation only:
MAX * (1 + tolerance)is value used to compute COM-MAX or MIL-MAX values
MAX * (1 - tolerance) is value used to compute COM-MIN or MIL-MIN values

COMPUTING THE JUNCTION TEMPERATURE

To ensure that the package and heatsink combination meets your performance requirements, the designer should compute the expected junction temperature for the product grade (military or commercial) based on the specified thermal environment so as not to exceed the maximum allowed junction temperature.

For commercial devices, the maximum junction temperature is 130°C.
For military devices, the maximum junction temperature is 150°C.

The thermal resistance between the die junction and the ambient environment depends on severall factors: die size, thermal resistance of the package, thermal resistance of the heatsink, the shape of the heatsink, ambient temperature, air flow speed and the direction of the air flow with respect to the package or heatsink fins.

• Computing Junction Temperature - Commercial Grade Devices

To compute the junction temperature for commercial grade devices, the designer needs to determine the maximum power dissipation of the die (Pd), the thermal resistance between the die and the ambient environment (Θja), and the maximum ambient temperature (Ta). The maximum junction temperature is:

$$Tj = (Pd * \Theta ja) + Ta$$

With proper thermal management, an ambient temperature Ta = 70°C can be achieved for most applications.

While the computation of Pd has already been presented in this manual (Section 5) and Ta is known, the thermal resistance Θja needs to be determined from the sum of two other thermal resistance specifications: Θjc and Θca.

Θjc is the thermal resistance between the die junction and the case (package). It is a function of die size, package construction and material thermal conductivity. Refer to Table 8-4 for Θjc of various package and device combinations.

Θca is the thermal resistance between the case (package) and the ambient environment. It is a function of the air flow and the heatsink that are used. Refer to the following pages that describe the heatsink sizes and shapes and provide tables of Θca for the heatsinks for various air flow rates.

$$\Theta ja = \Theta jc + \Theta ca$$

Compute the correct Θja to be used in the computation of the junction temperature.

• Computing Junction Temperature - Military Grade Devices

To compute the junction temperature for military devices, the designer needs to determine the maximum power disipation of the die (Pd), the thermal resistance between the die and the case (package) (Θjc), and the maximum case temperature (Tc). The maximum junction temperature is:

$$Tj = (Pd * \Theta jc) + Tc$$

The maximum case temperature Tc is taken as 125°C for most MILITARY applications.

Θjc is supplied in Table 8-4.

If the maximum junction temperature does not exceed 150°C, the designer has remained within the maximum die temperature specification of AMCC military arrays.

TABLE 8-4

AMCC Q20000 SERIES PACKAGING MATRIX ΘJC IN °C/W

PACKAGE LDCC	Q20P010 Q20010	Q20P025 Q20025	Q20045	Q20080	Q20120
68-LDCC	2.5 *				
100-LDCC	2.7	2.7 **			
132-LDCC		2.5			
196-LDCC			2.3	2.0	
PGA					
100-PGA-CD	2.2				
149-PGA-CD		2.0			
209-PGA-CD			1.8		
251-PGA-CD				1.4	
301-PGA-CD					1.2

Q20P010 Θjc same as Q20010 Θjc ; Q20P025 Θjc same as Q20025 Θjc unless otherwise noted.

* Q20P010 is available in a 68-LDCC; Q20010 is not.

** Q20P025 is available in a 100-LDCC; Q20025 is not.

PLACEMENT - SEE SECTION 7

Placement restrictions for dual-cell I/Os, added power and ground disbursement, bidirectional macros, etc. are detailed in the AMCC placement document in Section 7. If a preplacement file is being prepared for submission to AMCC, consult AMCC first for the required worksheets (array floorplan), restrictions and file formats.

Note that the Q20000 Series MSI macros are hard macros, i.e., there is only one orientation that is allowed for each.

STANDARD PACKAGES

While AMCC prefers that only AMCC-standard packages be used for the Q20000 Series, custom packages can be considered on an individual program basis. Consult your local sales representative or regional sales manager for additional details.

PLL ARRAY PACKAGES

The Q20P010 and Q20P025 PLL arrays are available in surface mount technology offering either a loop filter capacitor mounted in the package cavity, on the package or through the package pins. All packages have been custom designed by AMCC to offer controlled impedance on high speed signals and minimal digital noise injection to the PLL area. For complete details consult the ***AMCC Packaging Guide***.

Plastic Packages

AMCC is currently offering thermally enhanced plastic packages (TEP) for members of the Q20000 Array Series. For further information on these devices, consult AMCC.

Array	Package	Min	Max	Tolerance
Q20010	80-TEP	0.14 pF	0.73 pF	±5%
Q20010	68-PLCC	0.91 pF	1.00 pF	±5%
Q20010	100-PQFP	0.14 pF	0.73 pF	±5%
Q20010	100-TEP	0.14 pF	0.73 pF	±5%
Q20P010	44-PLCC	0.62 pF	0.65 pF	±5%
Q20025	100-TEP	0.14 pF	0.73 pF	±5%
Q20025	120-TEP	2.67 pF	3.48 pF	±5%
Q20025	100-PQFP	0.14 pF	0.73 pF	±5%
Q20045	160-TEP	0.24 pF	3.02pF	±5%
Q20045	208-TEP	1.55 pF	2.55 pF	±5%
Q20080	208 TEP	1.55 pF	2.55 pF	±5%

PQFP plastic quad flatpak
PLCC Plastic Leaded chip carrier
TEP thermally enhanced plactic package

Section 9
Operating Conditions

Operating Conditions

INTRODUCTION

This section documents the operating conditions used to specify the macros, how the macros are specified in Section 6 (a departure from earlier AMCC libraries) and what data extremes are to be used in design submission.

COMMERCIAL SPECIFICATION

CIRCUIT WITH A -4.5V SUPPLY: Commercial worst-case COM4 timing data are for circuits operating in the 0°C ambient to 70°C ambient temperature range with a power supply variation from -4.2V to -4.8V and a junction temperature maintained at less than or equal to 130°C.

ALL OTHER CIRCUITS: Commercial worst-case COM5 timing data are for circuits operating in the 0°C ambient to 70°C ambient temperature range, with a ± 5% power supply variation for +5V or -5.2V, and a junction temperature maintained at less than or equal to 130°C.

For a junction temperature that is greater than **130°C**, or for any other circuit specification that exceeds the commercial environment specification use the Military worst-case timing data when computing path propagation delay or set-up and hold times.

MILITARY SPECIFICATION

CIRCUIT WITH A -4.5V SUPPLY: Military worst-case MIL4 timing data are for circuits operating in the -55°C ambient to +125°C case temperature range with power supply variation from -4.5V to -4.8V and a junction temperature maintained at less than or equal to 150°C.

ALL OTHER CIRCUITS Military worst-case MIL5 timing data are for circuits operating in the -55°C ambient to +125°C case temperature range, with a ±10% power supply variation for +5V or -5.2V, and a junction temperature maintained at less than or equal to 150°C.

For a junction temperature that is greater than **150°C**, or for any other circuit specification that exceeds the military environment specification, consult AMCC.

MINIMUM PROPAGATION DELAY - LIBRARY SPECIFICATIONS

The AMCC Q20000 Macro Library is specified in Section 6 in two forms, COM5 and MIL5. Section 3 provided the adjustment factors to convert the macro specifications from COM5 to COM4 and from MIL5 to MIL4. These are repeated in Section 6 for the individual macros.

Specified: COM5, MIL5 Compute: COM4, MIL4

Each macro specification for propagation delay is given in a min/max range format (MINmin and MAXmax), as are the specifications for the k-Factors. (See Figure 9-1.) Use the min number for minimum analysis and the max number for worst-case maximum analysis. Use the adjustment factors (see Section 3) to find MINmax or MAXmin values.

Specified: **COM5MINmin/COM5MAXmax**
MIL5MINmin/MIL5MAXmax

Compute: **COM5MINmax/COM5MAXmin**
MIL5MINmax/MIL5MAXmin

The libraries are supplied on the workstations for simulation in all sixteen formats:

TABLE 9-1
MACRO LIBRARIES

MINIMUM	MAXIMUM	MINIMUM	MAXIMUM
Commercial:			
COM5MINmin	COM5MAXmin	COM4MINmin	COM4MAXmin
COM5MINmax	COM5MAXmax	COM4MINmax	COM4MAXmax
Military:			
MIL5MINmin	MIL5MAXmin	MIL4MINmin	MIL4MAXmin
MIL5MINmax	MIL5MAXmax	MIL4MINmax	MIL4MAXmax

The tables on the following pages define the operating conditions, maximum chip ratings, DC parametrics and TTL load circuits.

Figure 9-1 Commercial Libraries for COM5 Circuits

AMCC

Q20000 SERIES OPERATING CONDITIONS

RECOMMENDED OPERATING CONDITIONS - COMMERCIAL				
PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE}) V_{CC} = 0				
10K, 10KH Mode	-4.94	-5.2	-5.46	V
100K Mode	-4.2	-4.5	-4.8*	V
ECL Input Signal Rise/Fall Time	-	1.0	3.0	ns
TTL Supply Voltage (V_{CC})	4.75	5.0	5.25	V
TTL Output Current Low (I_{OL})			20	mA
Operating Temperature	0 (ambient)		70 (ambient)	°C
Junction Temperature			130	°C

ABSOLUTE MAXIMUM RATINGS	
ECL Supply Voltage V_{EE} (V_{CC} = 0)	-8.0 VDC
ECL Input Voltage (V_{CC} = 0)	GND to V_{EE}
ECL Ouput Source Current (continuous)	-50mA DC
TTL Supply Voltage V_{CC} (V_{EE} = 0)	7.0 V
TTL Input Voltage (V_{EE} = 0)	5.5 V
Operating Temperature	-55°C (ambient) to +125°C (case)
Operating Junction Temperature T_J	+150°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS - MILITARY				
PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE}) V_{CC} = 0				
10K, 10KH Mode	-4.7	-5.2	-5.7	V
100K Mode	-4.5	-4.5	-4.8*	V
ECL Input Signal Rise/Fall Time	-	1.0	3.0	ns
TTL Supply Voltage (V_{CC})	4.5	5.0	5.5	V
TTL Output Current Low (I_{OL})			20	mA
Operating Temperature	-55 (ambient)		125 (case)	°C
Junction Temperature			150	°C

* -5.7V is possible. Consult AMCC for ECL 100K DC parametrics oprating at this voltage.

ECL 10K INPUT/OUTPUT DC CHARACTERISTICS $V_{EE} = -5.2V$[1]

	$T_{ambient}$				T_{case}	UNIT
	−55°C	0°C	25°C	75°C	125°C	
V_{OHmax}[3]	$V_{CC}-850$	$V_{CC}-770$	$V_{CC}-730$	$V_{CC}-650$	$V_{CC}-575$	mV
V_{IHmax}[5]	$V_{CC}-800$	$V_{CC}-720$	$V_{CC}-680$	$V_{CC}-600$	$V_{CC}-525$	mV
V_{OHmin}[3]	$V_{CC}-1080$	$V_{CC}-1000$	$V_{CC}-980$	$V_{CC}-920$	$V_{CC}-850$	mV
V_{IHmin}[5]	$V_{CC}-1255$	$V_{CC}-1145$	$V_{CC}-1105$	$V_{CC}-1045$	$V_{CC}-1000$	mV
V_{ILmax}[5]	$V_{CC}-1510$	$V_{CC}-1490$	$V_{CC}-1475$	$V_{CC}-1450$	$V_{CC}-1400$	mV
V_{OLmax}	$V_{CC}-1655$	$V_{CC}-1625$	$V_{CC}-1620$	$V_{CC}-1585$	$V_{CC}-1545$	mV
V_{OLmin}	$V_{CC}-1980$	$V_{CC}-1980$	$V_{CC}-1980$	$V_{CC}-1980$	$V_{CC}-1980$	mV
V_{ILmin}[5]	$V_{CC}-2000$	$V_{CC}-2000$	$V_{CC}-2000$	$V_{CC}-2000$	$V_{CC}-2000$	mV
I_{IH}[2]MAX	30	30	30	30	30	μA
I_{IL}[2]MAX	−.5	−.5	−.5	−.5	−.5	μA

ECL 100K INPUT/OUTPUT DC CHARACTERISTICS $V_{EE} = -4.5V$[3]

SYMBOL	PARAMETER	TEST DC CONDITIONS	COMM 0°/+70°C			MIL −55°/+125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	Output Voltage HIGH	Loading is 50 Ohms to -2V	$V_{CC}-1035$		$V_{CC}-850$	$V_{CC}-1080$		$V_{CC}-835$	mV
V_{OL}	Output Voltage LOW	Loading is 50 Ohms to -2V	$V_{CC}-1830$		$V_{CC}-1605$	$V_{CC}-1880$		$V_{CC}-1595$	mV
V_{IHmin}[5]	Input Voltage HIGH	Maximum input voltage HIGH	$V_{CC}-1145$		$V_{CC}-800$	$V_{CC}-1145$		$V_{CC}-800$	mV
V_{ILmax}[5]	Input Voltage LOW	Maximum input voltage LOW	$V_{CC}-1950$		$V_{CC}-1475$	$V_{CC}-1950$		$V_{CC}-1475$	mV
I_{IL}[2]	Input LOW Current	$V_{IN} = V_{ILmin}$			−0.5			−0.5	μA
I_{IH}[2]	Input HIGH Current	$V_{IN} = V_{IHmax}$			30			30	μA

1 Data measured with $V_{EE} = -5.2 \pm .1V$ (or $V_{CC} = 5.0 \pm .1V$ for +5V ref. ECL 10K) assuming a +50°C rise between ambient (T_A) and junction temperature (T_J) for -55°C, 0°C, +25°C, and +70°C, and a +25°C rise for +125°C. Specifications will vary based upon T_J. See AMCC Packaging and Design Guides concerning V_{OH} and V_{OL} adjustments associated with T_J for packages and operating conditions.

2 Per fan-in.

3 Data measured at thermal equilibrium, with maximum T_J not to exceed recommended limits. See AMCC Packaging Guide to compute T_J for specific package and operating conditions. For +5V ref. ECL 100K, V_{OH} and V_{OL} specifications will vary based upon power supply. See AMCC Design Guide for adjustment factors.

4 Typical limits are at 25°C, $V_{CC} = 5.0V$.

5 These input levels provide zero noise immunity and should only be tested in a static, noise-free environment. Use extreme care in defining input levels for dynamic testing. Many outputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMCC recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for dynamic TTL testing and V_{ILMIN} and V_{IHMAX} for ECL testing.

AMCC

Q20000 SERIES ECL LOAD CIRCUITS

LOAD CIRCUIT FOR 2-STATE OUTPUTS

Figure 10

2-STATE WAVEFORM FOR INVERTING FUNCTIONS

Figure 11

2-STATE WAVEFORM FOR NON-INVERTING FUNCTIONS

Figure 12

NOTES:
1 Standard ECL load circuit used for macro specification, see Figure 10.
2 $V_M = V_{BIAS}$ to V_{LSH}.

AMCC

Q20000 SERIES TTL LOAD CIRCUITS

Figure 4

Figure 5

Figure 6

NOTES:
1 Standard TTL load circuit used for macro specification.
CL includes probe, jig and package.
2 VIN = 0 to 3.0 volts.

AMCC

Q20000 SERIES OPERATING CONDITIONS

TTL INPUT/OUTPUT DC CHARACTERISTICS

SYMBOL	PARAMETER	TEST DC CONDITIONS		COMM.0°/+70°C			MIL -55°/+125°C			UNIT
				MIN	TYP[4]	MAX	MIN	TYP[4]	MAX	
V_{IH}[5]	Input HIGH voltage	Guaranteed input HIGH voltage for all inputs		2.0			2.0			V
V_{IL}[5]	Input LOW voltage	Guaranteed input LOW voltage for all inputs				0.8			0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = −18mA			−.8	−1.2		−.8	−1.2	V
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = −1mA		2.7	3.4		2.4	3.4		V
V_{OL}	Output LoW voltage	V_{CC} = Min	I_{OL} = 4mA			0.4			0.4	V
			I_{OL} = 20mA			0.5			0.5	V
I_{OZH}	Output "off" current HIGH (3-state)	V_{CC} = Max, V_{OUT} = 2.4V		−50		50	−50		50	μA
I_{OZL}	Output "off" current LOW (3-state)	V_{CC} = Max, V_{OUT} = 0.4V		−50		50	−50		50	μA
I_{IH}	Input HIGH current	V_{CC} = Max, V_{IN} = 2.7V				50			50	μA
I_I	Input HIGH current at Max	V_{CC} = Max, V_{IN} = 5.5V				1.0			1.0	mA
I_{IL}[6]	Input LOW current	V_{CC} = Max, V_{IN} = 0.5V				−0.4			−0.4	mA
I_{OS}	Output short circuit current	V_{CC} = Max, V_{OUT} =0.5V		−25		−100	−25		−100	mA

5 These input levels provide zero noise immunity and should only be tested in a static, noise-free environment. Use extreme care in defining input levels for dynamic testing. Many outputs may be changed at once, so there will be significant noise at the device pins, and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMCC recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for dynamic TTL testing and V_{ILMAX} and V_{IHMIN} for ECL testing.

6 For standard speed options only.

Section 10
Introduction to Testing
Refer to Volume III, Section 3 for further detail

Introduction to Testing

There are three major areas of concern with respect to the testing of an array-based circuit: 1) the circuit itself must be designed to be testable; 2) the circuit itself must be designed to be reliable; and 3) the simulations must meet all conditions required for submission acceptance.

This is an overview only. The details of the simulations required and design submission in general are available in Volume III of this design manual in the *Vector Rules and Guidelines* section and in the *AMCCVRC* and *AMCCSUBMIT User's Guides.*

CIRCUIT TESTABILITY

Concepts of testing and testability must be considered from the beginning of any circuit design. AMCC encourages: 1) the use of testability techniques in circuit design; 2) the use of testability analysis early in the design process so that testability problems can be corrected by design; 3) the use of fault grading to assess test vector fault coverage; and 4) an understanding of the capabilities of today's advanced test equipment in the development of semi-custom circuits.

STRUCTURED DESIGN FOR TEST [DFT]

Structured approaches to ensure circuit testability such as LSSD, Scan Path and BILBO are generally driven by an overall system philosophy to testing. While AMCC does not promote one structured technique over another, design for test (DFT) methodologies can significantly improve circuit testability. AMCC strongly recommends the use of overall structured design procedures, including functional modularity, bus architectures and clear documentation.

CIRCUIT TESTABILITY ANALYSIS

All testability measures have one common goal: to enhance controllability and observability of the circuit. It is a grade on the logic design itself. Controllability is a measure of the ease in setting a particular node to a logic state level of zero or one, while observability determines the ease of propagating the state to one or more primary outputs.

After a netlist has been created and logic simulation has verified correct functional performance, testability can be verified by running testability analysis programs if they are available to the designer. (Testability analysis programs are currently not supported by AMCC.)

CIRCUIT SIMULATION REQUIREMENTS

AMCC design submission requirements include the simulation of the circuit for both the maximum MIL5, MIL4, COM5 or COM4, for an evaluation of maximum worst-case delay, and the minimum MIL5, MIL4, COM5 or COM4 for an evaluation of minimum worst-case delay, for functional, at-speed, AC test and parametric simulations.

The four types of simulations with format (**SAM** = sampled, **POC** = print on change) and conditions (MINIMUM, MAXIMUM) are:

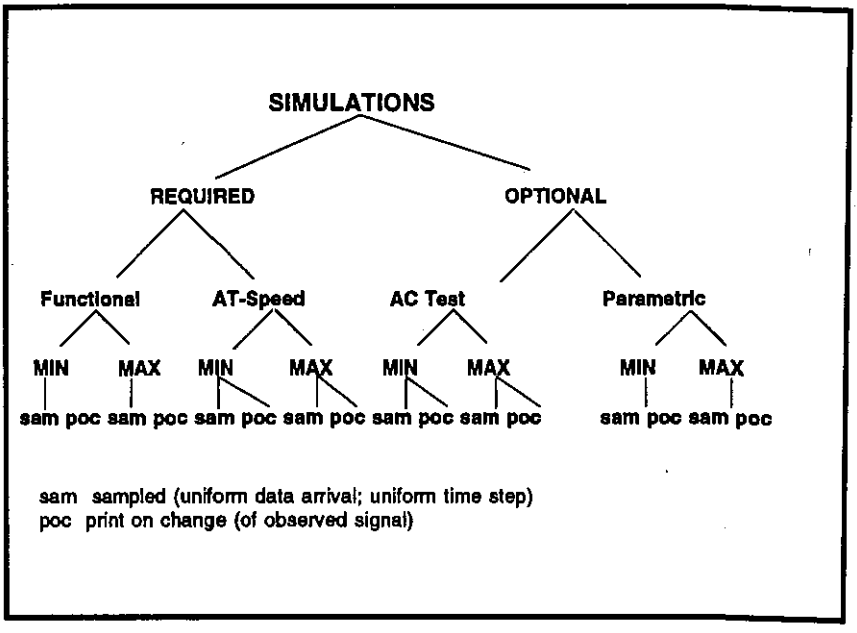


Figure 10-1 Circuit Simulation Requirements

No timing verifier available
AC tests are optional; parametric tests may be optional
MAX is COM4MAXmax, COM5MAXmax, MIL5MAXmax or MIL4MAXmax
MIN is COM4MINmin, COM5MINmin, MIL5MINmin or MIL4MINmin
Parametric Tests may be optional or required depending on vector SSOs

It is up to the designer to provide simulation vectors and the control files used to generate them that will exercise the correct worst-case conditions for the macros in the critical path.

FUNCTIONAL SIMULATION - REQUIRED

The object of functional testing is to detect a single SA1 (stuck-at-1) or SA0 (stuck-at-0) fault in the circuit if one exists. This ideally requires sufficient vectors to "cover" all possible SA1 and SA0 fault locations. The percent of coverage is the fault grade of the vector set.

Functional test vectors are created from the functional simulation sampled results file, containing input and expected output for that input.

The functional vector set for a circuit should detect any single fault occurring on a single path. In theory, triple faults, quintuplet faults (odd-numbered sets of faults) per path are covered by the vectors detecting single faults provided the faults do not mask each other. Even-numbered sets of faults on a path (double faults, quad faults, etc.) are assumed to mask each other and to not be detectable. The probability of multiple faults on a path is significantly less than the probability of a single fault. (Multiple faults that signal a catastrophic failure are detected within the AMCC screening.)

One extreme approach used to develop functional vectors is to cycle all inputs and outputs through 1-0 and 0-1 transitions as a first check after initialization. (Theoretically, in a combinational circuit, this should cycle all internal nodes as well.) This 2^n (where n = number of inputs) brute force approach is not necessary.

Minimum vector test sets and minimum vector test sequences will cover 100% of all observable faults. A fault cannot be detected by any test methodology if it is a masked fault. A masked fault cannot be seen at a primary output due to redundancy in the logic. Logic minimization is therefore a requirement if high fault grade scores are desired. Deliberate redundancy in a circuit will require added test points.

Guidelines

For guidelines in performing functional simulation, refer to *Vector Submission Rules and Guidelines* in Volume III.

Hazards, Races

If there is a difference in the functional simulation results between the maximum and the minimum timing library values, hazard and race conditions are indicated and must be evaluated. As an additional vector check, AMCC will screen test vectors through **LASAR 6** for race and hazard conditions beyond what can be detected with an EWS simulator. Consult AMCC for Lasar 6 availability for your system.

AMCC strongly recommends the use of ***RaceCheck*** for race and hazard analysis. Consult AMCC for availablbility on your system.

amccvrc

amccvrc (AMCC Vector Rules Checker) must be run against any ***amccsimfmt*** (AMCC Simulation Format) worst-case-maximum sampled simulation output file. ***amccvrc*** will issue a count of the number of test vectors and simulation vectors per file. A warning is issued after 16K vectors. Refer to *Vector Rules and Guidelines* in the design manual and to the *amccvrc User's Guide.*

Consult your account representative if you have functional vector files that total in excess of 4K vectors for arrays of up to 120 signal pads; in excess of 16K for arrays of 120 signal pads and over.

Fault-Grading

Functional simulation vector fault-grading can be performed using the LASAR 6 simulator. Fault-grading is used to verify that the functional simulation vectors sufficiently exercise nodes within the circuit to assure that the outgoing product matches the customer specification.

Insufficient fault coverage as determined in a fault grading run may require the addition of vectors to the set developed to evaluate logical functionality.

AMCC recommends the creation of a sufficient number of vectors to achieve a fault coverage of 90% or higher, and is prepared to perform the fault grading task upon request. Indications from recent research are that using stuck-at testing will not cover all fault conditions but that a high fault-grade score of 99% or better will raise the overall outgoing quality level of the device.

AT-SPEED SIMULATION - REQUIRED

In addition to functional simulation, the customer must perform an at-speed simulation and timing analysis for all critical (i.e., timing-sensitive) paths in the circuit. At-speed simulations for submission must be done using worst-case MIL5, MIL4, COM4 or COM5MAXmax for maximum timing; and the corresponding MINmin for minimum timing. The simulation is run at the maximum frequency of operation.

At-Speed simulations are submitted in sampled and print-on-change format. Note that it is not sufficient to simply "speed-up" the functional vectors.

Only ***amccsimfmt***ed simulation output files are submitted, along with the control and stimulus files. Refer to Volume III for format and sampling rules for at-speed vectors. ***amccvrc*** is not run against the at-speed vectors.

AC SPEED MONITOR

Each array in the Q20000 Turbo Series contains, as standard, a structure known as the AC Speed Monitor (see Section 2). This structure resides "off chip" between bonding pads and the scribe line. By applying a negative supply voltage to its independent power pin, this monitor will provide a frequency output which can be used as a measure of AC performance.

This may be considered as an alternative to AC testing. Consult AMCC.

AC TESTS SIMULATION - OPTIONAL

The designer may wish to specify AC tests.

AC path propagation delay tests require simulation vectors to initialize the circuit path to be measured and to support the measurements of the path. All AC tests may be grouped in one simulation control and stimulus file (EWS-dependent).

AC test simulations must be done using MIL5, MIL4, COM4 or COM5 MAX for maximum timing and the corresponding MIN for minimum timing. Sampled and print-on-change simulations must be performed.

If there is a difference in the AC test simulation results between the maximum and the minimum timing, (sampled files only), hazard and race conditions are indicated and must be evaluated.

amccvrc and ***amccsubmit***

amccvrc must be used to screen the amccsimfmted sampled worst-case maximum AC test simulation output files.

amccsubmit must be used to submit AC test simulations to AMCC. It is designed to prompt the designer via menus for the required information. Follow the directions in Volume III. ***amccsubmit*** will check for paths that are less than *5ns* and for circuit specifications too close to Front Annotation results.

Refer to Volume III, Section 3 for further information on AC tests.

amccsubmit will be used after its release. It incorporates ***amcctest*** as part of its functional capability. ***amcctest*** is no longer supported.

PARAMETRIC TESTING - OPTIONAL - MAY BE REQUIRED

Parametric testing for VIH, VIL is optional if the vector SSO limit is within the 8/16 limits (no more than eight (8) outputs of type TTL or ECL change in a vector for a mixed mode circuit; no more than 16 of either for a homogeneous circuit). They can be realized in several different ways.

Parametric simulations must be done using MIL5, MIL4, COM4 or COM5 MAX for maximum timing and the corresponding MIN for minimum timing. Only sampled simulations must be performed.

For vector sets with vector SSOs greater than the 8/16 limit but not exceeding the 16/32 limit, parametric vectors are required. (Vectors with more than 32 outputs changing are in error.)

If a parametric gate tree is used (the approach AMCC recommends), the output gate must be parameterized with the GTO gate-tree-output parameter/property. The GTO parameter is used by amccvrc.

Run parametric simulations using the worst-case maximum and worst-case minimum libraries.

amccvrc

The ***amccsimfmt***ed simulation maximum worst-case sampled output file will be run against the ***amccvrc*** parametric vector checker.

Refer to Volume III, Section 3 for information on the requirements for parametric testing.

AMCCSUBMIT

amccsubmit must be used to submit simulations to AMCC. It is designed to prompt the designer via menus for required validation and submission information. Follow the directions in Volume III, the *AMCCSUBMIT User's Guide*..

CIRCUIT DESIGN FOR TESTABILITY

Some specific design suggestions for improved circuit testability are:

- **Become familiar with the macro library *before* beginning the macro conversion or design.**
- **Use synchronous** rather than asynchronous circuits whenever possible. Functional tests are synchronous.
- Partition the design (**use structured design techniques**) into smaller, testable sections, usually along a functional boundary.
  - Use **degating logic** to isolate modules for test.
  - Use **modular architecture**, bus structures.
  - **Break up long counters** (>8).
- **Don't bury states.**
- **Use transparent latches** instead of flip/flops where possible.
- **Use macros,** especially flips/flops and latches, **with RESET or SET controls** where possible to simplify initialization.
- **Avoid feedback loops.** If unavoidable, provide a means to break up feedback loops during test (degating, enables).
- **Avoid redundant logic** - minimize! - or add test points to unmask masked faults.
- **Avoid derived clocks** - they complicate testing.
- **Design in test points,** especially in sequential logic. Add test points to improve controllability and observability. Perform testability analysis.
- If I/O pins are limited, use demultiplexors to control and multiplexors to observe internal nodes with otherwise poor observability (buried states).

- Any **3-state enable control** signal that is internally generated must be externally observable, and **should be externally controllable during test.**

- **Add parity trees** for error detection. Or **use Scan Path Design** to simplify test sequence generation or **use Level Sensitive Scan Design** to simplify test sequence generation. Keep test generation in mind while designing the circuit.

CIRCUIT DESIGN FOR RELIABILITY

Some specific design suggestions for improved circuit reliability are:

- **Become familiar with the macro library before beginning the macro conversion or design.**

- Be aware of "glitch" circuits. **Do not use potential glitch circuits to drive clock inputs.**

- **Avoid one-shot pulse generators.** They complicate testing. Consult AMCC prior to designing a one-shot or pulse generation circuit. See Figure 10-2.

- **Avoid gated and derived clocks.**

- **Avoid race and hazard conditions.** (***RaceCheck*** can help identify these.) Races and hazards are generated by having a signal follow two or more paths to a common circuit element (a.k.a. reconvergent fan-out.)

- **Avoid feedback loops.** If unavoidable, provide a means to break up feedback loops during test (using degating, enables).

- **Avoid feedback paths between registers.** If present, compute the worst-case set-up and hold times and verify operation.

- **Add sufficient IEVCC** for the number of simultaneously switching outputs and distribute among these outputs (similar to distributed ground in a ribbon cable). Add additional extra IEVCC if there are extra I/O pins available. **ITPWR and ITGND** are also available.

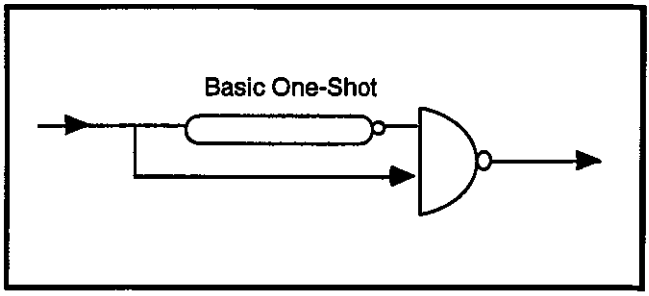


Figure 10-2 A basic One-Shot Circuit. AMCC requires that all paths be controllable and observable. This circuit complicates testing and part verification. Consult AMCC before use.

- **Properly derate fan-out on all distortion-sensitive paths and all clock paths.** Keep clock path loading balanced.

- **Avoid floating nodes on internal 3-state busses or external bidirectional busses.**

- **Use Johnson counters or separate flip/flops to decode terminal counts.** The loading on the Q outputs is identical, eliminating the loading skew (not the metal skew), and the outputs are a Gray code - only one output changes state per clock cycle. (Binary counter decoding can cause glitches.)

- **Compensate for rising and falling edge loading skews** and the reversed TTL input translator rising and falling edge skews by inversion **as needed to reduce pulse stretch and pulse shrink phenomena.**

POWER BUS DISTRIBUTION AND DECOUPLING

The optimal Power Bus Distribution and Decoupling is dependent on a number of interactive device and system variables, including the package design used, the number of simultaneous switching outputs on the device, output loading, the amount of switching noise contributed by other system components, the number of power busses and the design of the system and module power distribution.

AMCC recommends the use of multi-layer PC boards that provide dedicated low impedance power and ground planes. Besides maintaining a constant characteristic impedance for transmission lines, the planes provide for a low impedance return path to the ECL or TTL circuitry and act as an electromagnetic shield for the signal lines. The distributed capacitance will also improve noise margins by minimizing "ground bounce" and crosstalk.

Two-layer PC boards, on the other hand, may require successive approximations to optimize the system noise margins and reduce external noise from being fed back into the chip through the power and ground pins. This approach should only be attempted in lower performance systems.

I/O ECL VCC and Internal VCC package pins should be tied together as close to the chip as possible, using good high frequency practices. When mixed I/O is combined with multiple power busses, the TTL GND and ECL VCC (0V) can be tied directly together at the chip on multi-layer boards.

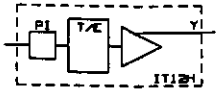
For 2-sided boards, the location will be system dependent and may require some experimentation. The primary considerations are the amount of simultaneous switching, the signal/ground pin ratio and the isolation between the TTL and ECL signal lines (and return paths).

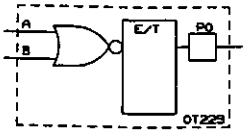
Low frequency (bulk) decoupling is generally provided in the range of 0.5 to 2.0 µf/WATT, while high frequency by-passing should be 100 to 1,000 pF/quadrant. The by-pass capacitors are generally placed as close to the chip as possible using high frequency techniques to minimize the inductance in the leads, traces, feed-throughs and components.

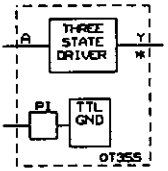
The AMCC Q20000 performance boards use a 1 µf tantalum capacitor in parallel with a 470pf ceramic chip capacitor for each of the Internal VEE/VCC pairs. This same combination is used for any VCC or additional VCC package pins with excellent results.

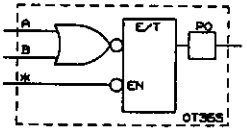
Section 11
Quicksheets

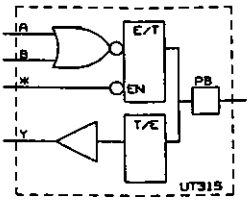
TTL I/O

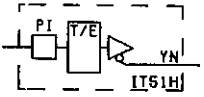


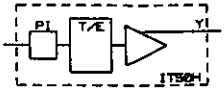












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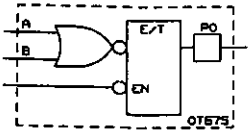

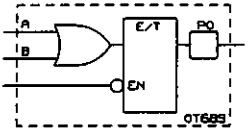

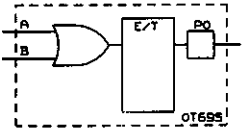

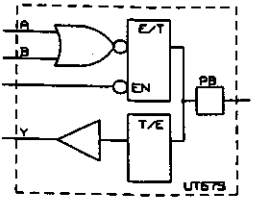

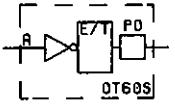

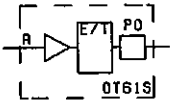

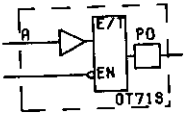

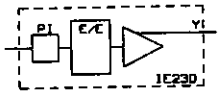
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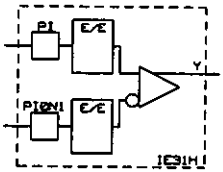
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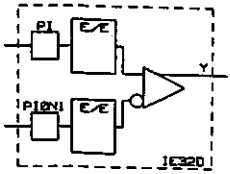
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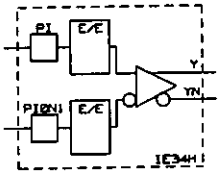
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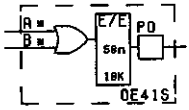
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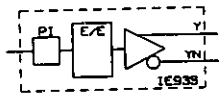
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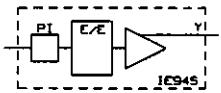
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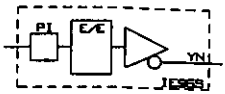
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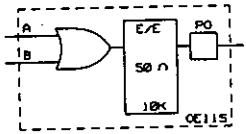
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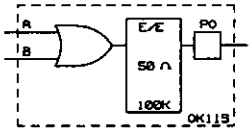
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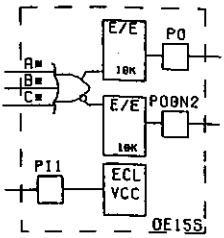
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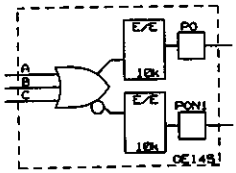
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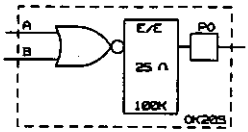
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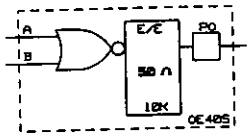
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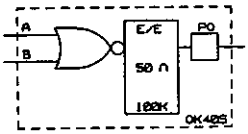
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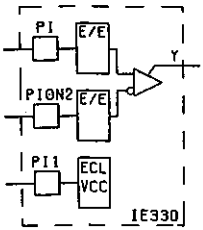
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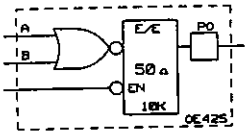
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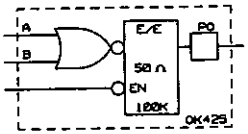
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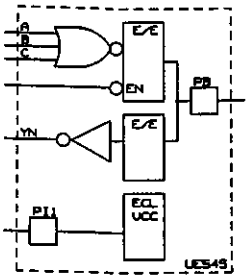
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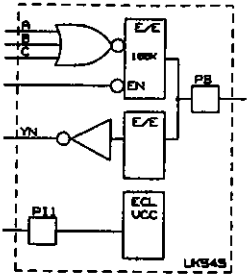
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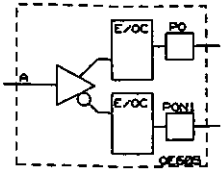
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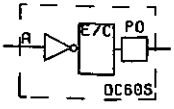
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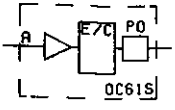
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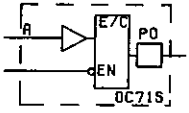
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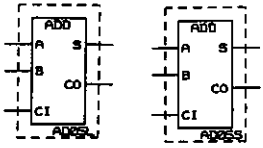

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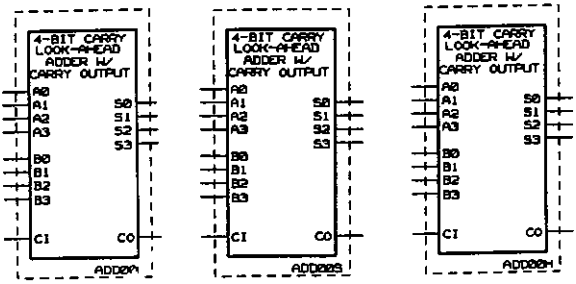
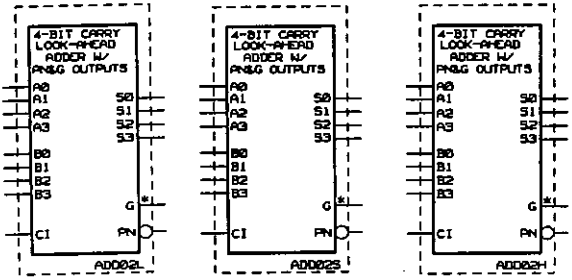
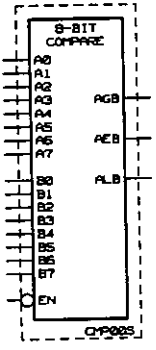
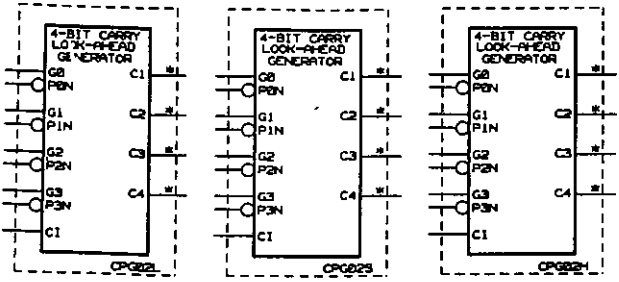






COMPARATOR

CARRY-LOOK-AHEAD



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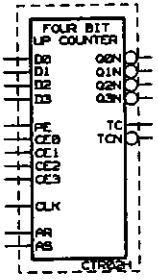

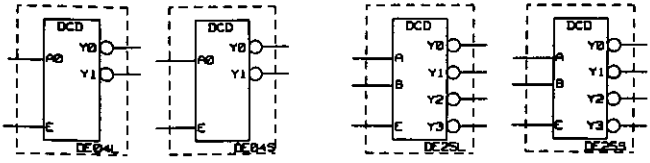

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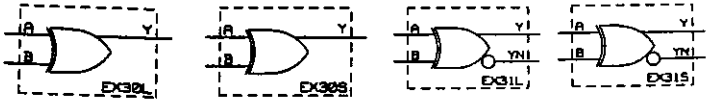

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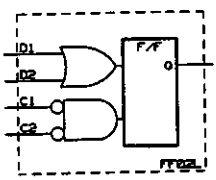
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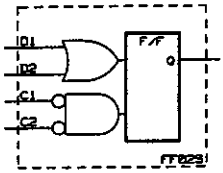
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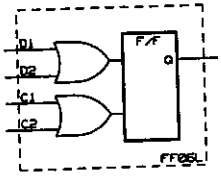
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D2
C1
C2
F/F
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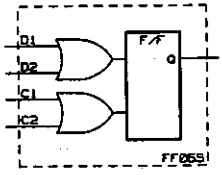
FF05L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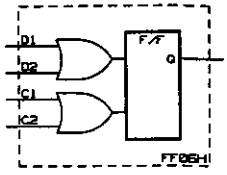
C1
C2
F/F
Q
FF05S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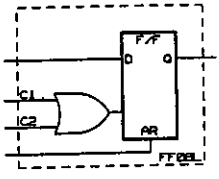
C1
C2
F/F
Q
FF05H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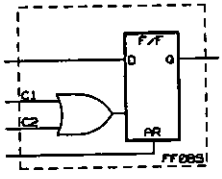
C2
F/F
Q
AR
FF08L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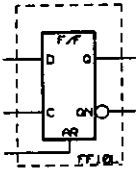
C1
C2
F/F
Q
AR
FF08S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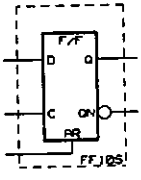
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F/F
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QN
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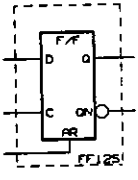
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F/F
Q
QN
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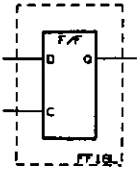
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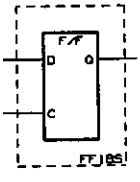
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C
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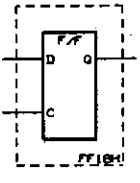
FFJ1S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C
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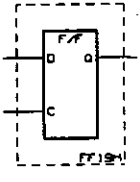
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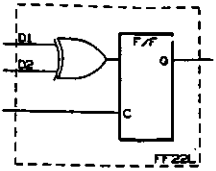
C
F/F
Q
FFJ1H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D2
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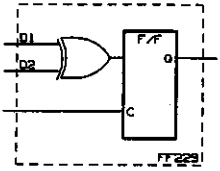
Q
C
FF22L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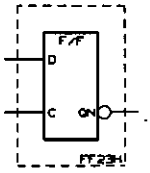
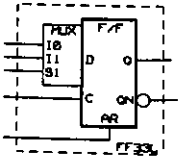
D2
F/F
Q
C
FF22S


F/F
D
C
QN
FF23H


MUX
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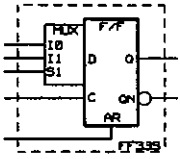
S1
F/F
D
Q
C
QN
AR
FF33L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S1
F/F
D
Q
C
QN
AR
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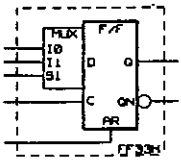
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S1
F/F
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C
QN
AR
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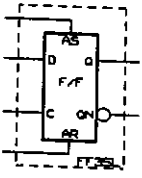
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C
QN
AR
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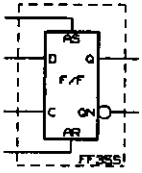
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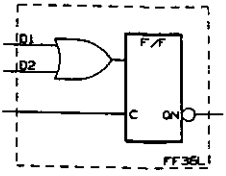
D
Q
F/F
C
QN
AR
FF35S

FLIP/FLOPS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F/F
C
QN
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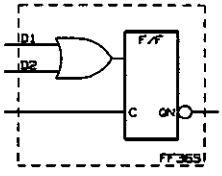
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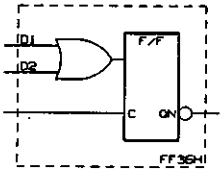
D2
F/F
C
QN
FF36S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D2
F/F
C
QN
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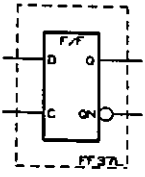
F/F
D
Q
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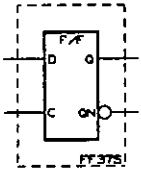
F/F
D
Q
C
QN
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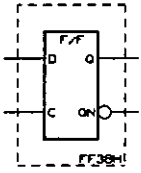
F/F
D
Q
C
QN
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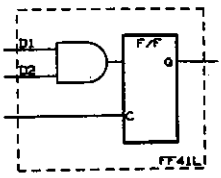
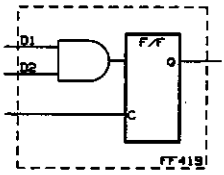
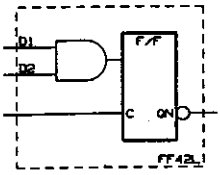

D1
D2
F/F
Q
C
FF41L


D1
D2
F/F
Q
C
FF41S

FLIP/FLOPS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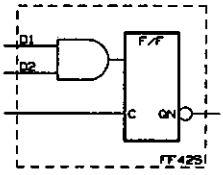
D2
F/F
C
QN
FF42L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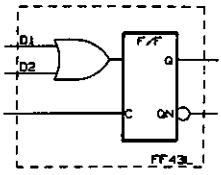
D2
F/F
C
QN
FF42S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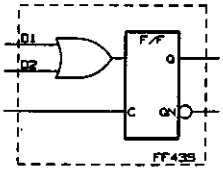
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D2
F/F
Q
C
QN
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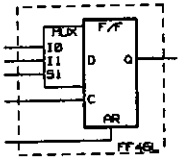
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S1
F/F
D
Q
C
AR
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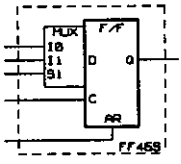
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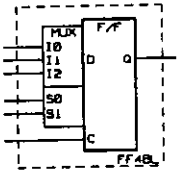
I1
S1
F/F
D
Q
C
AR
FF46S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S0
S1
F/F
D
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C
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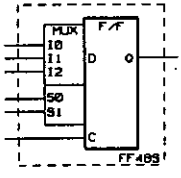
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S1
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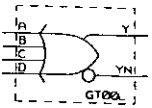
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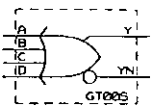
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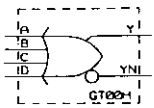
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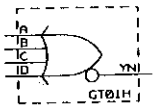
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D
YN
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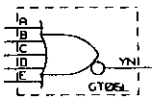
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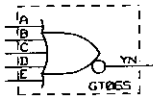
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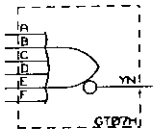
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E
F
YN
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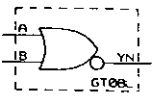
GATES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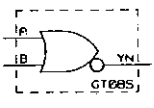
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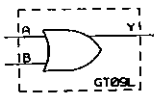
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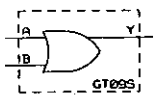
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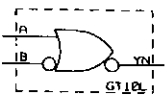
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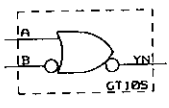
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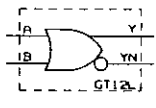
YN
GT10S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YN
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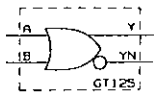
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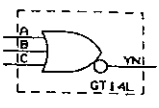
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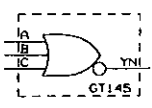
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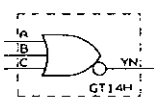
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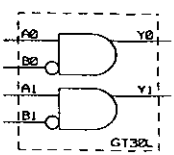
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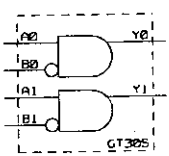
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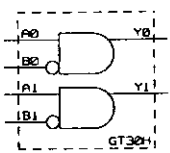
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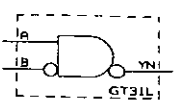
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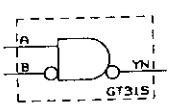
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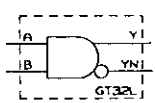
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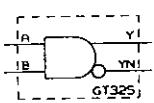
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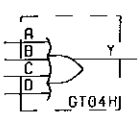
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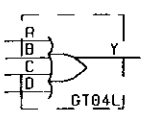
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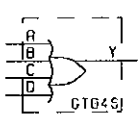
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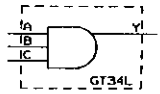
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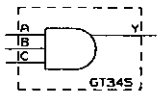
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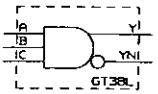
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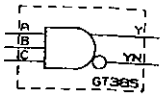
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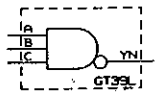
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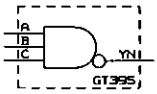
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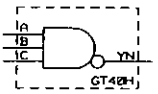
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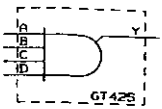
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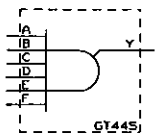
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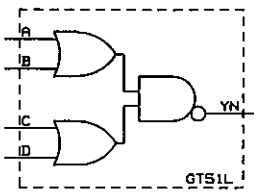
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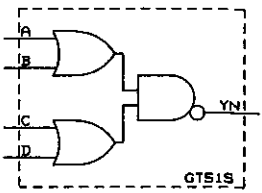
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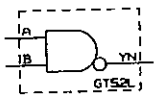
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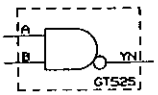
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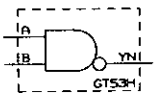
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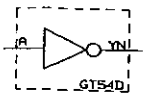
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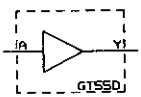
GATES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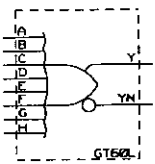
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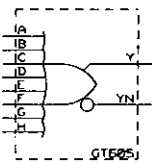
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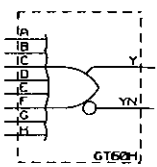
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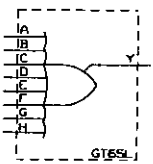
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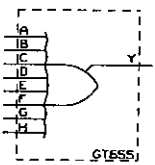
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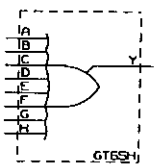
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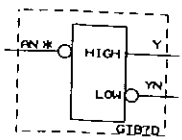
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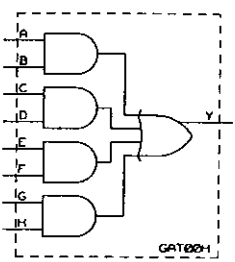
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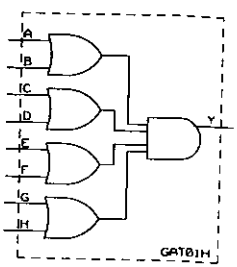
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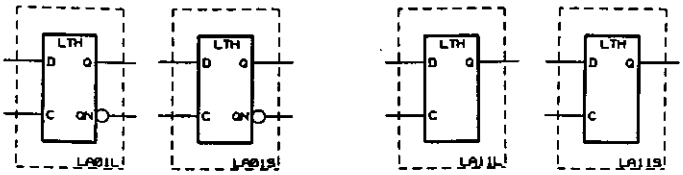
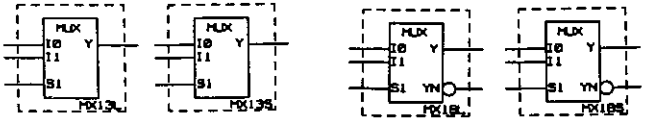
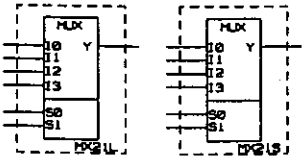
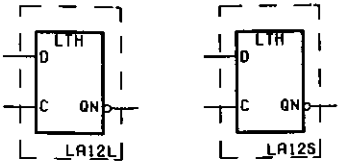


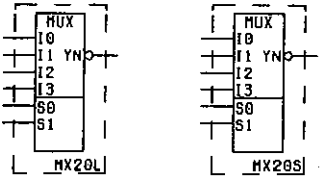
LATCHES

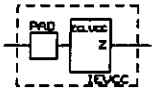




MULTIPLEXORS



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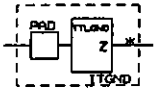
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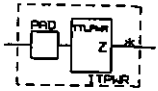
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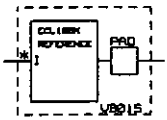
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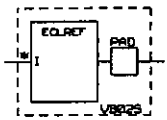
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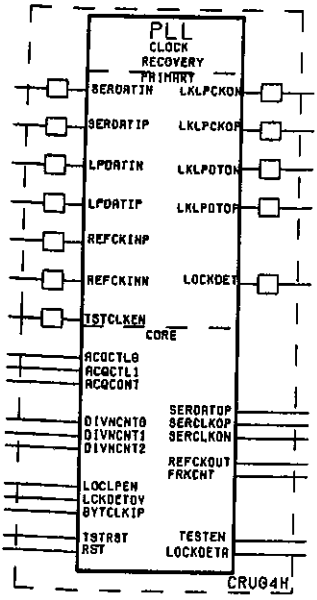
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REFCKINN
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CORE
ACQCTL0
ACQCTL1
ACQCONT
DIVNCNT0
DIVNCNT1
DIVNCNT2
LOCLPEN
LCKDETOV
BYTCLKIP
TSTRST
RST
LKLPCKON
LKLPCKOP
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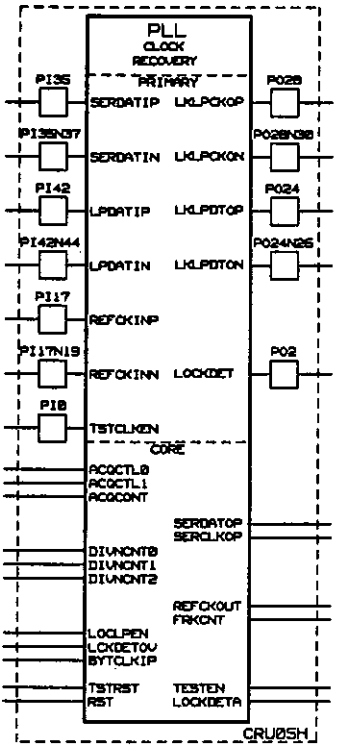
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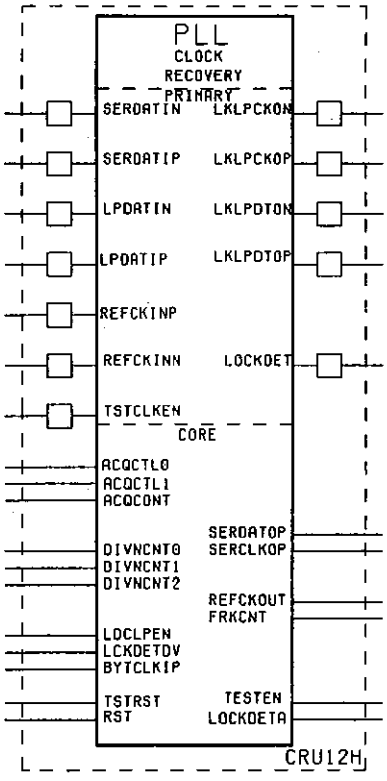
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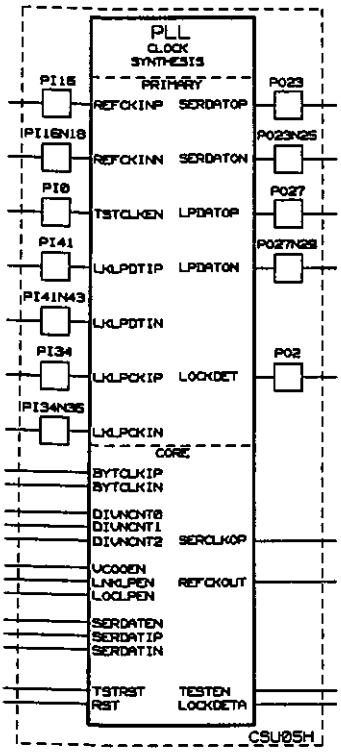
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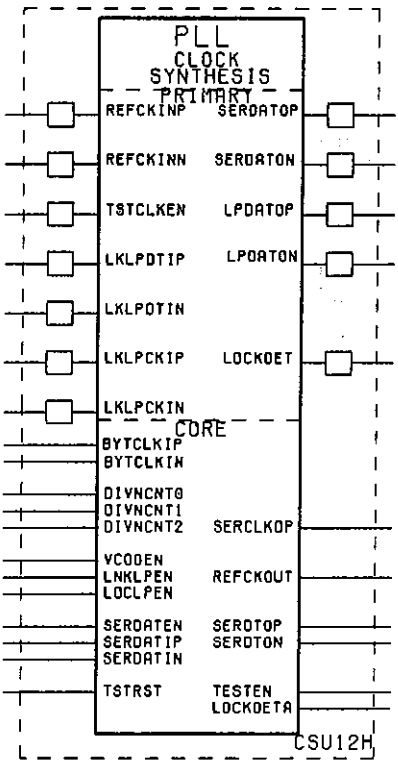
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