AMCC
APPLIED MICRO CIRCUITS CORPORATION

Application Note 8
External Set Up and Hold Time Bipolar Arrays

CHAP 12 - APPLICATION NOTE 8
EXTERNAL SET UP AND HOLD TIME, BIPOLAR ARRAYS

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EXTERNAL SET-UP and HOLD TIMES - 100% ECL

The basic external set-up and hold time equations for an ECL-only circuit are outlined below. Asynchronous T_{PLH} and T_{PHL} skews must also be taken into account by computing set-up and hold time for both rising and falling edges.

$$T_{su(external)} = [SU + (M-1) * |SU|] + T_{su(macro)} + (T_{DM} - T_{CM})$$

$$T_{h(external)} = [HL + (M-1) * |HL|] + T_{h(macro)} + (T_{DM} - T_{CM})$$

Where:

T_D = data path propagation delay from the circuit input and up to the memory macro data input pin

T_C = clock path propagation delay from the circuit input and up to the memory macro clock input pin

$SU = (1.1\ T_D - 0.9\ T_C)$

$HL = (1.1\ T_C - 0.9\ T_D)$

M = commercial grade or military grade multiplier (refer to the multiplication factor table)

T_{DM} = interconnect wire length <u>in excess of</u> 100mils/net in the data path

T_{CM} = interconnect wire length <u>in excess of</u> 100mils/net in the clock path

$T_{su(macro)}$ = Tsu as specified in Design Guide (SPEC = MIN)

$T_{h(macro)}$ = Th as specified in Design Guide (SPEC = MIN)

FIGURE 1

EXTERNAL SET-UP AND HOLD FOR ECL ONLY CIRCUIT

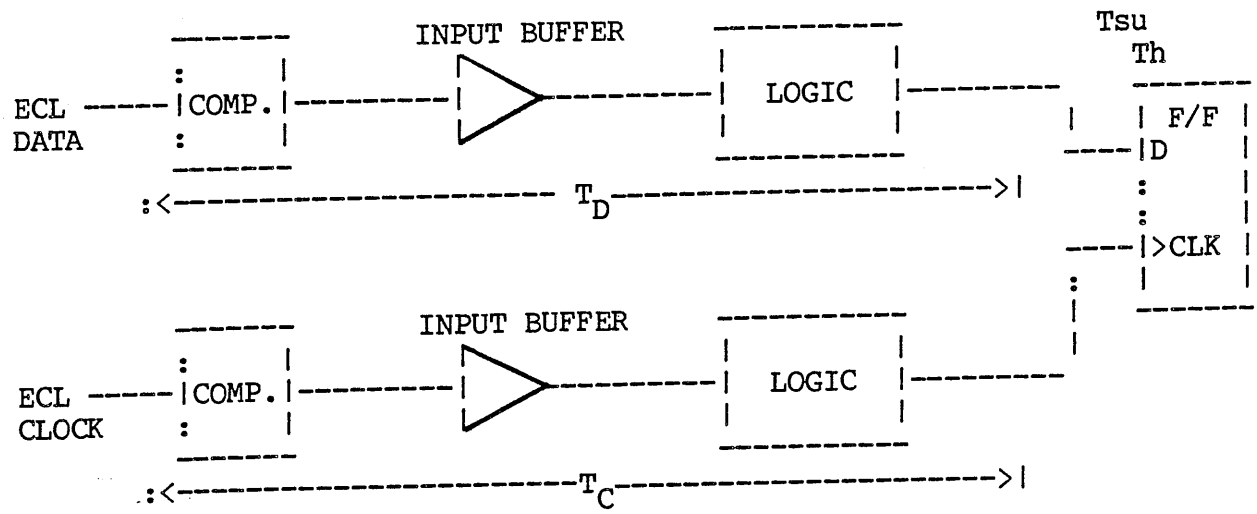
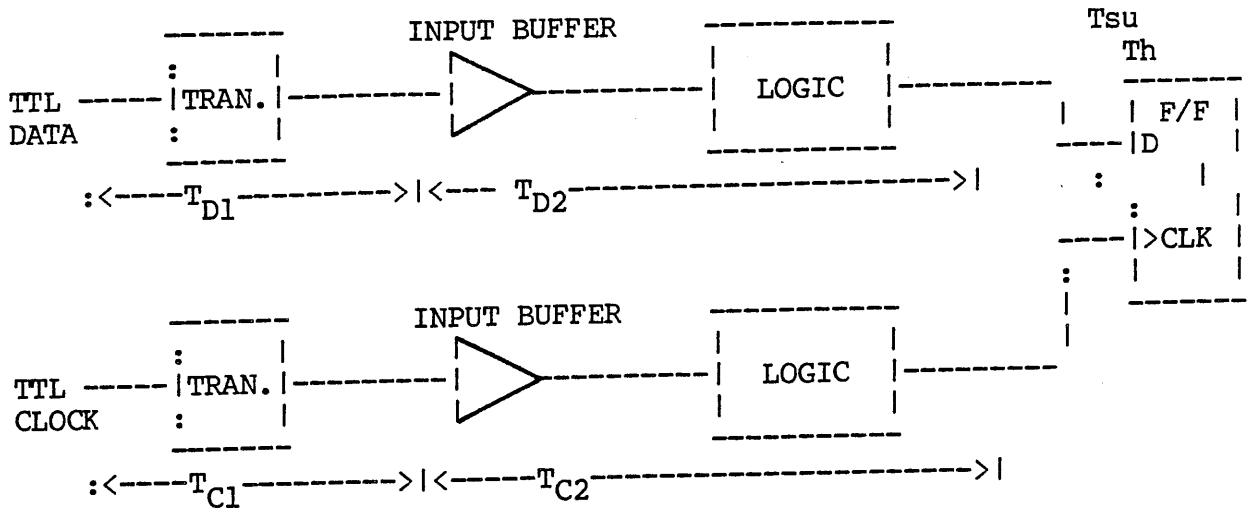


FIGURE 2

EXTERNAL SET-UP AND HOLD FOR TTL ONLY CIRCUIT



EXTERNAL SET-UP and HOLD TIMES - 100% TTL

The basic external set-up and hold time equations for a TTL-only circuit are outlined below. Asynchronous T_{PLH} and T_{PHL} skews must also be taken into account by computing set-up and hold time for both rising and falling edges.

$$T_{su(external)} = [SU1 + (M1-1) * |SU1|] + [SU2 + (M2-1) * |SU2|] + T_{su(macro)} + (T_{DM} - T_{CM})$$

$$T_{h(external)} = [HL1 + (M1-1) * |HL1|] + [HL2 + (M2-1) * |HL2|] + T_{h(macro)} + (T_{DM} - T_{CM})$$

Where:

T_{D2} = data path propagation delay from the circuit input and up to the memory macro data input pin; exclude the TTL input translator delay

T_{C2} = clock path propagation delay from the circuit input and up to the memory macro clock input pin; exclude the TTL input translator delay

T_{D1} = data path propagation delay from the TTL input translator

T_{C1} = clock path propagation delay from the TTL input translator

$SU1 = (1.1\ T_{D1} - 0.9\ T_{C1})$

$HL1 = (1.1\ T_{C1} - 0.9\ T_{D1})$

$SU2 = (1.1\ T_{D2} - 0.9\ T_{C2})$

$HL2 = (1.1\ T_{C2} - 0.9\ T_{D2})$

M1 = commercial grade or military grade multiplier - TTL inputs only

M2 = multiplier for internal delays
(refer to the multiplication factor table)

T_{DM} = interconnect wire length in excess of 100mils/net in the data path

T_{CM} = interconnect wire length in excess of 100mils/net in the clock path

$T_{su(macro)}$ = Tsu as specified in Design Guide (specified as minimum)

$T_{h(macro)}$ = Th as specified in Design Guide (specified as minimum)

EXTERNAL SET-UP and HOLD TIMES - ECL DATA AND TTL CLOCK

The basic external set-up and hold time equations for an ECL-DATA and TTL-CLOCK circuit are outlined below. Asynchronous T_{PLH} and T_{PHL} skews must also be taken into account by computing set-up and hold time for both rising and falling edges.

$$T_{su(external)} = [SU + (M2-1) * |SU|] + T_{su(macro)} + (T_{DM} - T_{CM})$$

$$T_{h(external)} = [M1 * T_{C_{translator}}] + [HL + (M2-1) * |HL|] + T_{h(macro)} + (T_{DM} - T_{CM})$$

Where:

T_D = data path propagation delay from the circuit input and up to the memory macro data input pin

T_C = clock path propagation delay from the circuit input and up to the memory macro clock input pin; excluding input translator delay

$T_{C_{translator}}$ = clock path delay due to input translator

SU = $(1.1\ T_D - 0.9\ T_C)$

HL = $(1.1\ T_C - 0.9\ T_D)$

M1 = commercial grade or military grade multiplier - TTL inputs only

M2 = multiplier for internal delays (refer to the multiplication factor table)

T_{DM} = interconnect wire length <u>in excess of</u> 100mils/net in the data path

T_{CM} = interconnect wire length <u>in excess of</u> 100mils/net in the clock path

$T_{su(macro)}$ = Tsu as specified in Design Guide (SPEC = MIN)

$T_{h(macro)}$ = Th as specified in Design Guide (SPEC = MIN)

EXTERNAL SET-UP and HOLD TIMES - TTL DATA AND ECL CLOCK

The basic external set-up and hold time equations for a TTL-DATA and ECL-CLOCK circuit are outlined below. Asynchronous T_{PLH} and T_{PHL} skews must also be taken into account by computing set-up and hold time for both rising and falling edges.

$$T_{su(external)} = [M1 * T_{D_{translator}}] + [SU + (M2-1) * |SU|] + T_{su(macro)} + (T_{DM} - T_{CM})$$

$$T_{h(external)} = [(M1-1) * T_{D_{translator}}] + [HL + (M2-1) * |HL|] + T_{h(macro)} + (T_{DM} - T_{CM})$$

Where:

T_D = data path propagation delay from the circuit input and up to the memory macro data input pin; excluding the TTL input translator delay

$T_{D_{translator}}$ = data path delay due to TTL input translator

T_C = clock path propagation delay from the circuit input and up to the memory macro clock input pin

$SU = (1.1\ T_D - 0.9\ T_C)$

$HL = (1.1\ T_C - 0.9\ T_D)$

M1 = commercial grade or military grade multiplier - TTL inputs only

M2 = multiplier for internal delays (refer to the multiplication factor table)

T_{DM} = interconnect wire length <u>in excess of</u> 100mils/net in the data path

T_{CM} = interconnect wire length <u>in excess of</u> 100mils/net in the clock path

$T_{su(macro)}$ = Tsu as specified in Design Guide (SPEC = MIN)

$T_{h(macro)}$ = Th as specified in Design Guide (SPEC = MIN)

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TABLE 10
TYPICAL LOADING DELAY DELTA Tpd

MACRO TYPE	RISE/FALL DELTA Tpd
S OPTION	0.05/0.10 ns/load
H OPTION	0.05/0.10 ns/load
P OPTION	0.05/0.10 ns/load
DRIVERS	0.05/0.10 ns/load

TABLE 11
TYPICAL WIRE-OR DELAY DELTA Tpd

NET SIZE	RISE/FALL DELTA Tpd
WIREOR2	0.05/0.1 ns
WIREOR3	0.10/0.2 ns
WIREOR4	0.15/0.3 ns

TABLE 12
WORST-CASE DELAY MULTIPLICATION FACTORS

1.5 --- For COMMERCIAL applications
(ALL BUT TTL INPUT MACROS)
0°C to 70°C, ±5% power supplies

2.0 --- FOR TTL INPUTS - COMMERCIAL APPLICATIONS

1.6 --- For MILITARY applications
(ALL BUT TTL INPUT MACROS)
-55°C ambient to +125°C case
±10% power supplies

2.5 --- FOR TTL INPUTS - MILITARY APPLICATIONS

TABLE 13
TYPICAL METAL DELAYS

First metal	7ps/mil
Second metal	4ps/mil

TABLE 9
TYPICAL LOADING DELAY DELTA Tpd

MACRO TYPE	RISE/FALL DELTA Tpd
S OPTION	0.03/0.05 ns/load
H OPTION	0.03/0.05 ns/load
L OPTION	0.03/0.10 ns/load
15-Load DRIVERS	0.03/0.03 ns/load

TABLE 10
TYPICAL WIRE-OR DELAY DELTA Tpd

NET SIZE	RISE/FALL DELTA Tpd
WIREOR2	0.10/0.05 ns
WIREOR3	0.20/0.05 ns
WIREOR4	0.30/0.05 ns

TABLE 11
WORST-CASE DELAY MULTIPLICATION FACTORS

1.5	--- For COMMERCIAL applications * $0^{o}C$ to $70^{o}C$, $\pm 5\%$ power supplies
1.6	--- For MILITARY applications ** $-55^{o}C$ ambient to $+125^{o}C$ case $\pm 10\%$ power supplies

* $T_j \leq 130^{o}C$

** $T_j \leq 150^{o}C$