AMCC
APPLIED MICRO CIRCUITS CORPORATION

High Performance Logic Array Design

Bipolar

THIRD EDITION

JANUARY 1985

A M C C
APPLIED MICRO CIRCUITS CORPORATION

INTRODUCTION

CHAP 1 - INTRODUCTION
Course Objectives
Where AMCC arrays fit
- Silicon Compiler
- Full Custom
- Logic Arrays

Summary of array advantages over other methods of design
Interconnect - as defined for AMCC arrays
Cell- defined
- Logic cell for the Q700
- Logic cell for the Q1500
- Logic Cell for the Q3500

Feasibility Study - what to evaluate
Technology
- Q700, Q1500 diffusion/junction-isolated 5 micron
- Q3500 oxide-isolated 3 micron

Macros - defined
- sample
- MSI macros - what are they?

Equivalent Gates
- defined
- measure of design density

AMCC CAD SUPPORT - INTRODUCTION
Design Flow Overview
SUMMARY - WHY ARRAYS
- Advantages
- Application Areas

MACRO - LOGIC EQUIVALENCE TABLES
as an aide to conversion from TTL or ECL to our macros:
- Q700
- Q1500
- Q3500 (TBS)

COURSE OBJECTIVE

- EFFECTIVE DESIGN PROCEDURES
- EFFECTIVE APPLICATION OF AMCC LOGIC ARRAYS
- INCLUDING:
  - STRUCTURED DESIGN
  - DESIGN CHECKLISTS
- EVERYTHING REQUIRED TO MAKE THE FIRST DESIGN A SUCCESSFUL DESIGN

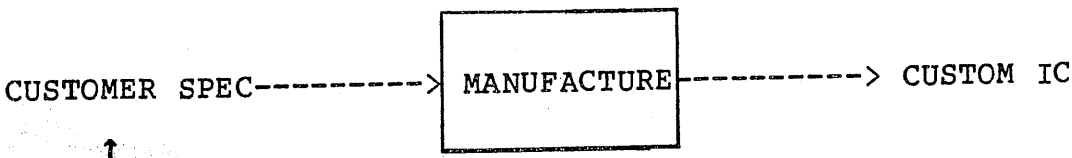
- SIMPLEST SEMICUSTOM:
  - ONE LEVEL INTERCONNECT
    - GATE ARRAYS
    - COMPONENT ARRAYS
- PROGRESS TO:
  - TWO AND MORE LEVELS INTERCONNECT
    - LOGIC ARRAYS
  - MOST COMPLEX (ALL LEVELS):
    - STANDARD CELL
      - LIBRARY
    - FULL CUSTOM
      - NO LIBRARY
- SILICON COMPILERS BEING EVALUATED TO REDUCE FULL CUSTOM DESIGN TIME

- THE LOGIC ARRAY FITS A HAPPY MEDIUM.
  - FULL LIBRARY
  - TWO OR MORE LEVELS
    (LESS LEVELS, LESS PROBLEMS

- AMCC HIGH PERFORMANCE SEMICUSTOM LOGIC ARRAYS
  - USER SPECIFIES TWO LAYERS OF METALIZATION PLUS VIA LAYER (THROUGH-HOLE)
  - Q3500 IS MULTI-LAYER (2 OR MORE)
  - POWER, SIGNAL CAN REACH ALL 4 SIDES
  - FACTOR OF 1-3 PRODUCTIVITY INCREASE OVER CUSTOM
  - LIBRARY DETERMINES DEGREE OF CUSTOMIZATION
    - LARGER LIBRARY PROVIDES FLEXIBILITY
    - MSI MACROS PROVIDE BLOCK-ARCHITECTURE APPROACH TO COMMON FUNCTIONS
  - SIZE OF THE LIBRARY MEANS THAT THE DIFFERENCE BETWEEN SEMICUSTOM AND CUSTOM WILL DECREASE

- AMCC SEMICUSTOM APPROACH USES ONLY 10% MORE SILICON THAN A FULL CUSTOM DESIGN WOULD - AND TAKES LESS TOTAL DESIGN TIME
- BEST TRADE-OFF BETWEEN FLEXIBILITY AND FAST DESIGN

- FULL CUSTOM IC

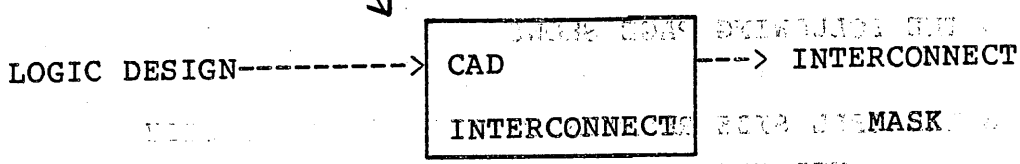


ALL MASK LAYERS

- AMCC LOGIC ARRAY - SEMICUSTOM

PREDEFINED SILICON

(BASE WAFER)



THREE MASK LAYERS (AT AMCC)

2-METALIZATION LAYERS

1-VIA LAYER

- PREDEFINED SILICON
  - TRANSISTORS
  - RESISTORS

AMCC
APPLIED MICRO CIRCUITS CORPORATION

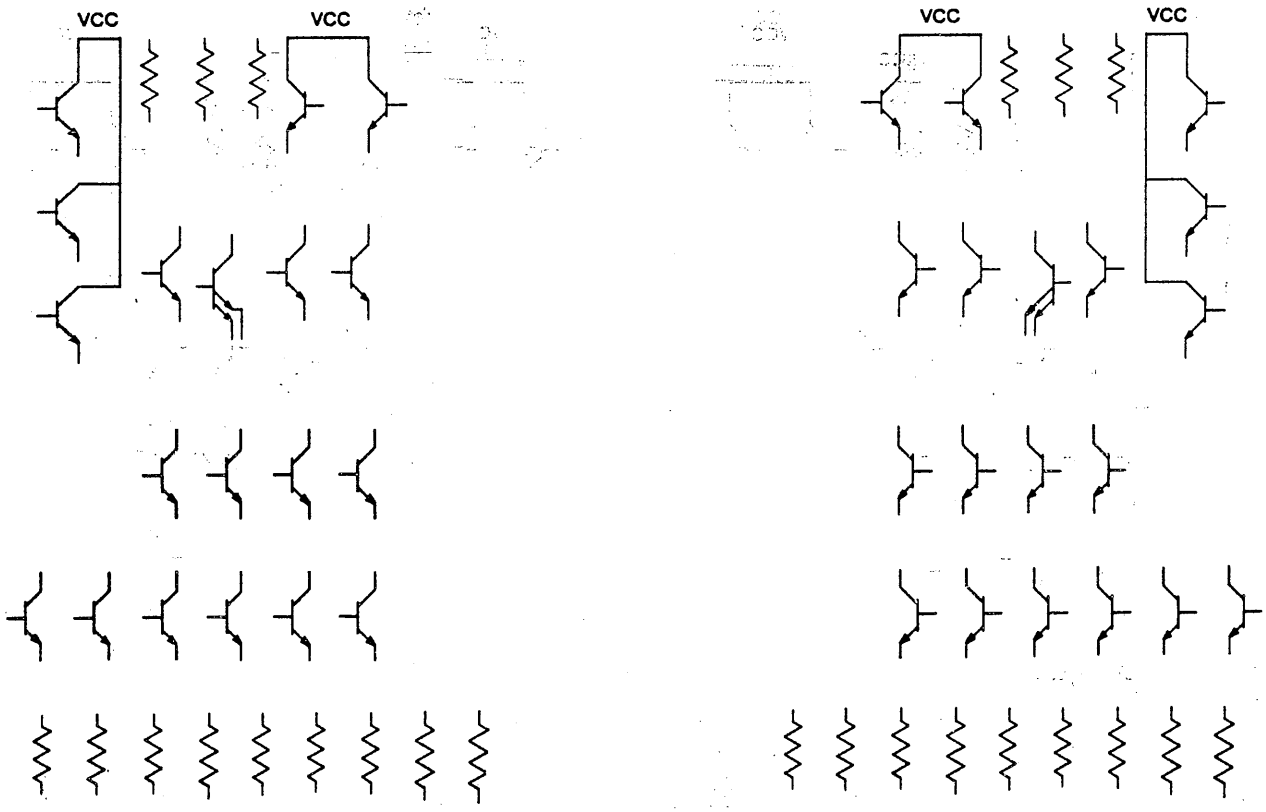
QUESTION: WHAT ARE THE USER-DEFINED INTERCONNECTION LAYERS?

- TWO METALIZATION LAYERS FOR AMCC

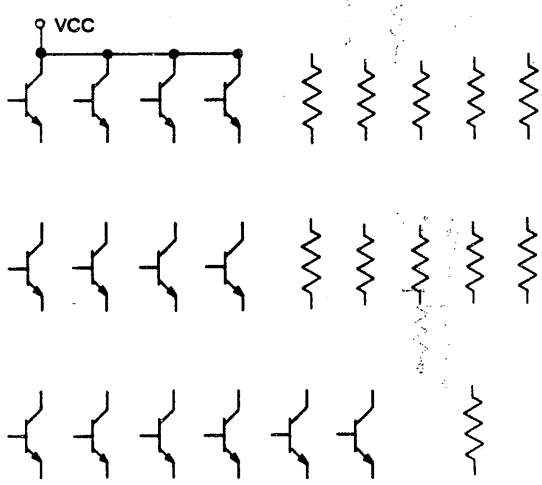
QUESTION: WHAT CONSTITUTES A CELL?

- UNCOMMITTED TRANSISTORS AND RESISTORS THAT ARE CUSTOMIZED BY THE MACROS
- THE Q1500 CELL IS DOUBLE THE SIZE OF THE Q700 (THERE ARE OTHER DIFFERENCES, OF COURSE)
- THE Q3500 CELL IS DOUBLE THE Q1500 CELL

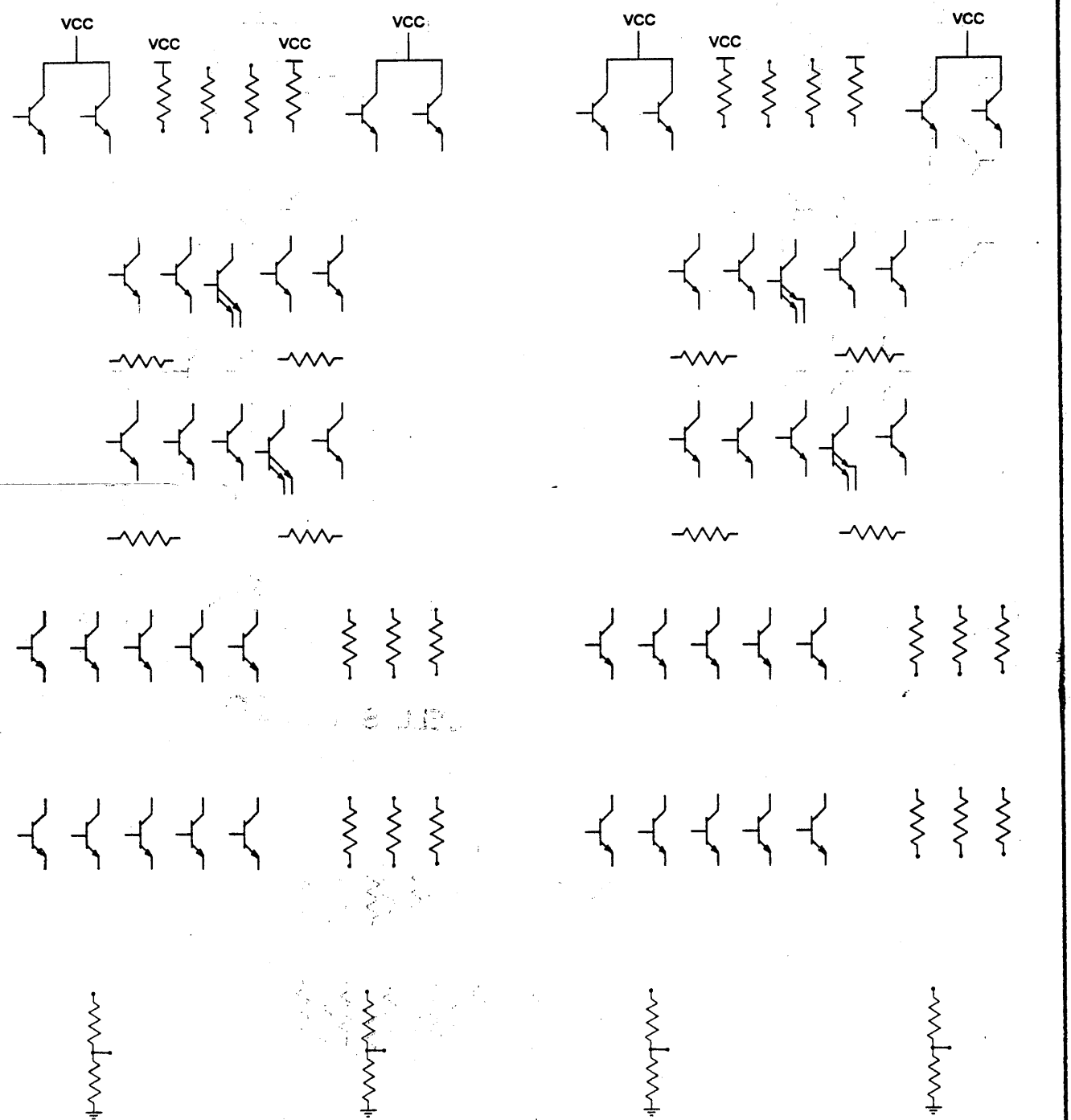
- THE NEXT PAGE DIAGRAMS THE BASIC LOGIC CELL (L CELL) FOR THE Q700 AND THE L CELL FOR THE Q1500
- THE FOLLOWING PAGE SHOWS THE Q3500 L CEL
- THE CELL SIZE RELATES TO THE DESIGN DENSITY
  - USE THE SMALLER ARRAYS WHEN THAT IS ALL YOU NEED



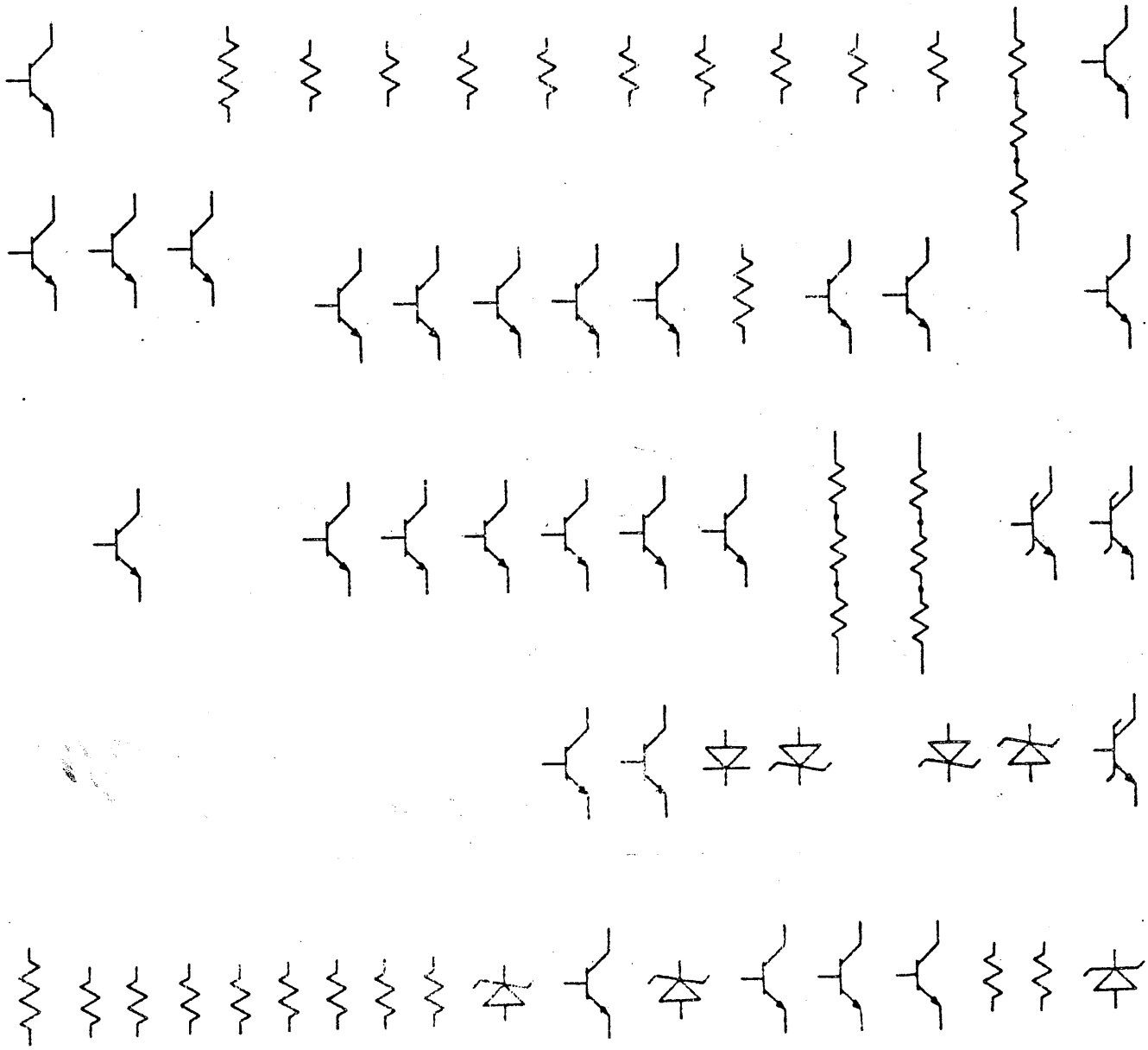
Q1500 SERIES LOGIC CELL SCHEMATIC



Q700 SERIES LOGIC CELL SCHEMATIC



Q3500 SERIES LOGIC CELL SCHEMATIC



Q3500 I/O CELL SCHEMATIC

— blank —

FEASIBILITY STUDY

POINTS TO CONSIDER:

- TECHNOLOGY
- LEVEL OF INTEGRATION
- DESIGN DENSITY REQUIRED
- UTILIZATION - SELECT FOR THE OPTIMUM
- I/O DRIVE, VOLTAGE LEVEL REQUIRED } START HERE BY YOUR DESIGN
- I/O INTERFACING REQUIRED BY THE ARRAY
- PIN-OUT
- POWER REQUIREMENTS FOR YOUR DESIGN
  - OPERATING POWER AND VOLTAGES AVAILABLE
- PERFORMANCE REQUIRED BY YOUR DESIGN
  - OPERATING SPEED POSSIBLE WITH THE ARRAY
- CRITICAL PATH ANALYSIS - DELAY TIMES
- OPERATING TEMPERATURE RANGE
- PACKAGING
- RADIATION TOLERANCE
- HIGH RELIABILITY SCREENING

COMPARING ARRAYS:
==========

QUESTION: WHAT IS THE TECHNOLOGY OF THE ARRAY SERIES?

TECHNOLOGY

- USE A MAINSTREAM TECHNOLOGY - ONE THAT WON'T DISSAPEAR A YEAR OR TWO DOWN THE ROAD
- AMCC USES DUAL METAL WASHED EMITTER HIGH SPEED BIPOLAR PROCESS - Q700, Q1500 SERIES
- USE A PROVEN PROCESS - STATE OF THE ART-
  5μCRON - Q700, Q1500 SERIES
- DON'T TAKE RISKS ON THE PROCESS
  - TOO MANY VARIABLES
- ECL INTERNAL - ECL AND/OR TTL EXTERNAL

- Q3500 SERIES - 3μCRON OXIDE-ISOLATED PROCESS
  - FASTER
  - 2 OR MORE LAYERS (CURRENTLY 2-LAYER METAL)

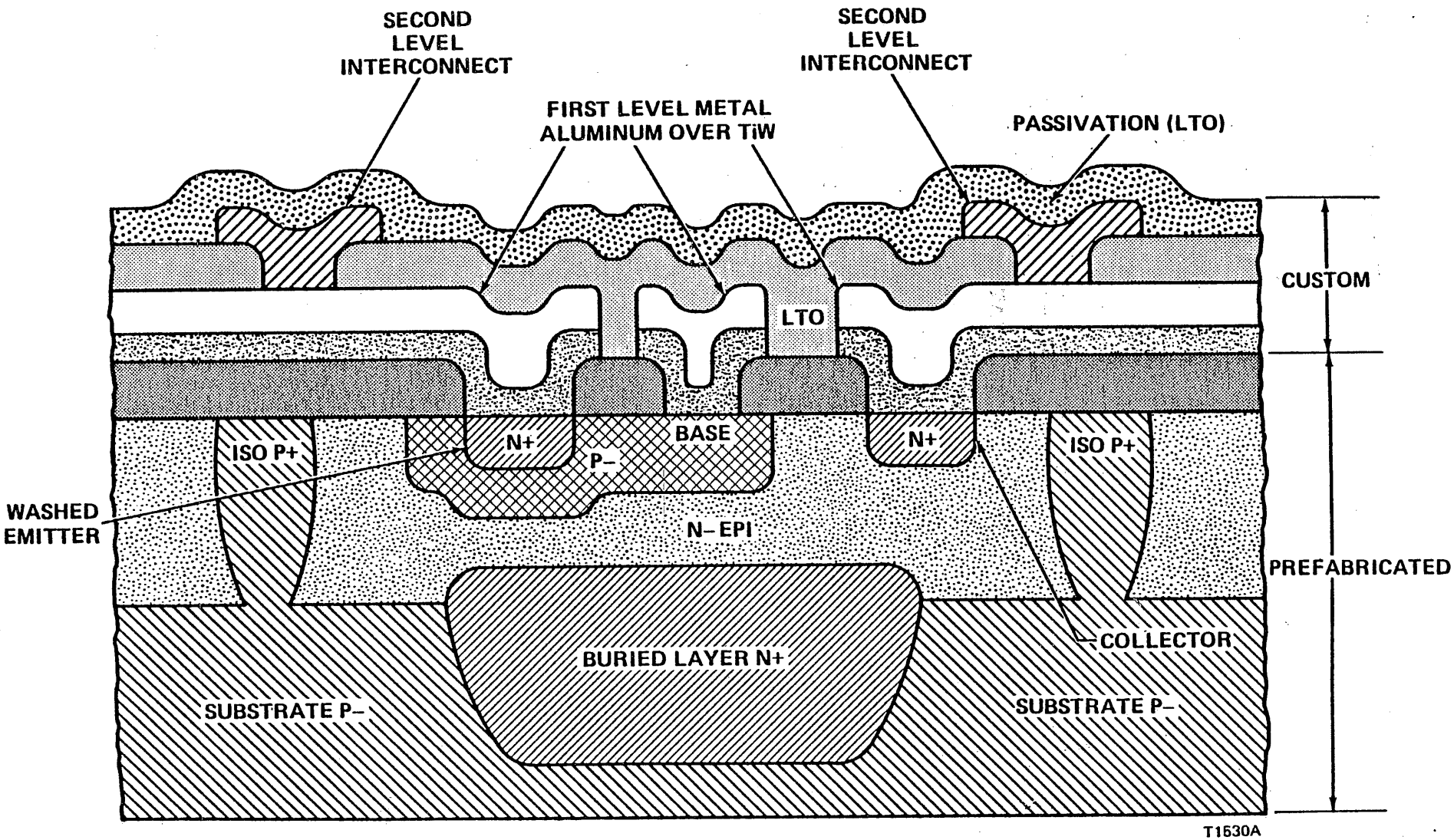
AMCC
APPLIED MICRO CIRCUITS CORPORATION

AMCC TECHNOLOGY (NEXT PAGE) - (Q700, Q1500 SERIES)

- PREFAB TO A P-SUBSTRATE
- SPEED IS APPROX TO EMITTER SIZE
  - WASHED EMITTER--5μcron SQ. EMITTER
  - DRILLED EMITTER MUST BE LARGER
- DIFFUSION/JUNCTION ISOLATED

- LAST DAY OF CLASS - TOUR OF THE FAB AREA AND A RUNNING DESCRIPTION OF THE PROCESS FOR THOSE INTERESTED

DUAL METAL WASHED EMITTER HIGH SPEED BIPOLAR PROCESS



- MACROS - WHAT ARE THEY?
  - AMCC REFERS TO A PREPROGRAMMED AND PREMODELED FUNCTIONAL ELEMENT AS A MACRO
  - A SIMPLE MACRO NORMALLY OCCUPIES ONE-HALF (.5) TO ONE (1) CELL
  - MACROS COME WITH DIFFERENT OPTIONS
    - POWER
    - HIGH-SPEED
    - LOW-POWER
  - DIFFERENT ARRAY SERIES HAVE DIFFERENT OPTIONS AVAILABLE
  - MACROS AND THEIR OPTIONS ARE DOCUMENTED IN THE DESIGN GUIDE FOR THE ARRAY SERIES

- ON THE NEXT PAGE

  (a) PROVIDES THE LOGIC REPRESENTATION FOR A 2:1 MUX

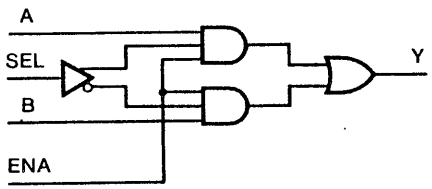
  (b) SHOWS THE DAISY (ALSO MENTOR, VALID EWS SYSTEM REPRESENTATION FOR A 2:1 MUX MACRO
  - THIS IS A Q700 MACRO

  (c) REPRESENTS THE ECL CELL DESIGN (PREDESIGNED AND PRETESTED) WHICH BECOMES INCORPORATED INTO THE MASKS OF THE CIRCUIT WHICH CALLS THIS MACRO

- IT IS THE COMBINATION OF THE MACROS AND THEIR INTERCONNECTIONS WHICH FORMS THE NETWORK THAT BECOMES THE ARRAY

FUNCTION CELLS

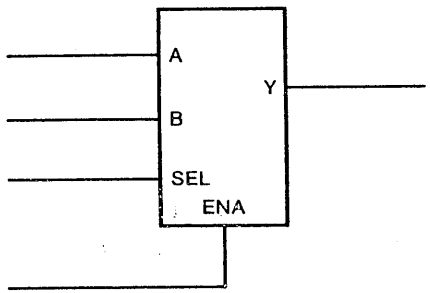
Logic Representation of 2 to 1 MUX



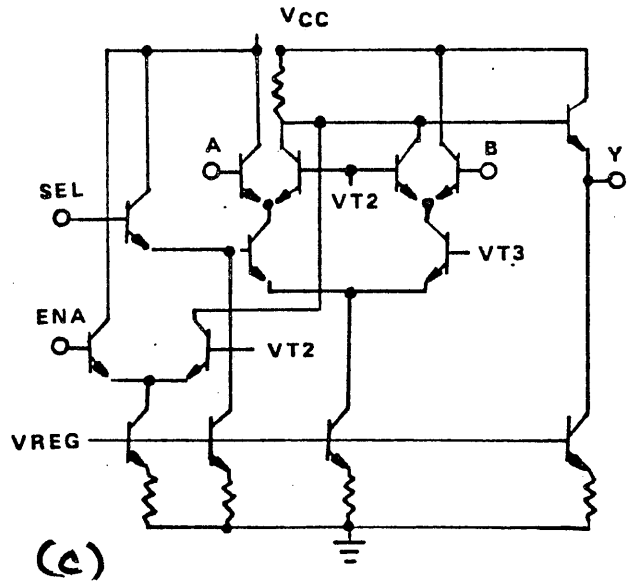
Gate Level Logic 2 to 1 MUX

(a)

Customer Designs with this ....



Logic 2 to 1 MUX

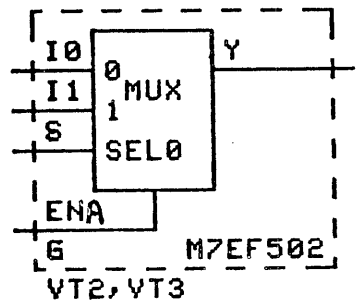


(c)

ECL CELL DESIGN 2 TO 1 MUX

DAISY MODEL

(b)



- MSI MACROS

  - AN MSI-MACRO IS ONE THAT PROVIDES AN MSI-EQUIVALENT FUNCTION
    - USING THE DEFINITION THAT MSI = 20 - 100 EQUIVALENT GATES
  - THESE ARE HIGH-FUNCTIONALITY MACROS

  - MSI MACROS SHARE COMPONENTS AMONG SEVERAL CELLS

  - AN EXAMPLE:
    - MS16 - 4-BIT UNIVERSAL REGISTER
      - 4 4:1 MUXS, 4 D F/F
    - MS16 USES 6 L CELLS

  - Q1500 SERIES, Q3500 SERIES USE MSI MACROS - AN EXPANDING COLLECTION

  - Q3500 SERIES USES THE "ABC" CONCEPT
    - AMCC BUILDING-BLOCK
      - MACROS HAVE SEVERAL DIFFERENT SHAPES FOR "BEST-FIT"

QUESTION: WHAT IS THE NUMBER OF EQUIVALENT GATES?

- 1 GATE = A 2-INPUT NAND OR NOR GATE
- A FALSE READING WHEN ESTIMATING WHAT AN ARRAY CAN DO FOR YOU
  - DEPENDS ON THE DESIGN!
- Q3500 MEANS 3500 "GATES" BUT WHAT YOU USE DEPENDS ON YOUR DESIGN, THE I/O REQUIRED, OTHER FACTORS

- REFER TO THE QUICKSHEETS FOR SOME SAMPLE MACROS FOR THE Q700, Q1500 AND Q3500 SERIES

- ACTUAL NUMBER OF GATES YOUR DESIGN REPRESENTS WILL VARY WITH THE DESIGN

- MSI MACROS ARE CELL-EFFICIENT, AND INCREASE THE DESIGN DENSITY

EQUIVALENT GATES

An equivalent gate is defined as a 2-input NOR gate, and the measure of design density is the number of these gates that would be required to construct the design in SSI logic.

The number of equivalent gates is also a sizing measure for the AMCC logical arrays.

SIZES OF THE AMCC ARRAYS

Array Name:	Number of Equivalent Gates:
Q3500S	3500
Q2400S	2400
QH1500A	1700
QM1600S	1600 + 1280 bits of RAM
Q1500A	1500
Q1300S	1300
Q700	1000
Q710	500
Q720	250

CAD SUPPORT

- ANALYZE HOW TO BEST APPLY SEMICUSTOM TO YOUR DESIGNS
- EVALUATE AS TO WHICH APPROACH SUITS YOUR NEEDS
- DECIDE WHO DOES THE DESIGN
    - AMCC
    - YOURSELF
        - REDUCES COST
        - MORE CONTROL OF DESIGN CYCLE
        - BETTER UNDERSTANDING OF THE DESIGN

AMCC
APPLIED MICRO CIRCUITS CORPORATION

- CAD SUPPORT - UP TO A FULL DESIGN SERVICE

- THE NEXT PAGE PROVIDES A VERY BRIEF OVERVIEW OF THE DESIGN CYCLE

    - THE CUSTOMER MUST SPECIFY THE SYSTEM

    * THE CUSTOMER PERFORMS SYSTEM PARTITIONING

    * THE CUSTOMER PERFORMS MACRO SELECTION/CONVERSION

    * THE CUSTOMER PERFORMS SCHEMATIC CAPTURE USING DAISY, MENTOR, VALID, TEGAS...

    * THE CUSTOMER PERFORMS DESIGN ANALYSIS SIMULATION, EVALUATION, ETC

    - AMCC PERFORMS LAYOUT AND VERIFICATION

    - AMCC PRODUCES THE PROTOTYPE AND DOES THE INITIAL TESTING

    - THE CUSTOMER PERFORMS THE FINAL SYSTEM EVALUATION

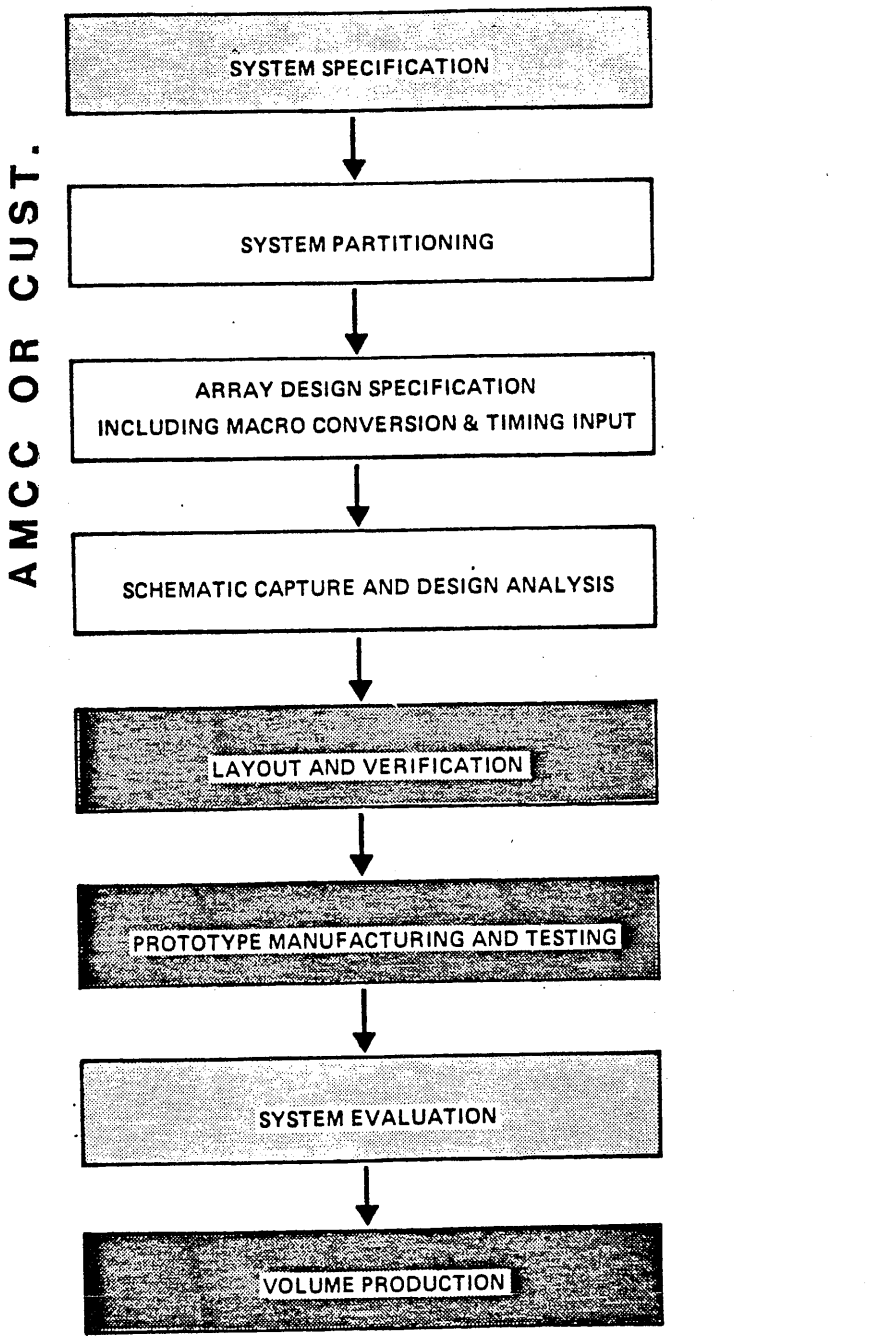
    - AMCC GOES INTO VOLUME PRODUCTION

* ON AN ITEM MEANS THAT AMCC IS AVAILABLE TO ASSIST OR TO PERFORM THE TASK - AT ADDITIONAL TIME AND CHARGES - IT IS FASTER IF YOU DO IT YOURSELF

FULL SERVICE SUPPLIER

AMCC
APPLIED MICRO CIRCUITS CORPORATION

LOGIC ARRAY DESIGN CYCLE



SUMMARY - WHY ARRAYS?

AMCC
APPLIED MICRO CIRCUITS CORPORATION

LOGIC ARRAY ADVANTAGES
-OVER STANDARD COMPONENTS

- FAST TURNAROUND TO PARTS (WAFERS IN STOCK)

  4-6 WEEKS AFTER FINAL DESIGN APPROVAL

- IMPROVED PERFORMANCE

  TRADEOFF AGAINST COST OF HIGH PERFORMANCE
  FULL CUSTOM

- LOWER POWER DISSIPATION

  TYPICAL OF GAIN FROM VLSI

- HIGHER RELIABILITY

  REDUCED PART COUNTS

  REDUCED PIN COUNTS

  ALSO TYPICAL FOR VLSI

- REDUCED SYSTEM COSTS

  FEWER PARTS

  LESS BOARD SPACE

  LOWER POWER NEEDS

  ALSO TYPICAL FOR VLSI

- PROPRIETARY DESIGN PROTECTION

  HARDER TO COPY OR REPRODUCE!

- CUSTOMER CONTROL OVER THE DESIGN

  - THIS IS NOT A MASS-PRODUCED FORCED-FIT

- LAST MINUTE CHANGES ARE POSSIBLE - CUSTOMER MAINTAINS CONTROL OVER THE DESIGN UNTIL PATTERN GENERATION

AMCC
APPLIED MICRO CIRCUITS CORPORATION

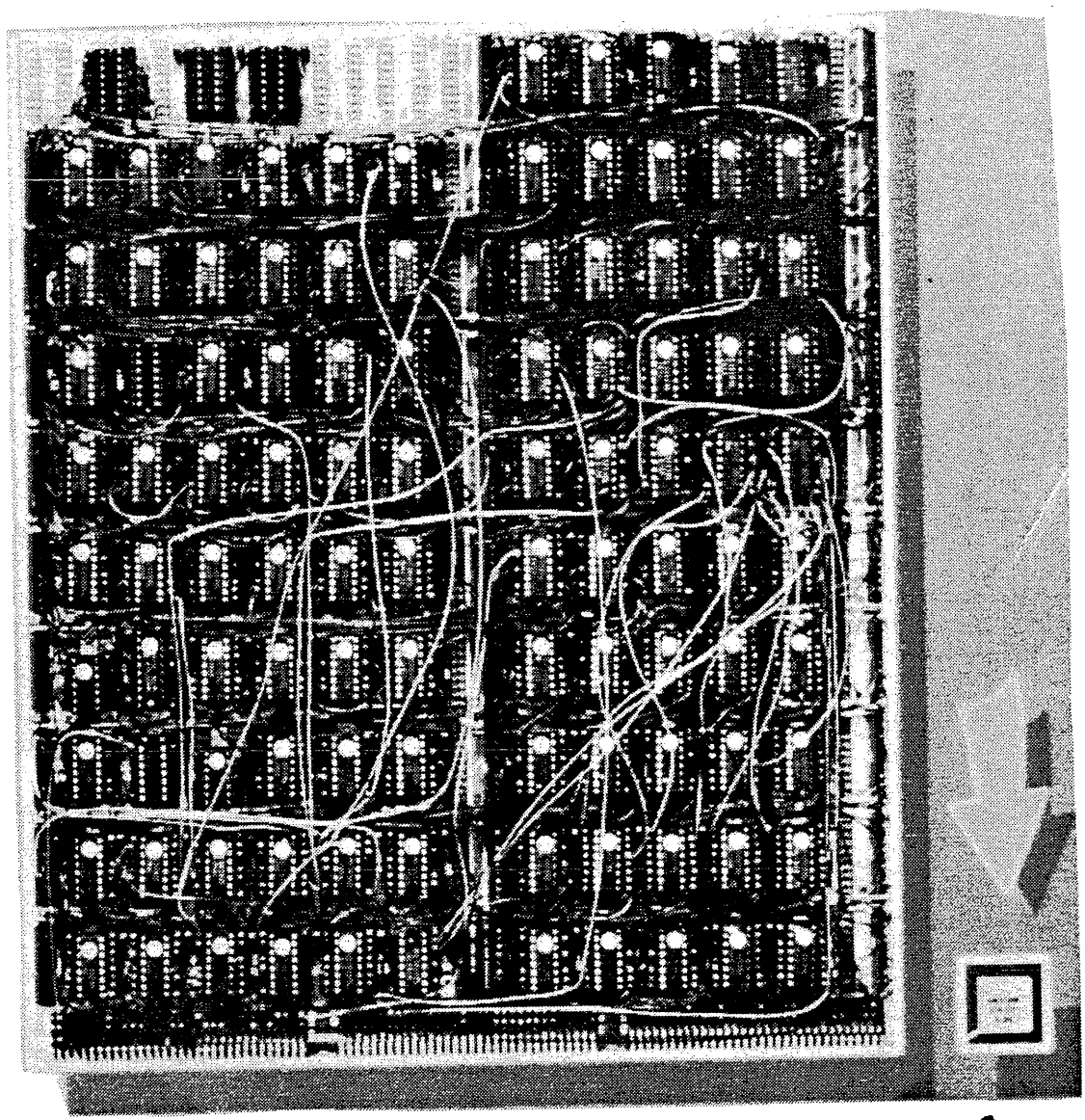
CASE IN POINT.....

THE BOARD:	THE ARRAY:
12 LAYER BOARD	2 LAYERS METAL
25 WATTS	2.5 WATTS (Q700)
20MHz	75MHz
11"x14"	!!!
COST OF BARE BOARD IS $1.50/SQ IN. PLUS COMPONENTS AND ASSEMBLY	LESS THAN $60.00/ARRAY IN PRODUCTION QUANTITY

THE ARRAY:

- LOWER POWER
- FASTER
- SMALLER
- COST EFFECTIVE
- DESIGN EDGE

12-Layer Board



AMCC
APPLIED MICRO CIRCUITS CORPORATION

AMCC LOGIC ARRAY APPLICATION AREAS

- OR WHO BENEFITS

- CPUS AND PERIPHERALS
- MINICOMPUTERS
- COMMUNICATIONS
- TEST EQUIPMENT
- MILITARY APPLICATIONS
    - RADAR
    - EW
    - AVIONICS
    - GUIDANCE
    - FLIGHT SIMULATION

etc.

- ARRAY APPLICATIONS -
  - FROM GARBAGE COLLECTION TO SYSTEM-ON-A-CHIP

- THE DESIGNER USING LOGIC ARRAYS CAN:
  - CAN DO ARCHITECTURAL CUSTOMIZATION
    - NOT HELD TO VON NEUMANN
  - GO TOWARD NEW ARCHITECTURES THAT ARE APPLICATION DRIVEN
  - CORE µPs ON ARRAYS UNDERMINE THIS APPROACH

- DON'T JUST MIMIC THE 74XX OR ECL 10K/100K FUNCTIONS
  - UNDERMINES FLEXIBILITY
  - AMCC HAS LARGE LIBRARIES
    - CAN PROVIDE 74XX-LIKE FUNCTIONS
    - CAN PROVIDE ECL 10K-LIKE FUNCTIONS
    - CAN PROVIDE ECL 100K-LIKE FUNCTIONS
    - BUT CAN ALSO PROVIDE FOR OTHERS
      ======
      - INNOVATIVE TECHNIQUES
      - INNOVATIVE SOLUTIONS

AMCC
APPLIED MICRO CIRCUITS CORPORATION

MACRO - LOGIC

EQUIVALENCE TABLES

==========

OPTIMIZED FUNCTIONS <----------> FAMILIAR CIRCUITS

ANALOG TO

HIGH LEVEL LANGUAGE <----------> ASSEMBLY LEVEL

==========

APPENDIX B
MACRO EQUIVALENCE TABLES

TTL DEVICE TYPE	# OF LOGIC FUNCTIONS/ TTL DEVICE	FUNCTION DESCRIPTION	# OF Q700 CELLS PER FUNCTION
74,74LS 74S SERIES:			
54/7400	4	2-input NAND gate	.5
54/7402	4	2-input NOR gate	.5
54/7408	4	2-input AND gate	.5*
54/7410	3	3-input NAND gate	.5*
54/7411	3	3-input AND gate	.5*
54/7420	2	4-input NAND gate	1*
54/7430	1	8-input NAND gate	2*
54/7432	4	2-input OR gate	.5*
54/7442	1	BCD-TO-DECIMAL-Decoder	5.5
54/7450	2	Expandable dual 2-wide 2-Input AOI gate	1
54/7451	2	2-Wide 2-Input AOI gate	1
54/7470	1	J-K Positive Edge-Triggered F/F	4
54/74H71	1	J-K Master-Slave F/F	4.5
54/7472	1	J-K Master-Slave F/F	4
54/7474	2	D-Type Edge-Triggered F/F Master/Slave	2
54/7475	4	Quad Bistable Latch	1
54/7476	2	J-K Master-Slave F/F	4
54/7478	2	J-K Negative Edge-Triggered F/F	4
54/7480	1	Gated Full Adder	3.5
54/7483	1	4-Bit Binary Full Adder, Ripple	13
54/7483A	1	4-Bit Binary Full Adder, Fast Ci	15
54/7485	1	4-Bit Magnitude Comparator, A=B only	8.5
		with A=B, A<B	12
		with A=B, A<B, A>B	16
		with A<B, or A>B	11
54/7486	4	2-input Exclusive OR gate	1
54/7489	1	16x4 Read/Write Memory	74
54/7490	1	Decade Ripple Counter	10
54/7491A	1	8-Bit Shift Register	16.5
54/7492	1	Divide-by-Twelve Ripple Counter	9
54/7492	1	Same with Reset	9.5
54/7493	1	4-Bit Binary Ripple Counter	8.5
54/7494	1	4-Bit Shift Register	16
54/7495A	1	4-Bit Shift Register	13
54/7496	1	5-Bit Shift Register	12.5
54/74100	2	4-Bit Transparent Latch	1
54H/74H102	1	J-K Negative Edge-Triggered F/F	4
54/74109	2	J-K Positive Edge-Triggered F/F without set or reset	3
54/74109	2	Same with Set or Reset	3.5
54/74109	2	Same with Set and Reset	4
54/74116	1	4-Bit Transparent Latch with Reset	4

TTL DEVICE TYPE	# OF LOGIC FUNCTIONS/ TTL DEVICE	FUNCTION DESCRIPTION	# OF Q700 CELLS PER FUNCTION
54/74138	1	1:8 Decoder/Demultiplexer	5
		with Enable	5.5
54/74139	2	1:4 Decoder/Demultiplexer	2
54/74148	1	8:3 Priority Encoder	10
54/74150	1	16:1 Multiplexer	12.5
54/74151A	1	8:1 Multiplexer	6
54/74153	2	4:1 Multiplexer	2
54/74154	1	1:16 Decoder/Demultiplexer	11
54/74155	2	1:4 Decoder/Demultiplexer	2.5
54/74157	4	2:1 Multiplexer	1
54/74158	4	2:1 Multiplexer, Inverting	1
54/74160	1	Synchronous BCD Decade Counter	17
54/74161	1	Synchronous 4-Bit Binary Counter	17
54/74162	1	Synchronous BCD Decade Counter	17
54/74163	1	Synchronous 4-Bit Binary Counter	17
54/74164	1	8-Bit Serial-In-Parallel-Out Shift Register	16.5
54/74170	1	4x4 Register File (O.C.)	26
54/74180	1	4-Bit Odd/Even Parity Generator/ Checker	9
54/74181	1	4-Bit ALU, Full Function	27
		without A=B	26
		without Lookahead	23
		without Lookahead, A=B	22
54/74182	1	Lookahead Carry Generator	7
54/74189	1	16x4 Read/Write Memory (3-state)	74
54/74190	1	BCD Decade Up/Down Counter	19
54/74191	1	4-Bit Binary Up/Down Counter	19
54/74193	1	4-Bit Binary Up/Down Counter	19
54/74195	1	4-Bit Parallel-Access Shift Generator	12
54/74240	1	Octal Inverter Buffer (3-State) No Hysteresis**	0
54/74245	1	Octal Bus Transceiver (3-State) No Hysteresis**	0
54/74259	1	8-Bit Addressable Latch	11
54/74670	1	4x4 Register File (3-State)	26
		Modulo-7 Johnson Counter	9
		4-Bit Preloadable Counter	16

* Use OR/NOR gate with inverted inputs
** Use I/O cells/macros to perform this function

ECL 10K DEVICE TYPE	# OF LOGIC FUNCTIONS/ ECL DEVICE	FUNCTION DESCRIPTION	# OF Q700 CELLS PER FUNCTION
10100/10500	4	2-Input NOR Gate with strobe	.5
10101/10501	4	OR/NOR gate	.5
10102/10502	4	2-Input NOR gate	.5
10103/10503	4	2-Input OR gate	.5
10104/10504	4	2-Input AND gate	.5
10105/10505	3	2-3-2-Input OR/NOR gate	.5
10106/10506	3	4-3-3-Input NOR gate	.5
10107/10507	3	2-Input EXOR/EXNOR	1.0
10109/10509	2	4-5-Input OR/NOR gate	1.0
10113/10513	4	EXOR gate	1.0
10117/10517	2	2-wide 2-3-Input OR-AND/OR-AND-INVERT gate	1.0
10118/10518	2	2-wide 3-Input OR-AND gate	1.0
10119/10519	1	4-wide 4-3-3-3-Input OR-AND gate	2.0
10121/10521	1	4-wide OR-AND/OR-AND-INVERT	2.0
10124/10524	4	TTL to MECL Translator	.5
10125/10525	4	MECL to TTL Translator	0
10130/10530	2	Latch	1.25
10131/10531	2	Type D Master-Slave F/F	2.5
10132/10532	1	Multiplexer with Latch and Common Reset	4.0
10134/10534	2	Multiplexer with Latch	2.0
10135/10535	2	J-K Master-Slave F/F	3.0
10136/10536	1	Universal Hexidecimal Counter	19.0
10137/10537	1	Universal Decade Counter	19.0
10138/10538	1	Bi-Quinary Counter	9.0
10141/10541	4	4-Bit Universal Shift Register	17.0
10153/10553	4	Latch (Negative Clock)	1.5
10158/10558	4	2-Input Multiplexer (Non-inverting)	1.0
10159/10559	4	2-Input Multiplexer (Inverting)	1.0
10160/10560	1	12-Bit Parity Generator/Checker	10.0
10161/10561	1	Binary to 1:8 Line Decoder (Low)	5.0
10164/10564	1	1:8 Multiplexer	5.0
10165/10565	1	8-Input Priority Encoder	14.0
10166/10566	1	5-Bit Magnitude Comparator	15.0
10168/10568	4	Latch (Common clock)	1.5
10170/10570	1	9 + 1-Bit Parity Checker	8.0

ECL 10K DEVICE TYPE	# OF LOGIC FUNCTIONS/ ECL DEVICE	FUNCTION DESCRIPTION	# OF Q700 CELLS PER FUNCTION
10171/10571	2	4-Line Decoder (Low)	2.0
10172/10572	2	4-Line Decoder (High)	2.0
10173	4	2-Input Multiplexer/Latch	2.0
10174/10574	2	4:1 Multiplexer	2.0
10175/10575	5	Latch	1.0
10176/10576	6	D Master-Slave F/F	2.0
10178/10578	1	Binary Counter	8.5
10179/10579	1	Look-Ahead Carry Block	7.0
10180/10580	2	Dual 2-Bit Adder/Subtractor	5.5
10181/10581	1	4-Bit ALU Full Function	27.0
		without A=B	26.0
		without Lookahead	23.0
		without Lookahead, A=B	22.0
10182/10582	1	2-Bit ALU	17.0
10197/10597	6	AND gate	0.5

TABLE 3 MACRO EQUIVALENCE

TTL DEVICE TYPE	FUNCTION	# OF LOGIC FUNCTIONS PER DEVICE	# OF Q1500 MACROS PER FUNCTION
54/7400	Quad 2-Input NAND Gate	4	1/4
54/7402	Quad 2-Input NOR Gate	4	1/4
54/7408	Quad 2-Input AND Gate	4	1/4
54/7410	Triple 3-Input NAND Gate	3	*1/4
54/7411	Triple 3-Input AND Gate	3	*1/4
54/7420	Dual 4-Input NAND Gate	2	*1/2
54/7430	8-Input NAND Gate	1	* 1
54/7432	Quad 2-Input OR Gate	4	1/4
54/7442	BCD-To-Decimal Decoder	1	3 1/2
54/7450	Expandable Dual 2-Wide 2-Input AOI Gate	2	1/2
54/7451	Dual 2-Wide 2-Input AOI Gate	2	1/2
54/7470	J-K Positive Edge-Triggered Flip-Flop	1	1 1/2
54H/74H71	J-K Master-Slave Flip-Flop	1	2
54/7472	J-K Master-Slave Flip-Flop	1	2
54/7474	Dual D-Type Edge-Triggered Flip-Flop	2	1
54/7475	Quad Bistable Latch	4	1/3
54/7476	Dual J-K Master-Slave Flip-Flop	2	1
54LS/74LS78	Dual J-K Negative Edge-Triggered Flip-Flop	2	1
54/7480	Gated Full Adder	1	1
54/7483	4-Bit Binary Full Adder, Ripple Carry	1	4
54LS/74LS83A	4-Bit Binary Full Adder, Fast Carry	1	4 1/2
54/7485	4-Bit Magnitude Comparator A=B only	1	4
54/7485	4-Bit Magnitude Comparator A=B, A<B	1	6
54/7485	4-Bit Magnitude Comparator A=B, A<B, A>B	1	8
54/7485	4-Bit Magnitude Comparator A<B or A>B	1	5 1/2
54/7486	Quad 2-Input Exclusive OR Gate	4	1/2
54LS/74LS89	16 X 4 Read/Write Memory	1	30
54/7490	Decade Ripple Counter	1	4
54/7491A	8-Bit Shift Register	1	6 1/2
54/7492	Divide-By-Twelve Ripple Counter	1	4
54/7492	Divide-By-Twelve Ripple Counter w/Reset	1	4
54/7493	4-Bit Binary Ripple Counter	1	3 1/2
54/7494	4-Bit Shift Register	1	6
54/7495A	4-Bit Shift Register	1	4 1/2
54/7496	5-Bit Shift Register	1	5
54/74100	Dual 4-Bit Transparent Latch	2	1/2
54H/74H102	J-K Negative Edge-Triggered Flip-Flop	1	1 1/2
54/74109	Dual J-K Positive Edge-Triggered Flip-Flop wo/S&R	2	1
54/74109	Dual J-K Positive Edge-Triggered Flip-Flop w/SorR	2	1
54/74109	Dual J-K Positive Edge-Triggered Flip-Flop w/S&R	2	1
54/74116	Dual 4-Bit Transparent Latch with Reset	1	1 1/2
54S/74S138	1-Of-8 Decoder/Demultiplexer	1	2
54S/74S138	1-Of-8 Decoder/Demultiplexer w/enable	1	2 1/2
54S/74S139	Dual 1-Of-4 Decoder/Demultiplexer	2	1
54/74148	8-To-3 Priority Encoder	1	4

*CONVERT TO NOR GATES - USE INVERTED INPUTS

MACRO EQUIVALENCE TABLE (CONT'D)

TTL DEVICE TYPE	FUNCTION	# OF LOGIC FUNCTIONS PER DEVICE	# OF Q1500 MACROS PER FUNCTION
54/74150	16-To-1 Multiplexer	1	4
54/74151A	8-To-1 Multiplexer	1	2
54/74153	Dual 4-To-1 Multiplexer	2	1
54/74154	1-Of-16 Decoder/Demultiplexer	1	4 1/2
54/74155	Dual 1-Of-4 Decoder/Demultiplexer	2	1
54/74S157	Quad 2-To-1 Multiplexer	4	1/2
54/74158	Quad 2-To-1 Multiplexer, Inverting	4	1/2
54/74160	Synchronous BCD Decade Counter	1	8 1/2
54/74161	Synchronous 4-Bit Binary Counter	1	8 1/2
54/74162	Synchronous BCD Decade Counter	1	8 1/2
54/74163	Synchronous 4-Bit Binary Counter	1	8 1/2
54/74164	8-Bit Serial-In-Parallel-Out Shifter	1	6
54/74170	4X4 Register File (O.C.)	1	11
54/74180	8-Bit Odd/Even Parity Generator/Checker	1	3 1/2
54/74181	8-Bit ALU Full Function	1	12
54/74181	8-Bit ALU w/o A=B	1	11 1/2
54/74181	8-Bit ALU w/o Lookahead	1	11
54/74181	8-Bit ALU w/o Lookahead & A=B	1	9 1/2
54/74182	Look-Ahead Carry Generator	1	4
54LS/74LS189	16X4 Read/Write Memory (3-State)	1	30
54/74190	BCD Decade Up/Down Counter	1	8
54/74191	4-Bit Binary Up/Down Counter	1	7
54/74193	4-Bit Binary Up/Down Counter	1	7
54/74195	4-Bit Parallel-Access Shift Register	1	4
54LS/74LS240	Octal Inverter Buffer (3-State) No Hysteresis*	1	0
54LS/74LS245	Octal Bus Transceiver (3-State) No Hysteresis*	1	0
54/74259	8-Bit Addressable Latch	1	5 1/2
54LS/74LS60	4X4 Register File (3-State)	1	11

*ACCOMPLISHED WITH I/O CELLS.
NO INTERNAL LOGIC CELLS REQUIRED.

MACRO EQUIVALENCE TABLE (CONT'D)

ECL 10K DEVICE TYPE	FUNCTION	# OF LOGIC FUNCTIONS PER DEVICE	# OF Q1500 MACROS PER FUNCTION
10100/10500	Quad 2-Input NOR Gate w/Strobe	4	1/4
10101/10501	Quad OR/NOR Gate	4	1/4
10102/10502	Quad 2-Input NOR Gate	4	1/4
10103/10503	Quad 2-Input OR Gate	4	1/4
10104/10504	Quad 2-Input AND Gate	4	1/4
10105/10505	Triple 2-3-2 Input OR/NOR Gate	3	1/4
10106/10506	Triple 4-3-3 Input NOR Gate	3	1/4
10107/10507	Triple 2-Input Exclusive OR/Exclusive NOR	3	1/2
10109/10509	Dual 4-5 Input OR/NOR Gate	2	1/2
10113/10513	Quad Exclusive OR Gate	4	2
10117/10517	Dual 2-Wide 2-3 Input OR-AND/OR-AND-INVERT Gate	2	1/2
10118/10518	Dual 2-Wide 3-Input OR-AND Gate	2	1/2
10119/10519	4-Wide 4-3-3-3-Input OR-AND Gate	1	1
10121/10521	4-Wide OR-AND/OR-AND-INVERT	1	1
10124/10524	Quad TTL-to MECL Translator	4	uses I/O
10125/10525	Quad MECL-to-TTL Translator	4	uses I/O
10130/10530	Dual Latch	2	1/3
10131/10531	Dual Type D Master-Slave Flip Flop	2	1
10132/10532	Dual Multiplexer w/Latch and Common Reset	1	2
10134/10534	Dual Multiplexer with Latch	2	1
10135/10535	Dual J-K Master-Slave Flip Flop	2	1
10136/10536	Universal Hexidecimal Counter	1	8
10137/10537	Universal Decade Counter	1	8
10138/10538	Bi-Quinary Counter	1	4
10153/10553	Quad Latch (Negative Clock)	4	1/2
10158/10558	Quad 2-Input Multiplexer (Non-Inverting)	4	1/2
10159/10559	Quad 2-Input Multiplexer (Inverting)	4	1/2
10160/10560	12-Bit Parity Generator/Checker	1	4
10161/10561	Binary to 1-8 Line Decoder (Low)	1	2
10164/10564	8-Line Multiplexer	1	2
10165/10565	8-Input Priority Encoder	1	5 1/2
10166/10566	5-Bit Magnitude Comparator	1	7 1/2
10168/10568	Quad Latch (Common Clock)	4	1/2
10170/10570	9 + 2-Bit Parity Checker	1	4
10171/10571	Dual 4-Line Decoder (Low)	2	1
10172/10572	Dual 4-Line Decoder (High)	2	1
10173	Quad 2-Input Multiplexer/Latch	4	2/3
10174/10574	Dual 4-to-1 Multiplexer	2	1
10175/10575	Quint Latch	5	1/3
10176/10576	Hex D Master-Slave Flip Flop	6	1
10178/10578	Binary Counter	1	3 1/2
10179/10579	Look Ahead Carry Block	1	4
10180/10580	Dual 2-Bit Adder/Subtractor	2	2
10181/10581	8-Bit ALU Full Function	1	12
10181/10581	8-Bit ALU w/o A=B	1	11 1/2
10181/10581	8-Bit ALU w/o Lookahead	1	11
10181/10581	8-Bit ALU w/o Lookahead & A=B	1	9 1/2
10182/10582	2-Bit Arithmetic Logic Unit & Function Generator		6 1/2
10197/10597	Hex AND Gate	6	1/4

Q3500 SERIES BIPOLAR GATE ARRAYS

CELL CAPABILITIES COMPARISON

	Moto 2500	AMCC Q2400S	AMCC Q3500S
2:1 Mux with Comm. Select (M252, M255, M256)	440	459	726
4:1 Mux with Enable (M251, M258)	110	153	242
2:4 Decoder with Enable (M261, M262)	220	153	242
2:4 Decoder High	110	153	242
Fast Add (M281)	110	153	242
D F/F with Reset (M291, M290)	220	229	363
D F/F with 2:1 Mux (M292)	110	153	242
2-Input gated XOR (M221)	440	306	484
4-Input XOR (M223)	220	306	484
D F/F with XOR (M296 + M293)	110	153	242
Direct Input from Package Pin	yes	yes	yes

Q3500 SERIES

— TBS —

THE LIBRARIES

CHAP 2 - THE LIBRARIES
Upward compatibility
Name conventions
- Q700
- Q1500/Q3500

Macros described
Logic Macros
- how to read the macro summary
- Q700 Examples
- Q1500 Examples
- Q3500 Examples
- MENTOR Examples

I/O
Mixed Mode
- power supply connections
- TTL output options
- ECL output buffer - Buffer limits

I/O Macros
- Q700 Examples
- Q1500 Exampls

TTL Input
- TTL Translator path worst-case multiplication factor

ECL Input
Q1500/Q3500 Series Feature - faster ECL
- IE85
- BIxx macros
- VTA generator

THE AMCC LOGIC ARRAY: ADVANTAGES

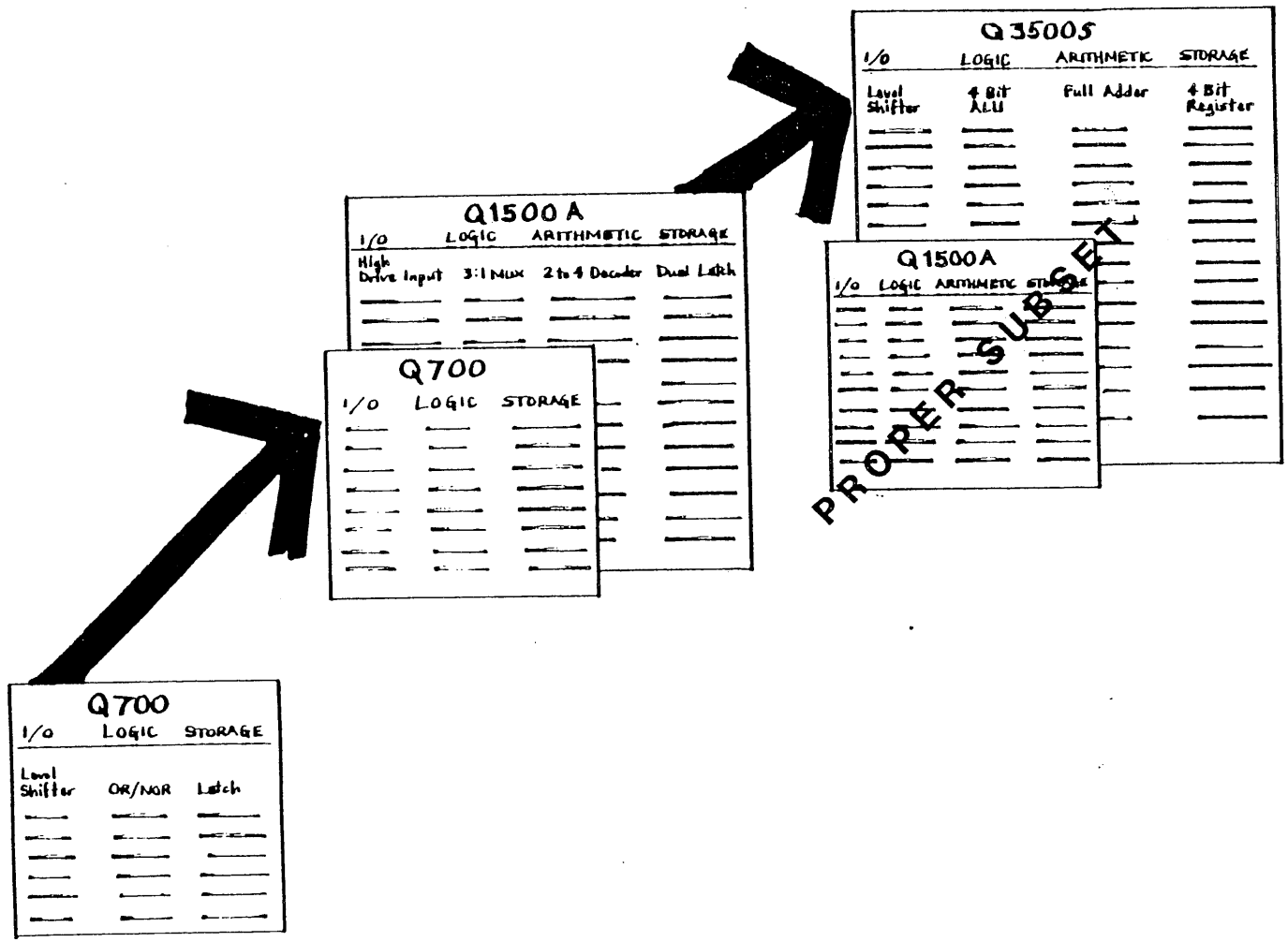
- EASE OF IMPLEMENTATION
    - POWERFUL SET OF MACROS
      - PREDESIGNED LOGICAL FUNCTIONS
    - HIGH FUNCTIONALITY
- UPWARD COMPATIBLE MACRO LIBRARIES
    - EASY UPGRADE TO LARGER ARRAY WHEN NEEDED

    Q700 SERIES ----> Q1500 SERIES

    Q1500 SERIES ----> Q3500 SERIES
- Q700 SERIES NAMES ARE DIFFERENT FROM THE REST OF THE ARRAY SERIES - FUNCTIONS ARE UPWARD COMPATIBLE TO Q1500 SERIES
- Q1500, Q3500 SERIES NAMES FOLLOW THE CONVENTION LISTED

AMCC
APPLIED MICRO CIRCUITS CORPORATION

UPWARDLY COMPATIBLE MACRO LIBRARY



Q700 name conventions:

M7AXnnn

M7:
M7 is the prefix on all Q700 series names.

A:
T = TTL
E = ECL

X:
B = I/O cell
I = I cell
Z = D cell (16 loads)
F = Function (including buffer) (L, B CELL)
D = Driver (15 loads) (L, B CELL)
P = Power option (L, B CELL)

nnn:

TB10n TB11n	}TTL I/O On An I/O CELL
TI10n TI11n	}TTL INPUT On An I CELL
TF22n	TTL INPUT BUFFER
TD22n	TTL INPUT BUFFER-DRIVER (15 LOADS)
TZ001	3-STATE EnABLE-DRIVER On A D CELL
EB10n EB11n	}TTLMIX I/O On An I/O CELL
EI10n	TTLMIX INPUT On An I CELL
EF20n EF23n	TTLMIX INPUT BUFFER
ED20n	TTL INPUT BUFFER-DRIVER (15 LOADS)
EF28n	TTLMIX OUTPUT BUFFER
EZ001	3-STATE EnABLE-DRIVER On A D CELL
EB15n	ECL I/O On An I/O CELL
EI10n	ECL INPUT On An I CELL
EF24n	ECL INPUT BUFFER
ED24n	ECL INPUT BUFFER-DRIVER (15 LOADS)
EF25n	ECL INPUT BUFFER
EF26n	ECL INPUT BUFFER
EF27n	ECL OUTPUT BUFFER
EF35n	2-INPUT INVERTERS, OR, NOR GATES
EF36n	4,5-INPUT OR, NOR GATES
EF37n	CLOCK BUFFERS
EF38n	GATE MACROS
EF39n	GATE MACROS
EF4nn	EXOR NETWORKS
EF5nn	MUXS
EF6nn	DECODERS
EF7nn	LATCHES

NEW MACRO NAMING CONVENTION- Q1500/QH1500/Q3500

THE EXPANSION OF A MACRO NAME (USING THE NEW CONVENTION)
IS GIVEN BELOW:

```
GT  40 P B A
 :  :  : : :
 :  :  : : ---------- REVISION LETTER - NOT USED TO CALL
 :  :  : :                           IT FOR THE EWS
 :  :  : :
 :  :  : ------------ LOCATION:    SITE     Q1500  QH1500  Q3500
 :  :  :                          ------------------------------
 :  :  :                          INPUT       I      J       -
 :  :  :                          OUTPUT      O      -       -
 :  :  :                          I/O         -      Q       X
 :  :  :                          LOGIC       L      L       Y
 :  :  :                          ECLOP       B      B       -
 :  :  :                          DOUBLE I/O  -      D       -
 :  :  :                          ------------------------------
 :  :  :
 :  :  ------------------ POWER/FANOUT:  S - STANDARD     (6 LOADS)
 :  :                                   P - POWER        (9 LOADS)
 :  :                                   H - HIGH SPEED   (9 LOADS)
 :  :                                   D - DRIVER      (15 LOADS)
 :  :                                   L - LOW POWER    (3 LOADS)
 :  ---------------------- CELL # (00-99)
 :
 ------------------------- CELL TYPE:
```

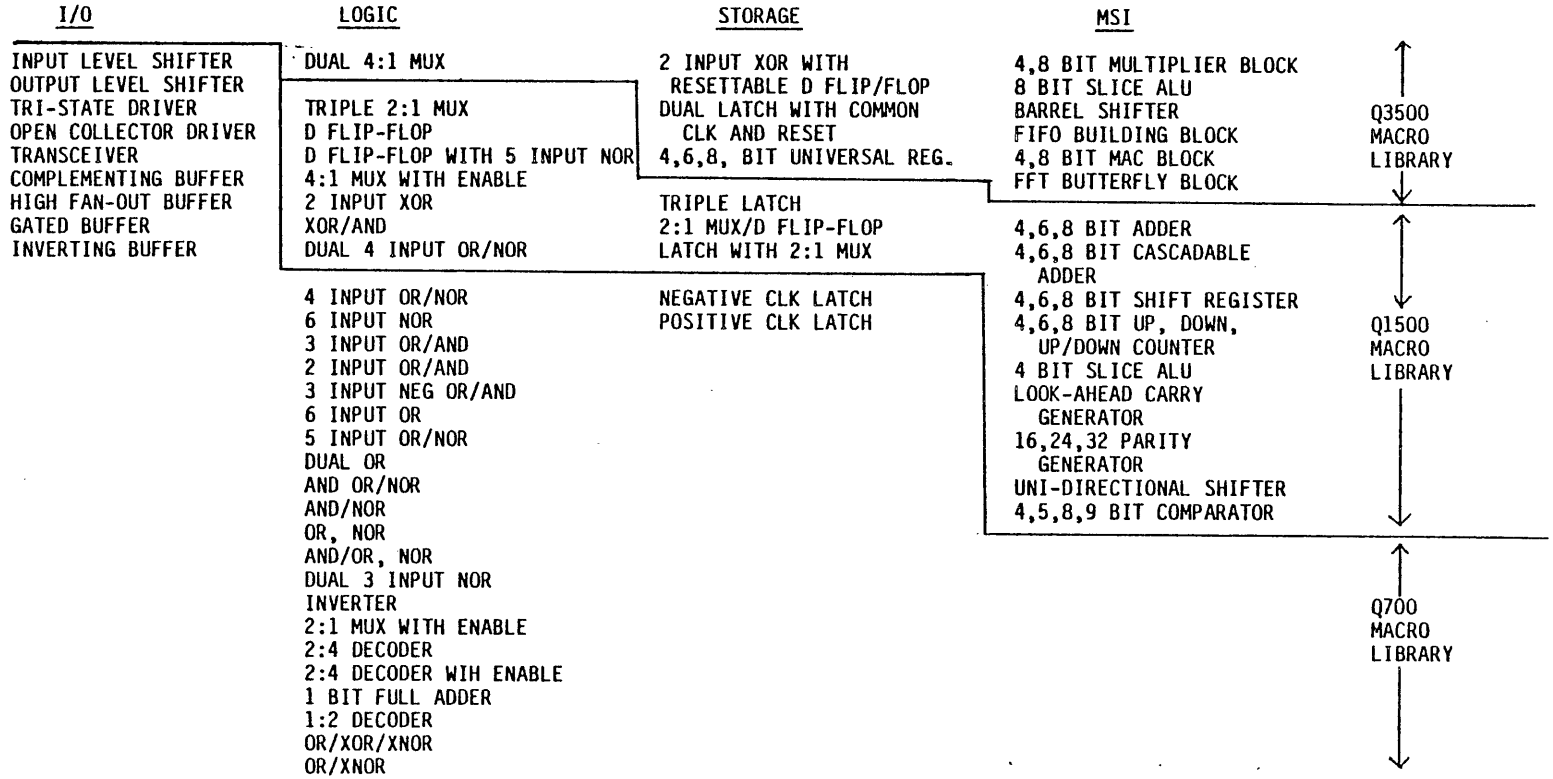
INPUT	INTERNAL
IE - ECL 10K/100K	AD - ADDER
IP - +5V REF ECL 10K/100K	BB - MSI BUILDING BLOCK - AMCC USE ONLY
IT - TTL	BE - ECL OUTPUT BUFFER
	BI - ECL INPUT BUFFER
	CP - CLOCK DRIVER
OUTPUT	DE - DECODER
OE - ECL 10K	EL - EXTENDED LIBRARY - COMMERCIAL ONLY
OP - ECL 10K (+5V REF)	EX - EXOR
OK - ECL 100K	FF - F/F
OQ - ECL 100K (+5V REF)	GT - GATE
OT - TTL	IB - INPUT BLANK CELL - AMCC USE ONLY
	LA - LATCH
BIDIRECTIONAL	MM - MEMORY MODULE
UE - ECL 10K	MS - MSI DEVICE - COMPOSED OF BB CELLS
UP - ECL 10K (+5V REF)	MX - MUX; MULTIPLEXOR
UK - ECL 100K	OB - OUTPUT BLANK CELL - AMCC USE ONLY
UQ - ECL 100K (+5V REF)	SP - SPECIAL CELL (CUSTOM) - AMCC USE ONLY
UT - TTL	

FOR TTL I/O MACROS: 00-39 INDICATES 100% TTL
40-79 INDICATES TTLMIX
FOR ECL I/O MACROS: ECL STANDARD REF IS -5.2V (ECL 10K); -4.5V (ECL 100K)
+5V ECL 10K/100K USES 0V TO +5V

- THE LIBRARIES
    - EACH ARRAY SERIES HAS ITS OWN LIBRARY
    - THE Q700, Q710, AND Q720 SHARE ONE LIBRARY - WITH A FEW MACROS RESTRICTED TO THE Q700 (THOSE PLACED ON THE D CELLS)
    - THE Q1500 AND THE QH1500 SHARE THE LOGIC MACROS BUT HAVE UNIQUE I/O LIBRARIES (SOME MACROS ARE THE SAME BUT THEY ARE DUPLICATED TO AVOID PROBLEMS)
    - THE Q3500 SERIES HAS ONE BASIC LIBRARY AND A SPECIAL SECTION ON MEMORY-MACROS FOR THE QM1600S
- THE MACRO LIBRARIES ARE GROWING
    - MSI IS BEING ADDED TO THE Q1500, Q3500
    - NEW MACROS CAN BE CUSTOMIZED TO YOUR DESIGN IF NEEDED - CUSTOM MACROS
- COMMERCIAL AND MILITARY TEMPERATURE RANGES ARE BOTH AVAILABLE

AMCC
APPLIED MICRO CIRCUITS CORPORATION

INCREASING FUNCTIONALITY MACROS



- THE BUILDING BLOCK EVOLUTION OF THE HARDWARE MATCHES THE EVOLUTION OF THE MACRO LIBRARIES

- SSI ~2-10 GATES
  - BASIC MACROS
    - AND/NAND
    - OR/NOR

- MSI ~20-100 GATES
  - LOGIC MACROS
    - MUXs
    - DECODERS
    - F/Fs
  - MSI LOGIC MACROS
    - 4-BIT UNIVERSAL REGISTER
    - 4-BIT UP COUNTER
    - 4-BIT COMPARATOR

- LSI ~200-1000 GATES
  - FUTURE EXPANSION
    - APPLICATION NOTES
    - SEQUENCERS (Am2910)
    - CONTROLLERS
    - REGISTERED ALUs (Am2901, Am29203)
    - FLOATING POINT

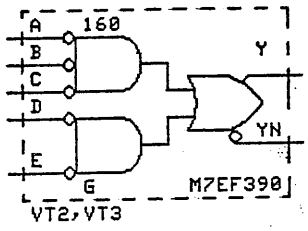
- MEMORY DEVICES
  - RAM ON AN ARRAY (QM1600S)
  - MEMORY MACROS
    - TBS

- VLSI
  - THE ARRAYS THEMSELVES

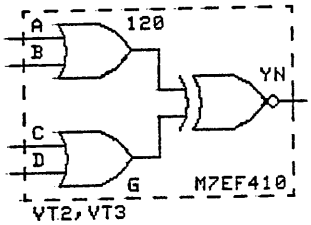
LOGIC MACROS

AMCC
APPLIED MICRO CIRCUITS CORPORATION

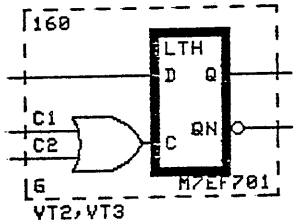
BASIC GATE STRUCTURE



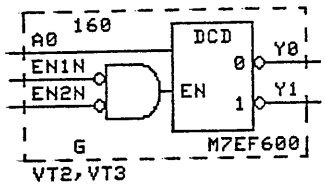
EXNOR NET



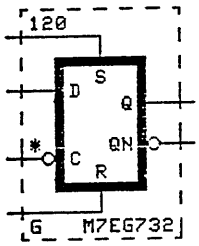
LATCH



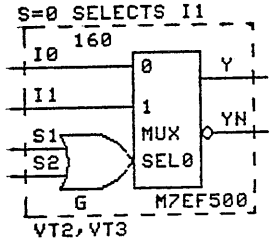
DECODER



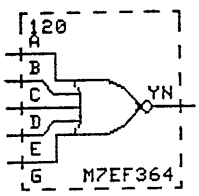
LATCH WITH SET AND RESET



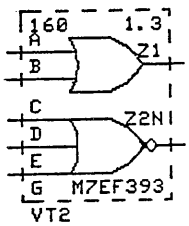
2:1 MUX WITH SEL0 SELECT
S=0 SELECTS I1



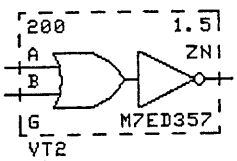
5-INPUT NOR

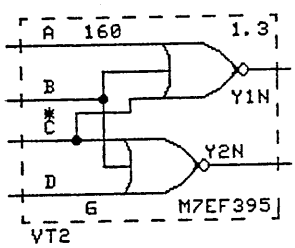


2-INPUT OR AND 3-INPUT NOR



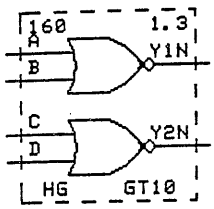
DRIVER - 15 LOAD LIMIT

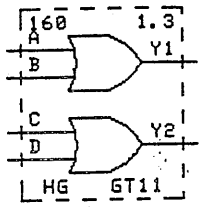




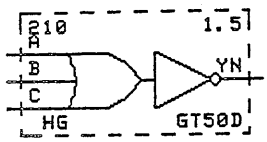
EXAMPLE Q700 MACROS

APPLIED MICRO CIRCUITS CORPORATION

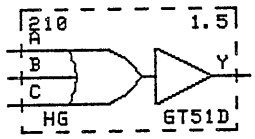


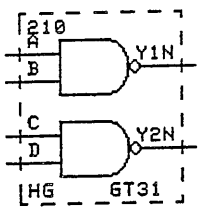


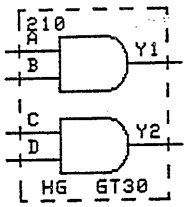
BASIC GATES

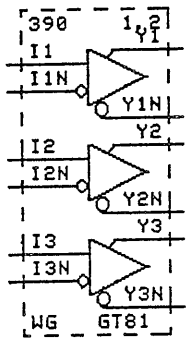


DRIVERS

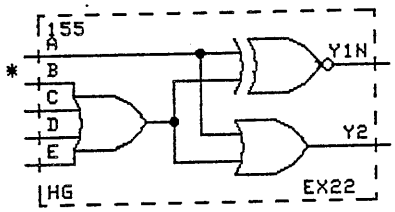






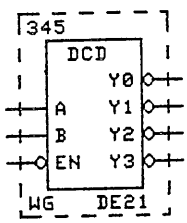


TRIPLE BUFFER

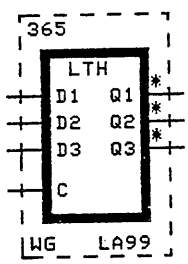


EXOR NET

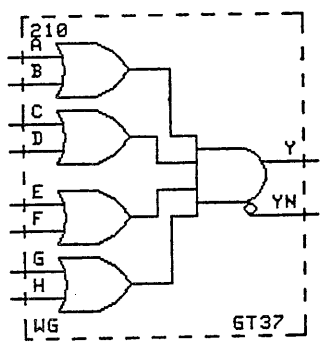
A COUNTS AS 1 LOAD

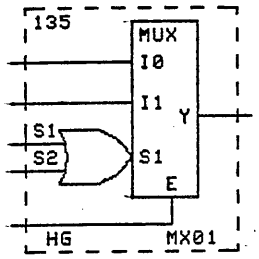


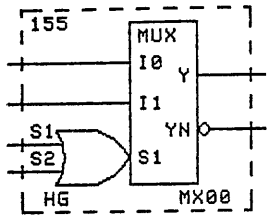
1 OF 4 DECODER

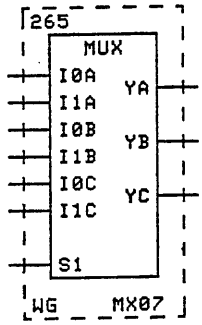


TRIPLE D LATCH, COMMON CLOCK

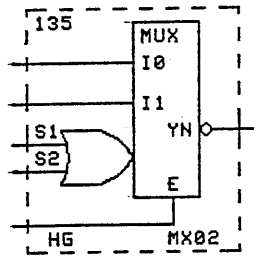


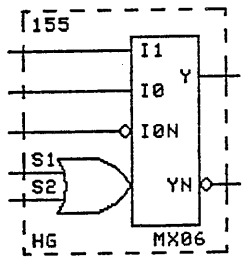






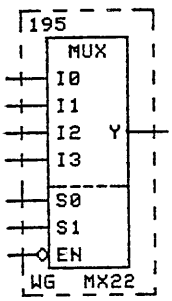
MUXS WITH ENABLE



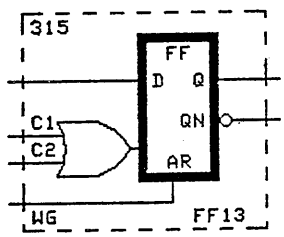


TRIPLE 2:1 MUX,
COMMON SELECT

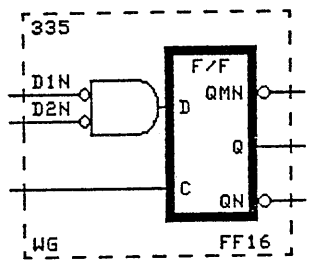
I0, I0N DIFFERENTIALLY DRIVEN

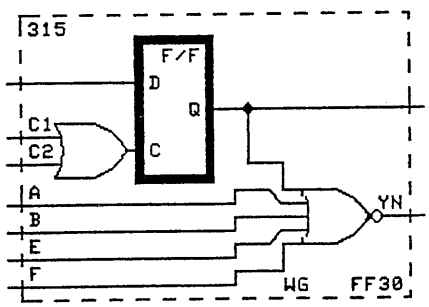


4:1 MUX WITH ENABLE



REPLACES FF11





ALSO FF25, FF31 (TBS)

- THE MACROS ARE AVAILABLE WITH OPTIONS
  - Q700 SERIES
    - STANDARD
    - POWER
  - Q1500 SERIES
    - STANDARD
    - HIGH-SPEED
    - POWER
  - Q3500 SERIES
    - STANDARD
    - HIGH-SPEED
    - SUPER-HIGH-SPEED
    - LOW-POWER
- ALL LIBRARIES HAVE THREE-STATE ENABLE DRIVERS
- ALL LIBRARIES HAVE HIGH-FANOUT DRIVERS
- PUT SPEED OR POWER ONLY WHERE YOU NEED IT
- SPEED-POWER PROGRAMMABILITY

SAMPLE MACROS: Q700

- THE NEXT PAGE SHOWS THE M7TF222 MACRO FOR THE Q700 SERIES
  - THE POWER-OPTION (P-OPT) VERSION OF THE MACRO IS M7TP222

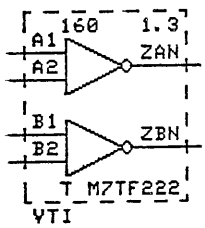
	STANDARD	POWER	
T_{pd}	1.3	1.3	ns
I_{CC}	1.6	2.0	mA
LOADS	6	9	

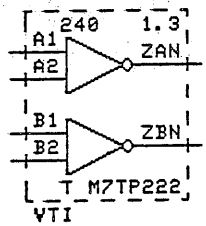
- A SPECIAL SET OF MACROS IS AVAILABLE FOR HIGH FAN-OUT
  - M7TD228 IS ONE OF THESE

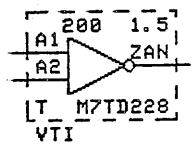
T_{pd} = 1.5ns
I_{CC} = 2.0mA
15 LOADS

AMCC
APPLIED MICRO CIRCUITS CORPORATION

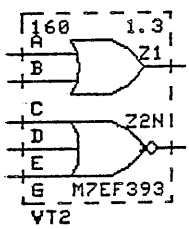
Q700 MACROS: VERSIONS

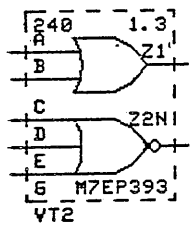


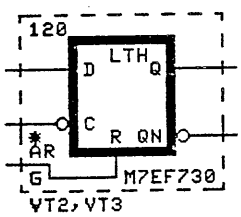


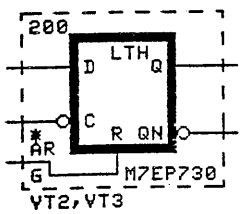


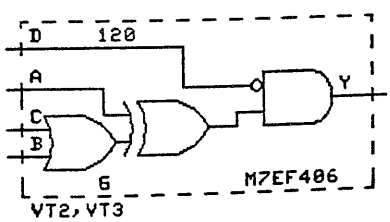
THIS IS A DIFFERENT MACRO

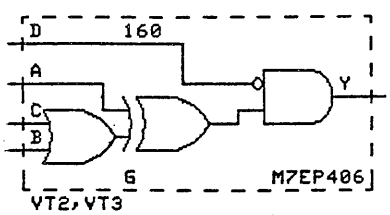












AMCC Q700 MACRO LIBRARY SUMMARY - INTERNAL LOGIC MACROS LOGIC

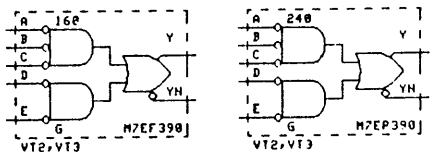
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES T_A = 25°
I = I_{CC} FOR 100% TTL CIRCUITS, ELSE I = I_{EE}

M7EF390 L/B cell 3-INPUT, 2-INPUT OR-AND/NAND

	S	P	H	
Tpd A,B,C->Y,YN	1.3	1.3		ns
D,E->Y,YN	2.0	2.0		ns
I	1.6	2.4		mA

PRELIMINARY

$Y = (\bar{A}\,\bar{B}\,\bar{C}) + (\bar{D}\,\bar{E})$

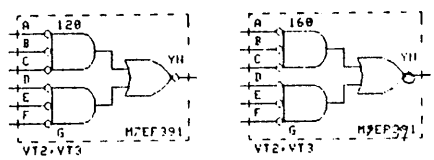


M7EF391 L/B cell 2-TERM 3-INPUT OR-AND

	S	P	H	
Tpd A,B,C->YN	1.3			ns
D,E,F->YN	2.0			ns
I	1.2	1.6		mA

PRELIMINARY

$YN = \overline{(\bar{A}\cdot\bar{B}\cdot\bar{C}) + (\bar{D}\cdot\bar{E}\cdot\bar{F})}$



AMCC Q700 MACRO LIBRARY SUMMARY - INTERNAL LOGIC MACROS LOGIC

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES $T_A = 25^o$
$I = I_{CC}$ FOR 100% TTL CIRCUITS, ELSE $I = I_{EE}$

M7EF720 L/B cell NEGATIVE TRANSPARENT LATCH WITH ASYNC. SET

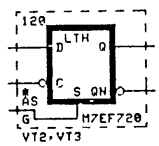
	S	P	H	
Tpd C->Q,QN	1.7			ns
D->Q,QN	1.4			ns
AS->Q,QN	1.4			ns
Tsu	1.5			ns
Th	0.5			ns
PW C->Q	4.0			ns
PW AS->Q	10.0			ns
I	1.2	2.0		mA

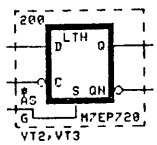
2.1 min
0.7 min

* CLK FROM M7EF370/371/372

$Q_{n+1} = (AS \cdot C) + (C \cdot Q_n) + (\bar{C} \cdot D)$

D	C	AS	Q_{n+1}
0	0	X	0
1	0	X	1
X	1	0	Q_n
X	1	1	1





M7EF730 L/B cell NEGATIVE TRANSPARENT LATCH WITH ASYNC. RESET

	S	P	H	
Tpd C->Q,QN	1.7			ns
D->Q,QN	1.4			ns
AR->Q,QN	1.4			ns
Tsu	1.5			ns
Th	0.5			ns
PW C->Q	4.0			ns
PW AR->Q	10.0			ns
I	1.2	2.0		mA

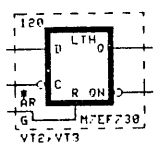
Same Time

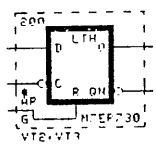
2.1 min
0.7 min

* CLK FROM M7EF370/371/372

$Q_{n+1} = (\bar{C} \cdot D) + C \cdot Q \cdot \overline{AR}$

D	C	AR	Q_{n+1}
0	0	X	0
1	0	X	1
X	1	0	Q_n
X	1	1	0



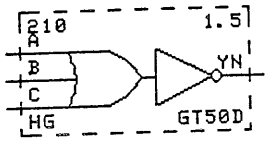


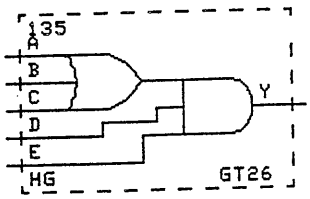
SAMPLE MACROS: Q1500/QH1500

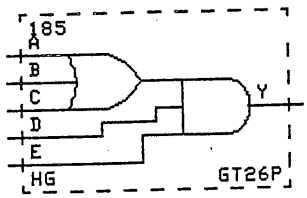
- THE NEXT PAGE SHOWS SOME OF THE Q1500/QH1500 MACROS AND THEIR OPTIONS
- THERE IS A STANDARD, A POWER (MORE DRIVE) AND A HIGH-SPEED VERSION OF MANY OF THE MACROS

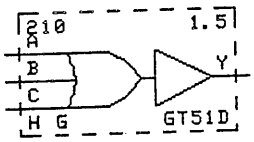
- GT50D, GT51D, GT52D
  - SOME OF THE 15-LOAD DRIVERS
  - THESE HAVE NO OPTIONS
- BIXX SERIES EXAMPLES
  - MUST CONNECT TO VTA GENERATOR
  - S (DEFAULT), P AND H SHOWN
- GT26, GT26P
  - SOME GATE MACROS HAVE NO H OPTION (AS YET)
- FF13, FF13P, FF16, FF16P
  - NEW FLOP/FLOPS
  - NO HIGH SPEED OPTIONS ON THESE

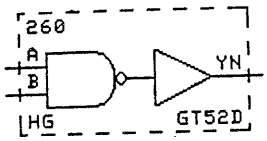
AMCC
APPLIED MICRO CIRCUITS CORPORATION

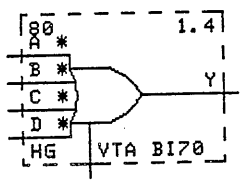


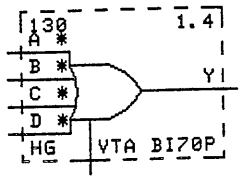


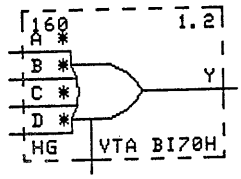


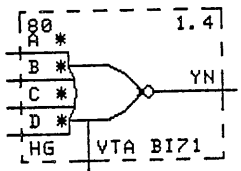


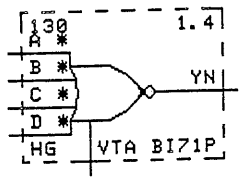


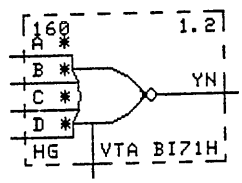




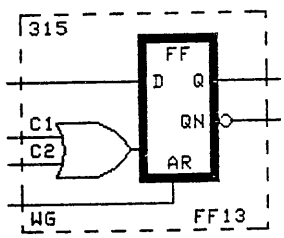


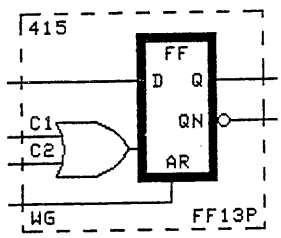


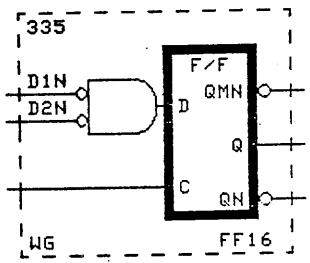


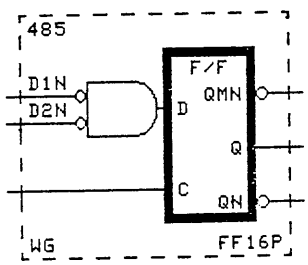


VTA







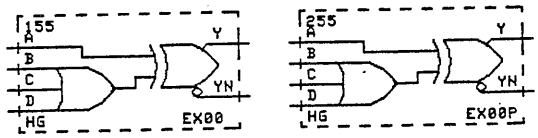


AMCC Q1500/QH1500 MACRO SUMMARY - EXxx

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES $T_A = 25^oC$
$I = I_{CC}$ FOR SINGLE +5V POWER SUPPLY, ELSE $I = I_{EE}$

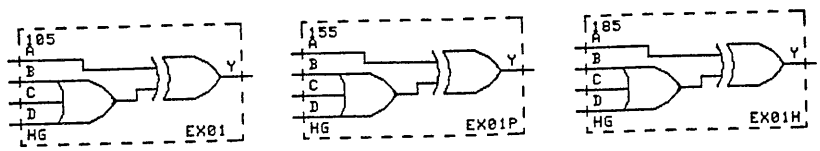
EX00	0.5 L/B cell	3-INPUT OR-EXOR/EXNOR		
	S	P	H	
Tpd A->Y	1.3	1.3		ns
B,C,D->Y	2.0	2.0		ns
I	1.55	2.55		mA
FANOUT LOAD LIMIT:	6	9		

$Y = A \oplus (B + C + D)$



EX01	0.5 L/B cell	3-INPUT OR-EXOR			
	S	P	H		
Tpd A->Y	1.3	1.3	1.1		ns
B,C,D->Y	2.0	2.0	1.6		ns
I	1.05	1.55	1.85		mA
FANOUT LOAD LIMIT:	6	9	9		

$Y = A \oplus (B + C + D)$



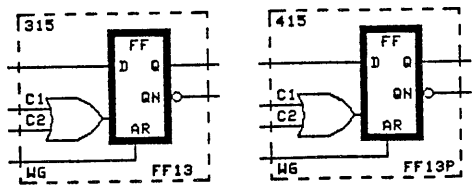
AMCC Q1500/QH1500 MACRO SUMMARY - FFxx

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES T_A = 25°C
I = I_{CC} FOR SINGLE +5V POWER SUPPLY, ELSE I = I_{EE}

FF13	L/B cell	D-F/F WITH ASYNC RESET GATED CLOCK, RISING EDGE TRIGGERED	
	S	P	H
Tpd C->Q,QN	2.0	2.0	ns
AR->Q,QN	3.4	3.4	ns
PW(C1,C2)	4.0	4.0	ns min
PW(AR)	6.0	6.0	ns min
Tsu	2.0	2.0	ns min
Th	0.7	0.7	ns min
T_{REC}	3.0	3.0	ns min
I	3.15	4.15	mA
FANOUT LOAD LIMIT:	6	9	

D	C1	C2	AR	Q_{n+1}	QN_{n+1}
X	0	0	0	Q_n	QN_n
X	X	1	0	Q_n	QN_n
X	1	X	0	Q_n	QN_n
1	_↑-	0	0	1	0
0	_↑-	0	0	0	1
1	0	_↑-	0	1	0
0	0	_↑-	0	0	1
X	X	X	1	0	1

_↑- = rising edge of clock



AMCC Q1500/QH1500 MACRO SUMMARY - MSxx

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES $T_A = 25^oC$
$I = I_{CC}$ FOR SINGLE +5V POWER SUPPLY, ELSE $I = I_{EE}$

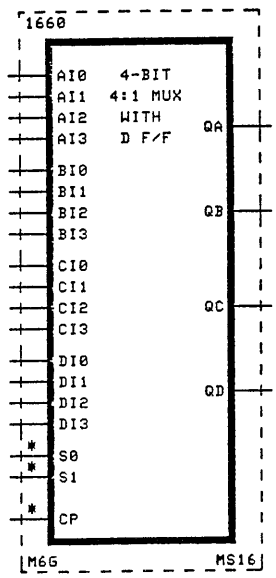
MS16 6 L/B cells 4-BIT 4:1 MUX WITH D F/F

	S	P	H	
Tpd CP->QA,QB,QC,QD	2.35			ns
Tsu DATA	2.5			ns min
Th DATA	-0.5			ns min
Tsu S0	3.6			ns min
Th S0	-1.6			ns min
Tsu S1	3.2			ns min
Th S1	-1.2			ns min
I	16.6			mA
FANOUT LOAD LIMIT:	6			
INTERCONNECT PINS:	47			

- UNIVERSAL REGISTER
* S0,S1,CP COUNT AS 2 LOADS

S1	S0	I
0	0	I0
0	1	I1
1	0	I2
1	1	I3

S1	S2	AI0	AI1	AI2	AI3	C	QA_{n+1}
0	0	0	X	X	X	_↑‾	0
0	0	1	X	X	X	_↑‾	1
0	1	X	0	X	X	_↑‾	0
0	1	X	1	X	X	_↑‾	1
1	0	X	X	0	X	_↑‾	0
1	0	X	X	1	X	_↑‾	1
1	1	X	X	X	0	_↑‾	0
1	1	X	X	X	1	_↑‾	1
X	X	X	X	X	X	0	QA_n



AMCC
APPLIED MICRO CIRCUITS CORPORATION

SAMPLE MACROS: Q3500 SERIES

- THE NEXT TWO PAGES SHOW PRELIMINARY DOCUMENTATION FOR 4 OF THE Q3500 MACROS TO SHOW THE S, LP, AND H OPTIONS

- EX02, EX02H, EX02L
- GT39, GT39H, GT39L
- LOW-POWER (L OPTION) NOT YET DEVELOPED ON DAISY, MENTOR, VALID LIBRARIES

THIS DATA IS PRELIMINARY

- MX01, FF14
  - Q3500 LIBRARY IS NOT DOWN-WARD COMPATIBLE

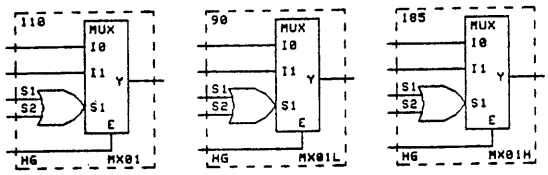
AMCC
APPLIED MICRO CIRCUITS CORPORATION

MX01 .5 L cell 2:1 MUX WITH GATED SELECT AND ENABLE

	S	LP	H	
Tpd I->Y	0.65	0.7	0.55	ns
S->Y	0.95	1.0	0.80	ns
E->Y	1.25	1.3	1.10	ns
I	1.10	0.9	1.85	mA

$Y = I1\ (S1 + S2)\ E + I0\ (\overline{S1 + S2})\ E$

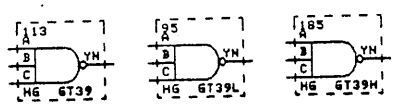
E	S1+S2	I0	I1	Y
0	X	X	X	0
1	0	0	X	0
1	0	1	X	1
1	1	X	0	0
1	1	X	1	1



GT39 .5 L cell 3-INPUT NAND

	S	LP	H	
Tpd A->YN	0.60	0.65	0.50	ns
B->YN	1.00	1.05	0.90	ns
C->YN	1.30	1.35	1.20	ns
I	1.13	0.95	1.85	mA

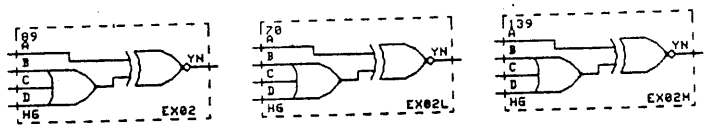
$YN = \overline{A.B.C} = \bar{A} + \bar{B} + \bar{C}$



EX02 .5 L cell 3-INPUT OR-EXNOR

	S	LP	H	
Tpd A->Y	0.60	0.65	0.55	ns
B,C,D->Y	0.90	0.95	0.80	ns
I	0.89	0.7	1.39	mA

$YN = \overline{A \oplus (B + C + D)}$

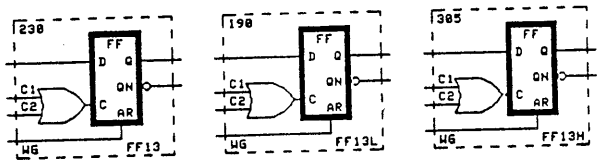


FF13 L cell D F/F WITH ASYNC RESET, GATED CLOCK

	S	LP	H	
Tpd C->Q,QN	1.20	1.25	0.98	ns
AR->Q,QN	1.00	1.05	0.75	ns
PW(C1,C2)	2			ns min
PW(AR)	2			ns min
Tsu	0.5			ns min
Th	0.0			ns min
I	2.30	1.90	3.05	mA

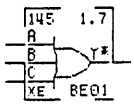
(same)

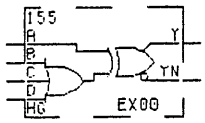
AR	D	C1+C2	Q_{n+1}	
0	DATA	0	Q_n	
0	DATA	1	DATA	
1	X	X	0	ASYNC. RESET

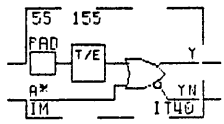


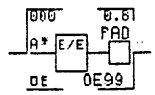
AMCC
APPLIED MICRO CIRCUITS CORPORATION

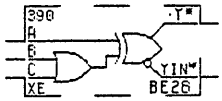
SAMPLE MENTOR GRAPHICS

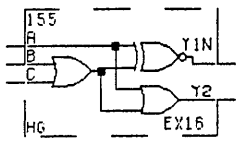


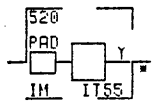


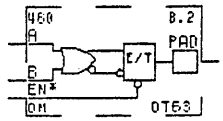


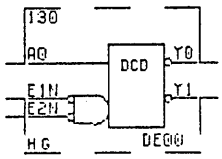


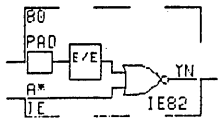


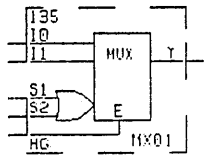


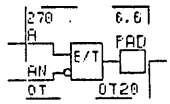


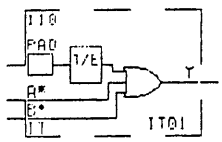


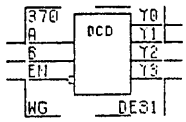












I/O MACROS

- I/O MACROS COVER
  - STANDARD REFERENCE VOLTAGE ECL
  - +5V REF ECL
  - ECL 10K
  - ECL 100K (QH1500 ARRAY, Q3500 SERIES)
  - TTL
- THE AMCC ARRAYS ALLOW MIXED MODE
  - ECL AND TTL BOTH ON THE SAME CHIP
  - +5V REF ECL - TTL MIXED
  - +5V REF ECL ALONE - FOR ECL FUNCTIONS ON A TTL BOARD

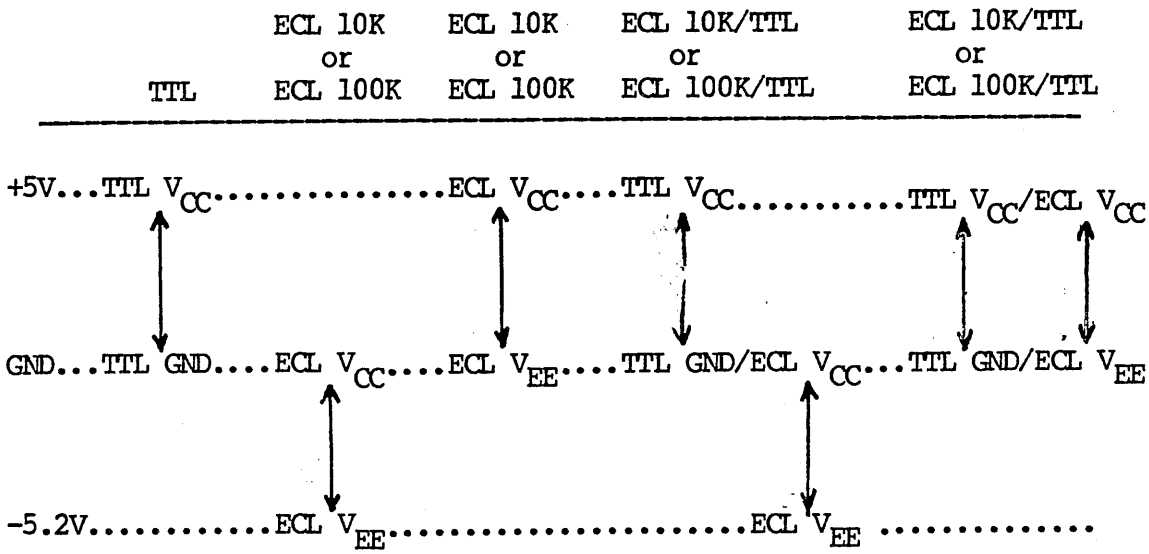
    OR INTER-CHIP COMMUNICATIONS ON THE SAME BOARD
  - ECL 10K AND 100K ON THE SAME CHIP (Q3500 SERIES)

- FOR EACH I/O MODE AND POWER SUPPLY CONFIGURATION, THE ARRAY PADS ARE CONNECTED AS FOLLOWS:

I/O MODE ARRAY PAD-->	TTL V_{CC}	TTL GND	ECL V_{CC}	ECL V_{EE}
TTL	+5V	+GND	+5V	+GND
ECL 10K or ECL 100K	-GND	-GND	-GND	-5.2V
ECL 10K or ECL 100K	+5V	+5V	+5V	+GND
ECL 10K/TTL or ECL 100K/TTL	+5V	+GND	+5V	+GND
ECL 10K/TTL or ECL 100K/TTL	+5V	+GND	-GND	-5.2V

POWER SUPPLY OPTIONS

	SINGLE POWER SUPPLY +5V	-5.2V	-4.5V	DUAL POWER SUPPLY +5V/-5.2V	+5V/-4.5V
100% TTL	•	-	-	-	-
100% ECL 10K	•	•	-	-	-
100% ECL 100K	•	•	•	-	-
ECL 10K/TTL	•	-	-	•	-
ECL 100K/TTL	•	-	-	•	•



- NOTE: +GND IS THE +5V RETURN
- -GND IS THE -5.2V RETURN

- TTL SINGLE CELL OUTPUT OPTIONS ARE:
  (AVAILABLE ON ALL ARRAYS)

    - TOTEM-POLE OUTPUT
    - OPEN-COLLECTOR
    - 3-STATE
    - TRANSCEIVER (ALL EXCEPT Q1500)
      (ON THE Q1500, USE I AND O CELL-PAIR TOGETHER)

- ECL TERMINATIONS AVAILABLE ARE:
  - 50 ohm (ALL ARRAYS)
  - 100 ohm (Q1500 ONLY)**
  - 200 ohm (Q700, Q1500 ONLY)**
  - USE 50 ohm TERMINATION TO HANDLE 100 ohm, 200 ohm TERMINATIONS WHERE SPECIFIC MACROS FOR THESE CASES ARE NOT AVAILABLE

ECL OUTPUT BUFFER LIMITATION

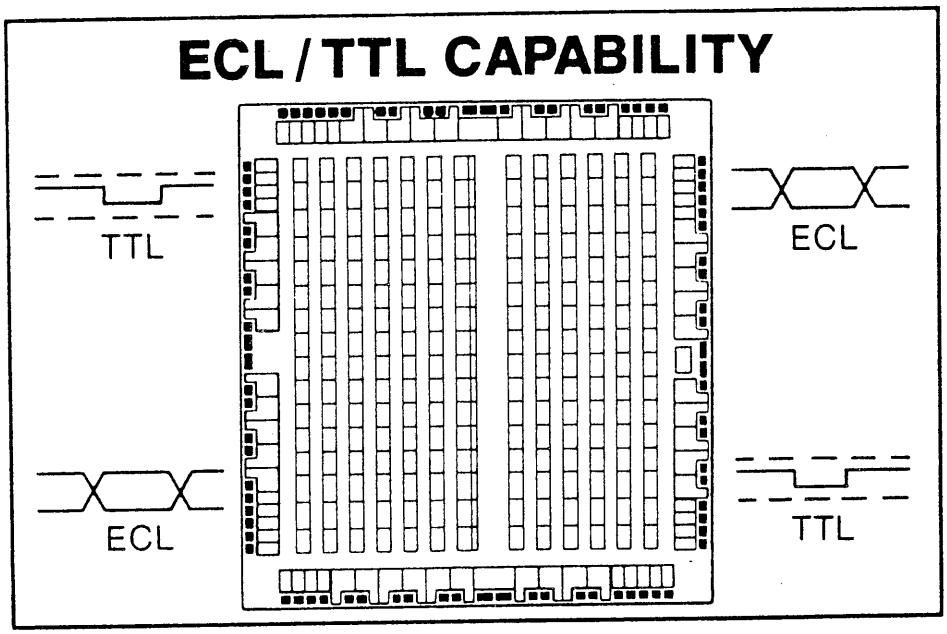
The type of ECL termination selected determines the number that will be allowed. ECL output buffers MUST be placed on buffer cells. QH1500A and the Q3500 series ECL buffers are part of the ECL output macros.

ECL OUTPUT BUFFER LIMITATON

Array Series	Array Series	ECL Output Buffers 50	100	200
Q700	Q700	26	-	38*
	Q710	20	-	28*
	Q720	14	-	26*
Q1500	Q1500A	32	38*	38*
	QH1500A		N/A	
Q3500	any		N/A	

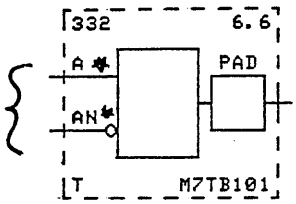
Limited either by # of B cells or # of output cells

- USE CARE WHEN SELECTING MACROS!!!

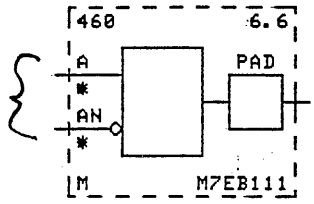


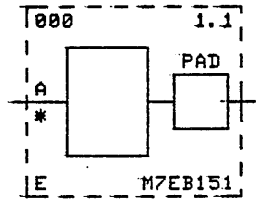
- PIN-RESTRICTIONS ARE MARKED ON THE EWS GRAPHIC BY AN ASTERISK (*)
- AMCC ERC SOFTWARE PERFORMS PIN HOOK-UP CHECK TO CATCH VIOLATIONS
- TAKE THE TIME EARLY IN THE DESIGN TO STUDY THE LIBRARY AND THE PORTIONS OF THE MACRO LIBRARY THAT WILL BE USED

AMCC
APPLIED MICRO CIRCUITS CORPORATION

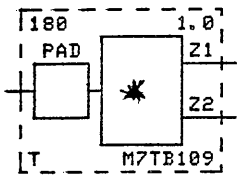


TTL OUTPUT

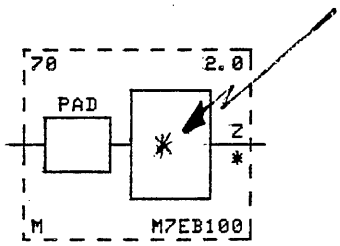




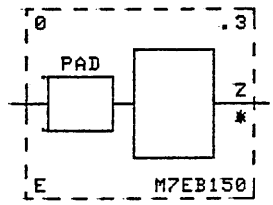
ECL OUTPUT



TTL INPUT TTL

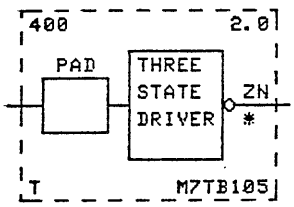


TTL MIX

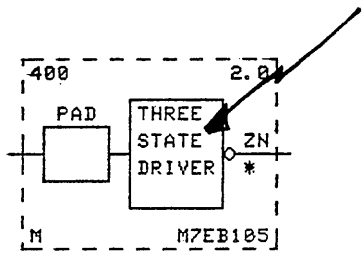


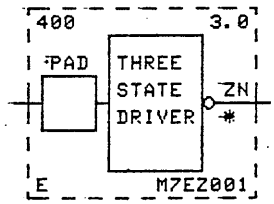
ECL INPUT

ECL

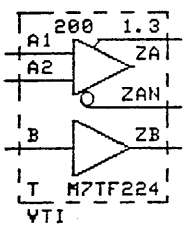


THREE STATE DRIVER

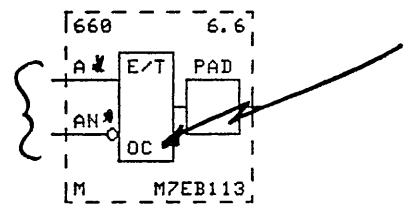




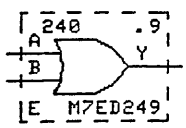
D CELL DRIVER



TTL INPUT BUFFER



TTL OPEN COLLECTOR OUTPUT



DRIVER BUFFER

SPECIFICATION CHANGES

The Q700 LATCH macros have been changed so that the Tsu and Th specifications are worst-case MINIMUM and not typical. They DO NOT get multiplied in either the path delay computation or in the external set-up and hold time computation.

LATCH MACRO:	Tsu	Th	T_{REC} (AR)	Units
M7EF700	2.0	0.7		ns min
M7EF701	2.0	0.7		ns min
M7EF720	2.0	0.7	3.0	ns min
M7EF730	2.0	0.7	3.0	ns min
M7EF731	2.0	0.7		ns min

T_{REC} has been added to those macros with a RESET. T_{REC} is the length of time between the removal of a reset signal and the resumption of normal clock behavior.

	TTL INPUT MACROS:	Tpd+	Tpd-		
TTL	M7TB104	2.1	0.5	ns TYP	
	M7TB105	2.1	0.5	ns TYP	
	M7TI107	1.0	0.4	ns TYP	
	M7TB107	1.0	0.4	ns TYP	
	M7TB108	2.1	0.5	ns TYP	
	M7TI108	2.1	0.5	ns TYP	
	M7TB109	1.0	0.4	ns TYP	
	M7TI109	1.0	0.4	ns TYP	
	M7TB110	2.1	0.5	ns TYP	
	M7TI110	2.1	0.5	ns TYP	
	M7TZ001	4.0	2.0	ns TYP	
TTLMIX	M7EB100	2.1	0.5	ns TYP	
	M7EI100	2.1	0.5	ns TYP	
	M7EB105	2.1	0.5	ns TYP	
	M7EB114	2.1	0.5	ns TYP	INPUT ONLY
	M7EZ001	4.0	2.0	ns TYP	

All of the TTL input translator macros use 2.0 (Commercial) and 2.5 (Military) worst-case multipliers for propagation delay (path delay or set-up and hold time computations).

AMCC
APPLIED MICRO CIRCUITS CORPORATION

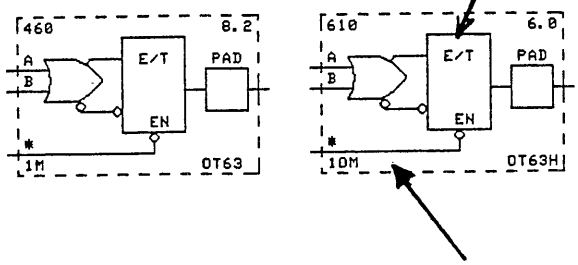
AMCC Q1500 MACRO SUMMARY - TTL MIX — Q1500 TTLMIX
FOR TTL I/O IN STD ECL/TTL MIXED MODE CIRCUITS
DUAL POWER SUPPLIES: +5V, -5.2V
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES $T_A = 25^oC$

OT63	O cell	TTL 3-STATE OUTPUT WITH OR BUFFER		
	S	P	H	
Tpd A,B->PAD	8.2		6.0	ns
TPLZ	9.0		9.0	ns
TPHZ	6.0		6.0	ns
TPZH	6.0		6.0	ns
TPZL	9.0		9.0	ns
I_{CC} HIGH	3.4		4.35	mA
I_{CC} LOW	3.8		4.95	mA
I_{CC} HI-Z	4.6		6.1	mA

* EN FROM IT58 OR OT57 ←

$PAD = (A + B) \cdot \overline{EN}$

A	B	EN	PAD
X	1	0	1
1	X	0	1
0	0	0	0
X	X	1	HIGH-Z



AMCC Q1500 MACRO SUMMARY - TTL LIB
FOR TTL I/O IN 100% TTL OR +5V REF ECL/TTL MIXED MODE
SINGLE POWER SUPPLY: +5V
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES $T_A = 25^oC$

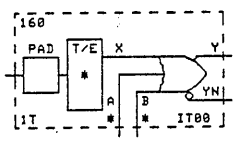
IT00	I cell	TTL INPUT WITH OR/NOR BUFFER		
	S	P	H	
Tpd+ PAD->X	1.6		1.0	ns
Tpd- PAD->X	0.5		0.4	ns
Tpd X,A,B->Y,YN	1.3		1.3	ns
I_{CC}	1.6		3.6	mA
I_{IL}	0.4		2.4	mA
FANOUT LOAD LIMIT:	6		6	

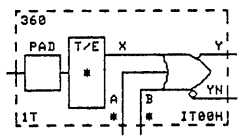
- USE WORST CASE PROPAGATION DELAY MULTIPLIERS 2.0 (COMMERCIAL) AND 2.5 (MILITARY) FOR Tpd+ AND Tpd-; 1.5 AND 1.6 FOR Tpd BUFFER
- BOTH THE RISING EDGE AND THE FALLING EDGE PROPAGATION MUST BE COMPUTED

* A,B FROM IT05 UNBUFFERED INPUT MACROS

$$Y = A + B + PAD$$

$$YN = \overline{A} \cdot \overline{B} \cdot \overline{PAD}$$



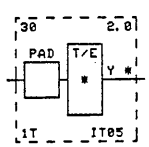


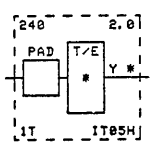
IT05	I cell	UNBUFFERED TTL INPUT		
	S	P	H	
Tpd+ PAD->Y	2.1		1.0	ns
Tpd- PAD->Y	0.5		0.4	ns
I_{CC}	0.3		2.4	mA
I_{IL}	0.4		2.4	mA
FANOUT LOAD LIMIT:	1		1	

- USE WORST CASE PROPAGATION DELAY MULTIPLIERS 2.0 (COMMERCIAL) AND 2.5 (MILITARY)
- BOTH THE RISING EDGE AND THE FALLING EDGE PROPAGATION MUST BE COMPUTED

* TO IT00, IT01, IT02 A OR B INPUT ONLY

$$Y = PAD$$





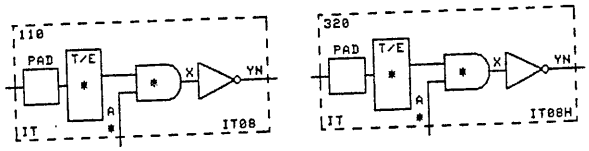
AMCC Q1500 MACRO SUMMARY - TTL LIB
FOR TTL I/O IN 100% TTL OR +5V REF ECL/TTL MIXED MODE
SINGLE POWER SUPPLY: +5V
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES $T_A = 25^oC$

IT08	I cell	TTL INPUT WITH NAND BUFFER		
	S	P	H	
Tpd+ PAD->X	1.6		1.0	ns
Tpd- PAD->X	0.5		0.4	ns
Tpd+ A->X	1.4		0.8	ns
Tpd- A->X	0.3		0.2	ns
Tpd X->YN	1.3		1.3	ns
I_{CC}	1.1		3.2	mA
I_{IL}	0.4		2.4	mA
FANOUT LOAD LIMIT:	6		6	

- USE WORST CASE PROPAGATION DELAY MULTIPLIERS 2.0 (COMMERCIAL) AND 2.5 (MILITARY) FOR Tpd+ AND Tpd-; 1.5 AND 1.6 FOR Tpd BUFFER
- BOTH THE RISING EDGE AND THE FALLING EDGE PROPAGATION MUST BE COMPUTED

* A FROM IT10 UNBUFFERED INPUT ONLY

$$YN = \overline{A \cdot PAD}$$

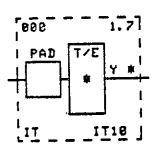


IT10	I cell	TTL INPUT		
	S	P	H	
Tpd PAD->Y	0.2			ns
I_{CC}	0.0			mA
I_{IL}	SAME AS I_{IL} OF MACRO BEING DRIVEN			
FANOUT LOAD LIMIT:	1			

- USE WORST CASE PROPAGATION DELAY MULTIPLIERS 2.0 (COMMERCIAL) AND 2.5 (MILITARY)
- BOTH THE RISING EDGE AND THE FALLING EDGE PROPAGATION MUST BE COMPUTED FOR THIS PATH

* TO IT06,IT07,IT08 A INPUTS ONLY

$$Y = PAD$$



Q1500/Q3500 SERIES FEATURE

ECL INPUT

For ECL input, the output of the RC compensation network provided by the input portion of the macro is buffered by either a buffer on the input macro or by the BIxx ECL input buffered-logic macros. ECL inputs function in the same manner on circuits which have +5V referenced ECL input with a single +5V power supply. Refer to the macro summary for restrictions in input and buffer macro pairing for the Q1500 series arrays.

BIXX SERIES BUFFERED-LOGIC MACROS

For ECL input, there is the option of the BIXX series buffered logic macros which offer most of the functions offered by the other internal logic macros and which also provide ECL input buffering. These macros have specific inputs which must be connected to the IE85 (Q1500A, QH1500A standard reference ECL) or IP85 (QH1500A, +5V REF ECL) unbuffered ECL input macros. They must also be connected to the VTA threshold generator (macro VT00).

IE85 (IP85) has a fanout of 8 and the distinction that there is no propagation delay penalty for the fanout. The use of the IE85/IP85 and BIXX macro combination will usually provide a denser and a faster design. The BIXX macros are part of the shared logic portion of the library and are listed in the internal logic section in Appendix A.

ECL INPUT

APPLIED MICRO CIRCUITS CORPORATION

IEnn - BInn-VTA

VTA GENERATOR USAGE ON THE Q1500 SERIES ARRAYS

(The Q3500 series will also have a specification for this generator.)

The BIXX buffer-logic macros combinea logic function with the ECL input buffer function to eliminate the delay normally associated with a dedicated buffer. These high-performance macros have some or all of their input pins restricted to be driven from the IE85 (IP85) ECL unbuffered input macro. The fanout of the IE85 macros is limited to 8 loads. The fanout loading has no affect on the path propagation delay. This is the only instance of this variation on Tpd computation.

The loading presented at the package pin is equivalent to the loading on IE85 (IP85). Input pin loading should be taken into consideration in the input current specification and when setting the test limits.

The majority of the BIXX macros require pin-connect to the VTA threshold gnerator. Unlike the VT2, etc. of the Q700, where the pins are counted but not visible on the schematic, the VTA generator is called up as the VT00 macro and the BIXX macros are connected to it by the circuit designer (treated as any other macro pin).

One VT00 macro is used to fanout to all VTA input pins for a Q1500A design. Two VT00 macros, wire-ORed together, are used to fanout to all VTA input pins for a QH1500A design. The Q3500 series VTA will have another procedure. TBS.

AMCC QH1500 MACRO SUMMARY - ECL LIB
FOR ECL IN 100% ECL OR ECL/TTL MIXED MODE

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES $T_A = 25^oC$

Ix85 I or I/O cell ECL INPUT COMPENSATOR (UNBUFFERED)

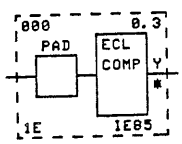
	S	P	H	
Tpd PAD->Y	0.3			ns
I_{EE}	0.0			mA
FANOUT LOAD LIMIT:	8			

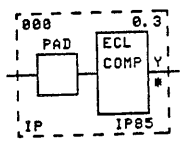
---

* FOR +5V CIRCUIT: TO IP90 OR BInn SERIES
* FOR -5.2V CIRCUIT: TO IE90, IE81, IE82 OR BInn SERIES

Y = PAD

Power Supply:	Macro:
ECL 10K/100K -5.2V	IE85
ECL 10K/100K +5V	IP85





AMCC Q1500/QH1500 MACRO SUMMARY - BIXX
FOR ANY ECL I/O MODE

ECL INPUT BUFFERS

ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES $T_A = 25^{\circ}$

BI46	B/L cell	S	P	H	TRIPLE 2:1 MUX WITH COMMON SELECT
Tpd S1->Y		1.9	1.9		ns
A0,A1,B0,B1,C0,C1->Y		1.2	1.2		ns
I_{EE}		2.9	4.4		mA
FANOUT LOAD LIMIT:		6	9		

* A0,A1,B0,B1,C0,C1,S1 FROM UNBUFFERED INPUT MACRO IE85 or IP85

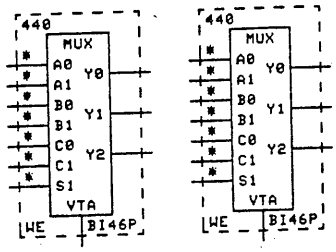
$$Y0 = [\overline{S1} \cdot A0 + S1 \cdot A1] + \overline{VTA}$$
$$Y1 = [\overline{S1} \cdot B0 + S1 \cdot B1] + \overline{VTA}$$
$$Y2 = [\overline{S1} \cdot C0 + S1 \cdot C1] + \overline{VTA}$$

PRELIMINARY

VTA	S1	A0	A1	Y0
0	X	X	X	1
1	0	0	X	0
1	0	1	X	1
1	1	X	0	0
1	1	X	1	1

VTA	S1	B0	B1	Y1
0	X	X	X	1
1	0	0	X	0
1	0	1	X	1
1	1	X	0	0
1	1	X	1	1

VTA	S1	C0	C1	Y2
0	X	X	X	1
1	0	0	X	0
1	0	1	X	1
1	1	X	0	0
1	1	X	1	1



AMCC
APPLIED MICRO CIRCUITS CORPORATION

THE ARRAYS

CHAP 3 - THE ARRAYS THEMSELVES
Device Architecture - Die plot, L,B cells
- Q700
- Q1500
- Q3500

Resource Summary:
Internal Resources
Maximum Cell Utilization Guideline
Maximum Current Specification
I/O Resources
- Basic
- By Mode
- Q700
- Q1500
  - o Q1500/QH1500 power/ground interconnect

Extra Power/Ground - when?
- Q700 Series
- Q1500A array only
- Q3500 Series

VTI Load Limit

DEVICE ARCHITECTURE

AMCC semicustom logic arrays are formed from a customer-specified design added to an AMCC designed preprocessed silicon base array. The base array for the Q7ØØ series is composed of five types of cells:

Cell Type	Location
Logic (L)	internal
Buffered logic (B)	internal
Input (I)	perimeter
Input/Output (I/O)	perimeter
3-State Driver (D)	perimeter*

Each cell consists of a number of uncommitted transistors and resistors, with each cell type designed to support specific high-speed requirements. No power is used by a cell in its base configuration.

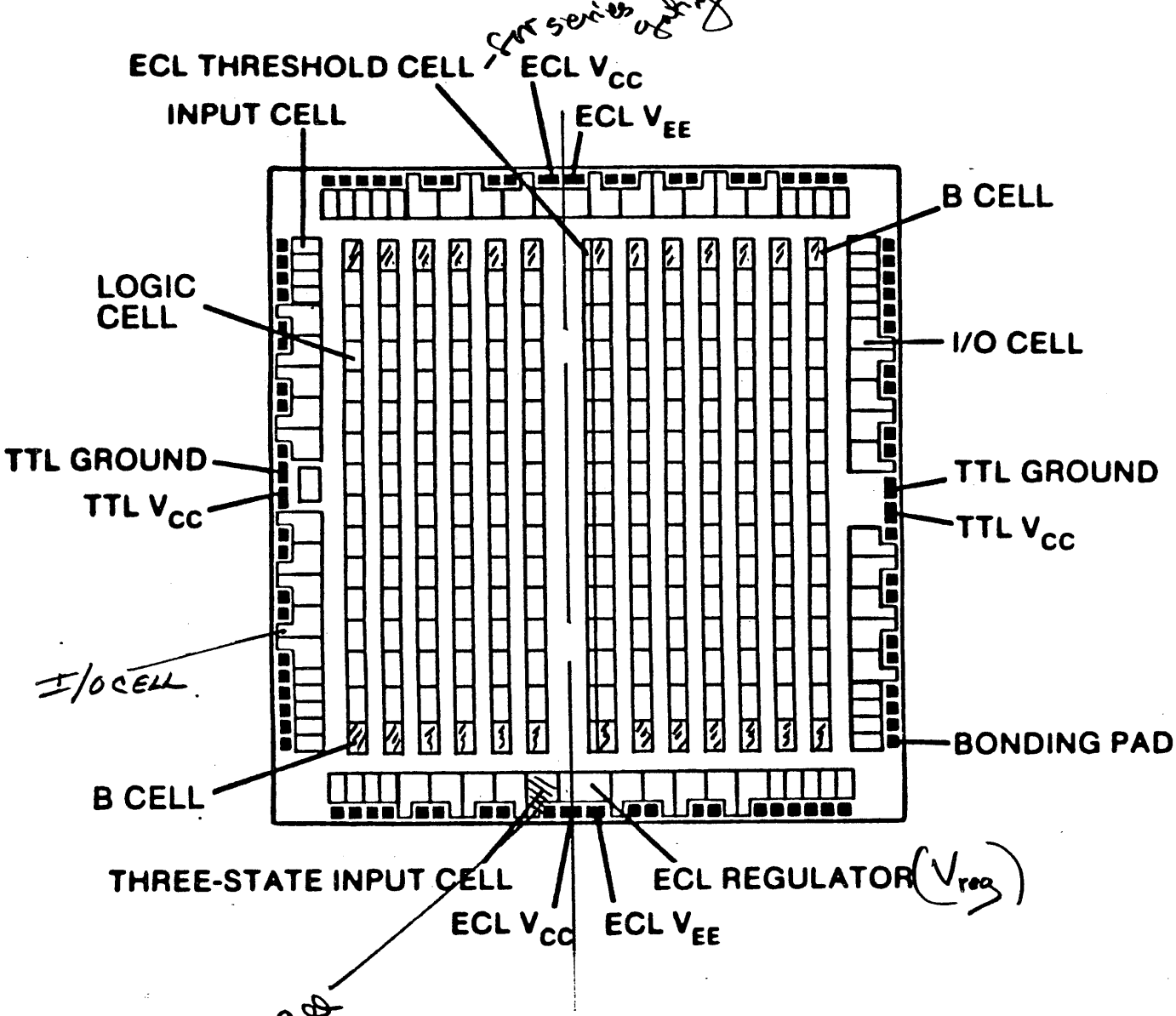
Array Series	Array Name	Buffer Cells	Logic Cells
Q700	Q700	26	182
	Q710	20	100
	Q720	14	42

Array Series	Array Name	Input Cells	Output Cells	I/O Cells
Q700	Q700	38		38
	Q710	28		28
	Q720	8		26

- REFER TO THE Q700 DATA SHEET.....
  - THE Q700 ARRAY DIE LAYOUTS
  - ARRAY IS ARRANGED WITH I/O ON THE PERIPHERY (I/O CELLS)
  - TTL POWER AND GROUND ON THE RIGHT AND THE LEFT (FORM MIRROR IMAGE "C"s)
  - ECL POWER GROUND ON THE TOP AND THE BOTTOM
  - SOME CELLS ARE INPUT-ONLY (I-CELLS)
  - TWO SPECIAL (Q700 ONLY) CELLS AT THE BOTTOM ARE 3-STATE ENABLE-DRIVERS (D Cells)
  - BUFFER (B) CELLS ARE ACROSS THE TOP ROW OF THE INTERNAL ARRAY
  - INTERNAL LOGIC (L) CELLS ARE THE BULK OF THE ARRAY
  - LOGICAL OPERATIONS ARE PERFORMED IN EITHER L OR B CELLS
    - THE INDIVIDUAL MACRO DOCUMENTS WHERE IT CAN BE PLACED

AMCC
APPLIED MICRO CIRCUITS CORPORATION

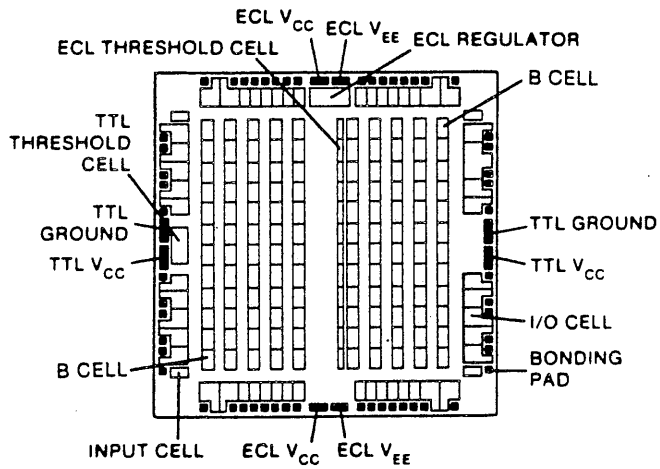
Q700 DIE ORGANIZATION



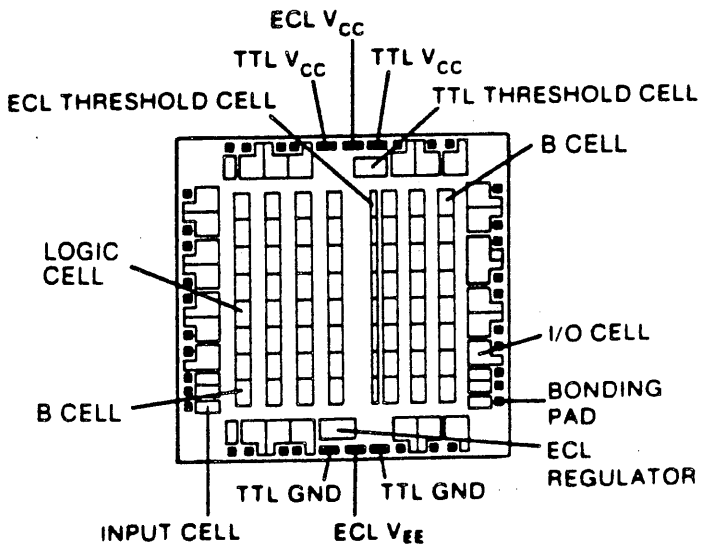
Q700 — Die Size 236 Mils x 243 Mils

- REFER TO THE DATA SHEET FOR THE Q710, Q720 DIE LAYOUTS (CHIP PLANS)
  - THE ARRANGEMENTS ARE SIMILIAR
  - NO DRIVER (D) CELLS ON THE Q710 OR Q720
  - THE ARRAYS ARE SMALLER

Q710 — Die Size 195 mils x 197 Mils



Q720 — Die Size 152 Mils x 148 Mils



DEVICE ARCHITECTURE

The AMCC logic arrays are formed from a customer-specified design added to an AMCC pre-processed silicon base array.

Q1500A ARRAY

The base array for the Q1500A array is composed of four types of cells:

TABLE 2
Q1500A ARRAY CELL TYPES

Cell Type	Location	Quantity
Logic (L)	internal	112
Buffer (B)	internal	16
Input only (I)	perimeter	46
Output only (O)	perimeter	38

QH1500A ARRAY

The base array for the QH1500A array is composed of three types of cells:

TABLE 3
QH1500A ARRAY CELL TYPES

Cell Type	Location	Quantity
Logic (L)	internal	136
Input only (I)	perimeter	60
Input/Output (I/O)	perimeter	60

- REFER TO THE Q1500/QH1500 DATA SHEET.....

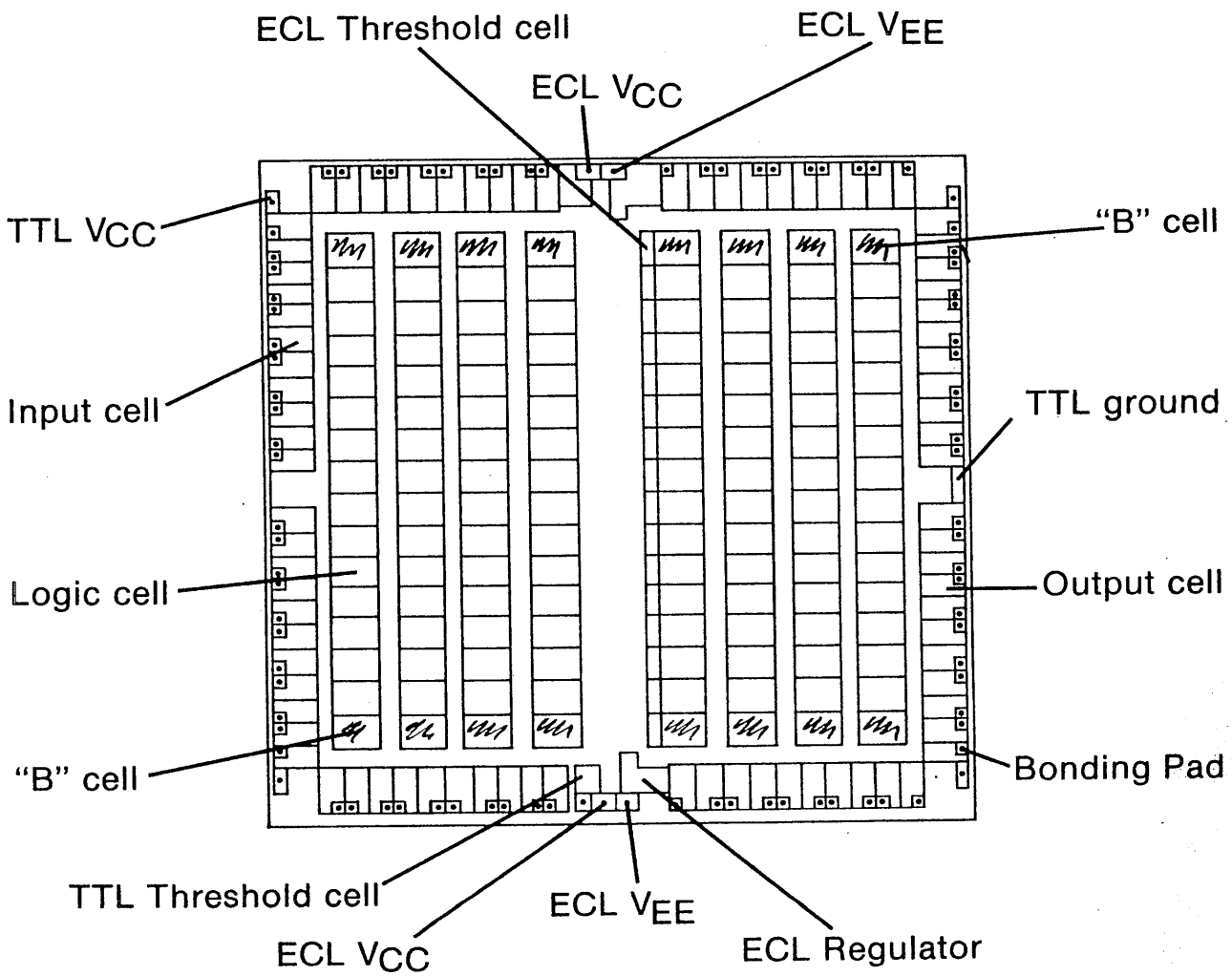
  Q1500 ONLY:

  - THE ARRANGEMENT AGAIN PLACES I/O AROUND THE PERIPHERY
  - NOTE THE DISTRIBUTION OF POWER AND GROUND
  - BUFFER CELLS ARE AGAIN AT THE TOP AND BOTTOM
  - THE Q1500 USES INPUT-ONLY (I) CELLS
  - THE Q1500 USES OUTPUT-ONLY (O) CELLS
  - LOGIC CELLS ARE IN THE CENTER
  - THE LOGIC CELL ON THE Q1500/QH1500 IS TWICE AS LARGE AS THAT FOR THE Q700 SERIES - INTENDED FOR THOSE APPLICATIONS WHICH NEED THE MORE COMPLEX LOGIC FUNCTIONS AND HIGH DENSITY

AMCC
APPLIED MICRO CIRCUITS CORPORATION

Q1500A DIE ORGANIZATION

Die Size 269 mils x 257 mils



- REFER TO THE Q1500/QH1500 DATA SHEET.....

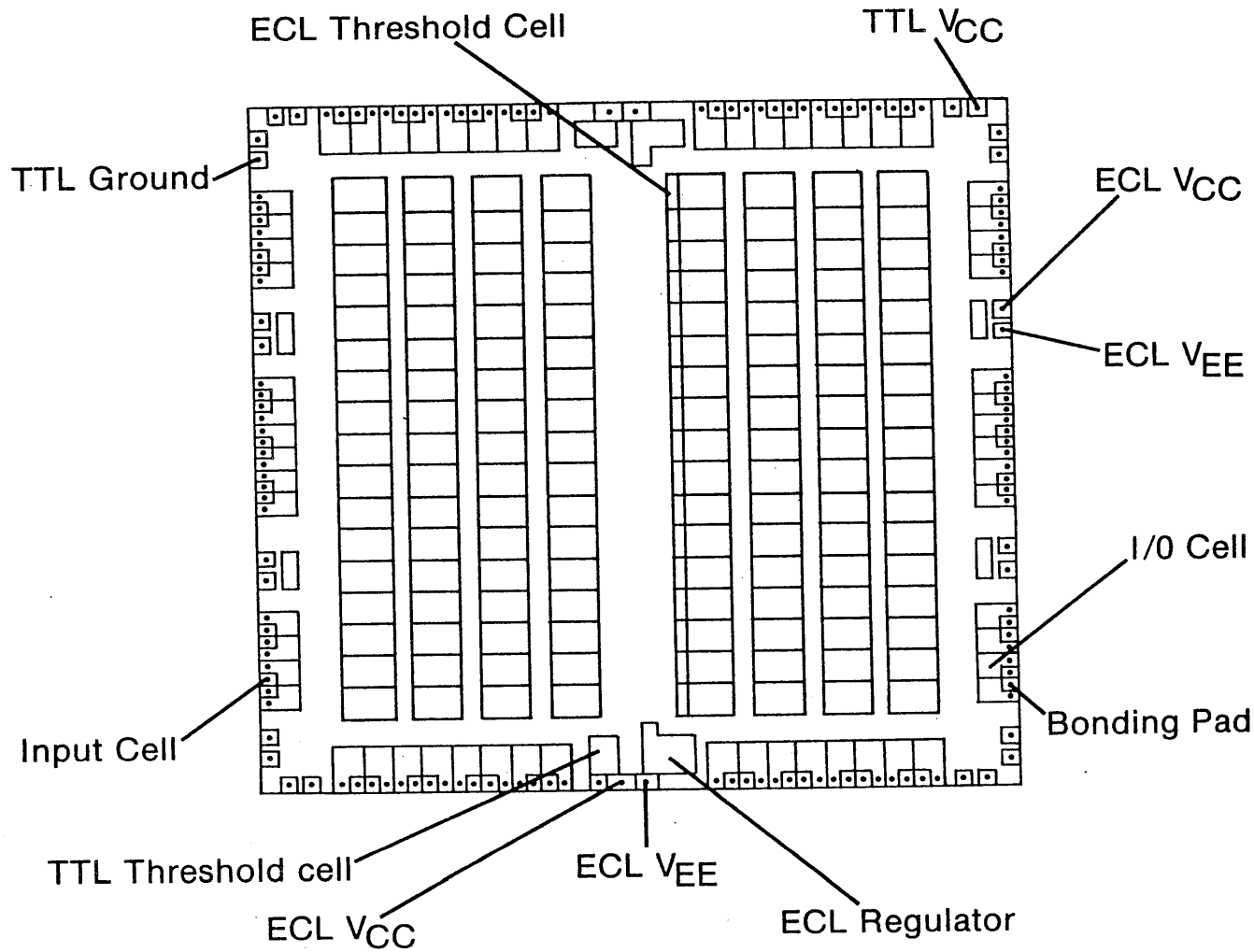
  QH1500 ONLY

  - THE MOST NOTABLE DIFFERENCE IS THAT THE QH1500 USES NO BUFFER CELLS per se
  - THE QH1500 USES A DIFFERENT SET OF I/O MACROS - BUFFERING IS INCLUDED
  - THE QH1500 USES INPUT-ONLY CELLS
  - THE QH1500 USES INPUT/OUTPUT CELLS
  - POWER IS DISTRIBUTED AROUND THE PERIPHERY SIMILIAR TO THE Q1500
    - TTL AT THE CORNERS
    - ECL AT THE MIDDLE OF EACH EDGE

AMCC
APPLIED MICRO CIRCUITS CORPORATION

QH1500A DIE ORGANIZATION

Die Size 305 mils x 305 mils



AMCC
APPLIED MICRO CIRCUITS CORPORATION

DEVICE ARCHITECTURE

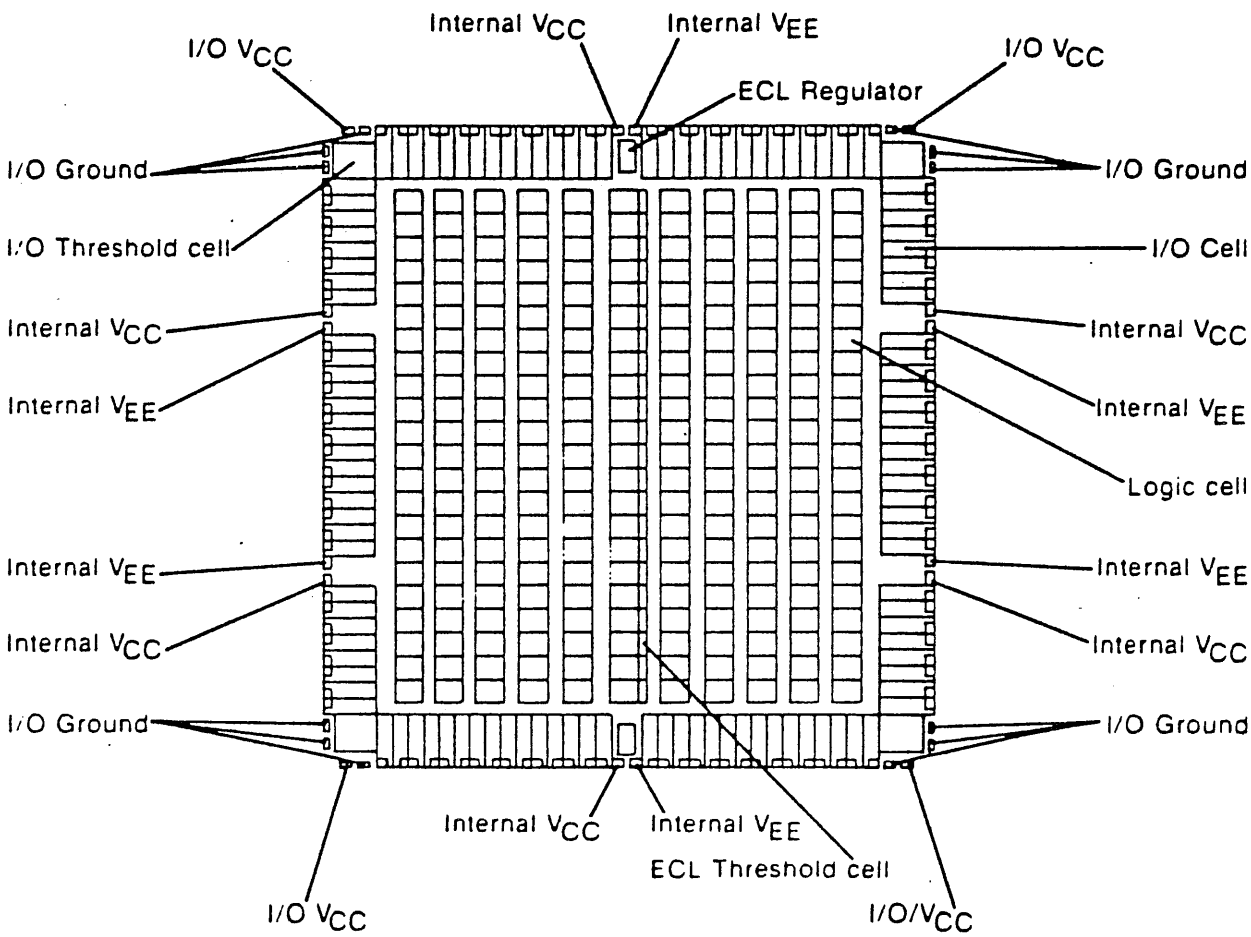
The AMCC logic arrays are formed from a customer-specified design added to an AMCC pre-processed silicon base array. The base array for the Q3500 series is composed of two types of cells:

Cell Type	Location	Number of: Q3500S	Q2400S	QM1600S	Q1300S
Logic (L)	internal	242	153	110	84
Input/Output (I/O)	perimeter	120	98	104	80

Each cell consists of a number of uncommitted transistors and resistors, with each cell type designed to support high-speed requirements. No power is used by a cell in its base configuration.

Q3500 SERIES BIPOLAR GATE ARRAYS

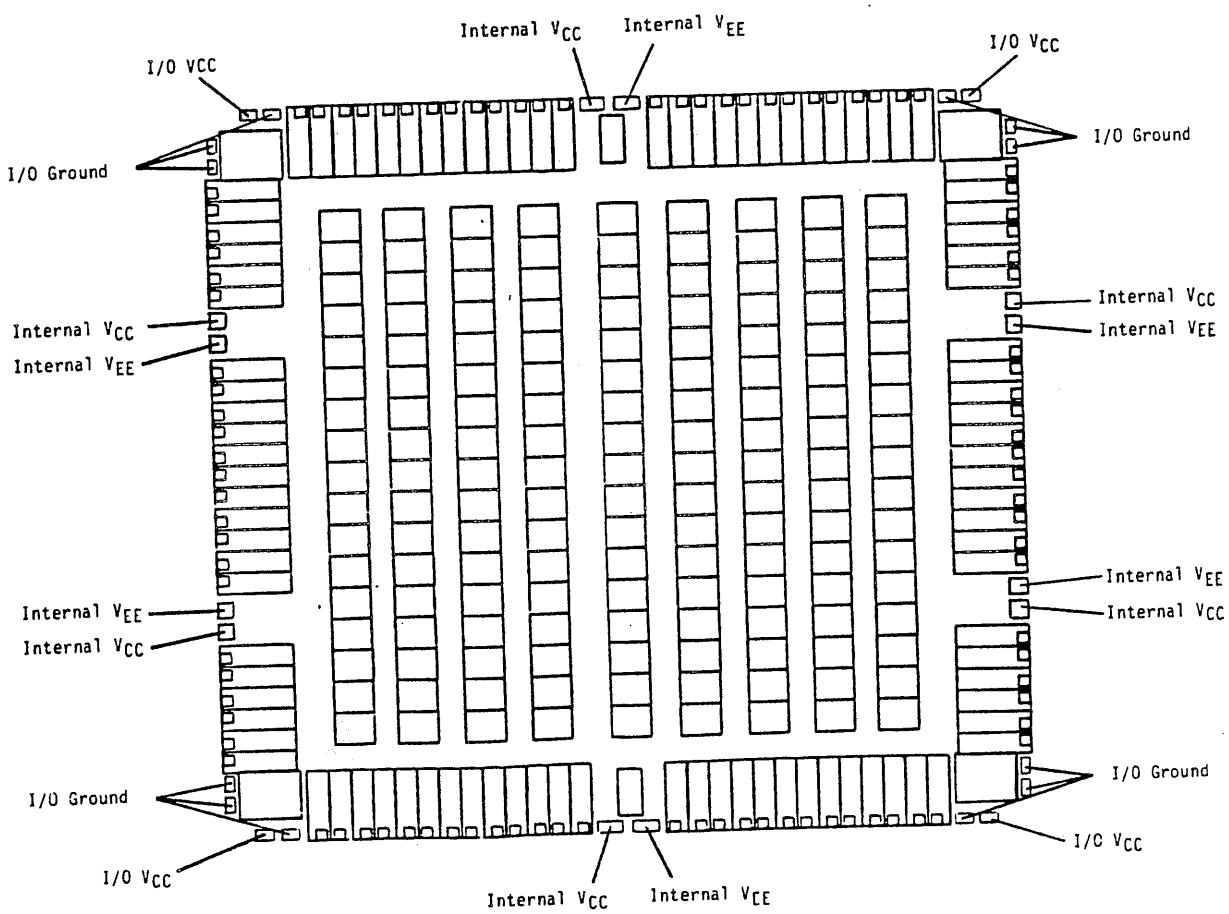
Q3500S



DIE SIZE: 350 MILS X 350 MILS

Q3500 SERIES BIPOLAR GATE ARRAYS

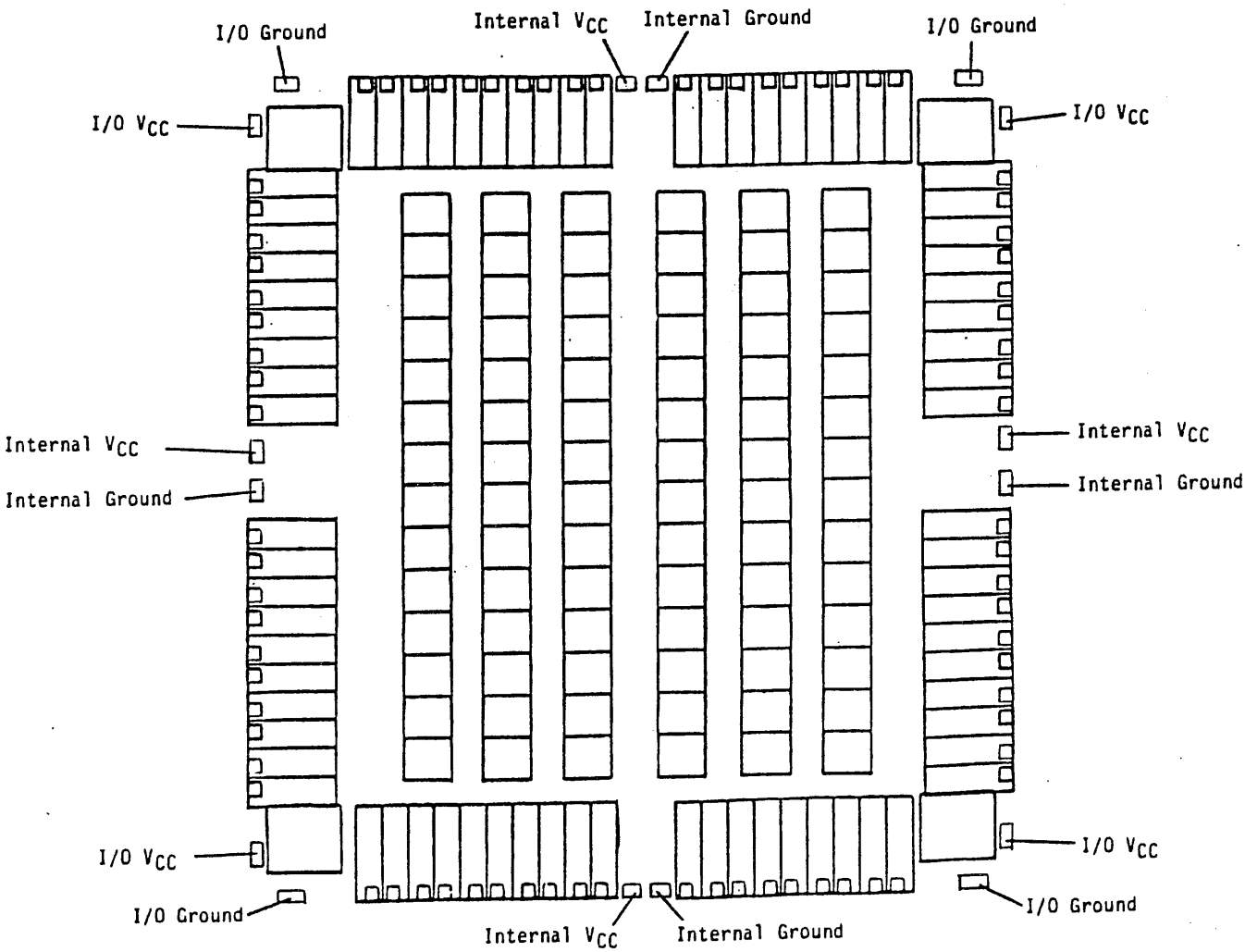
Q2400S



DIE SIZE: 291 MILS X 270 MILS

Q3500 SERIES BIPOLAR GATE ARRAYS

Q1300S

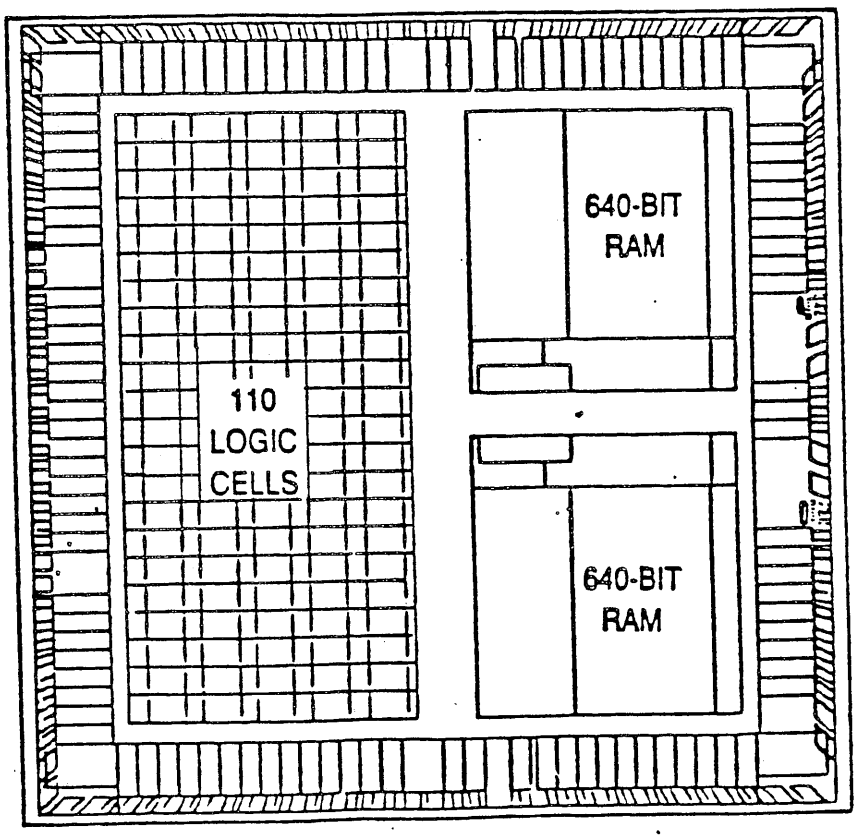


DIE SIZE: 230 MILS X 230 MILS

AMCC
APPLIED MICRO CIRCUITS CORPORATION

QM1600S

PRELIMINARY



DIE SIZE 305 MILS X 322 MILS

RESOURCE SUMMARY

INTERNAL RESOURCES

In selecting an array, one of the first considerations is the number and type of internal cells and the number and modes of I/O cells available. This could be the limiting factor in the decision between arrays within a series or between the array series themselves.

INTERNAL RESOURCES

The internal matrix area of the arrays is restricted to buffer (B) and logic (L) cells.

INTERNAL ARRAY CELL RESOURCE SUMMARY

Array Series	Array Name	Buffer Cells	Logic Cells
Q700	Q700	26	182
	Q710	20	100
	Q720	14	42
Q1500	Q1500A	16*	112
	QH1500A	-*	136
Q3500	Q3500S	-	242
	Q2400S	- **	153
	QM1600S	-	110
	Q1300S	-	84

* QH1500A and up contain buffering in the I/O macros

** QM1600S also uses 1280 bits RAM in the internal matrix

QUESTION: UTILIZATION - WHAT IS AVAILABLE?
OR - WHAT IS THE UTILIZATION LIMIT
BEFORE IT CANNOT BE AUTOMATICALLY ROUTED?

OR BEFORE ROUTING BECOMES A PROBLEM...

MAXIMUM CELL UTILIZATION

Cell utilization is a means of estimating the feasibility of a design on a given array. The specified limit is designed to quarentee that designs meeting the restrictions are routable designs and that the array in question ca be built. The utilization refers to the internal array matrix (L and B cells) only. The limits for the three array series are given below.

CELL UTILIZATION LIMITS

Array Series:	%
Q700	85
Q1500	95
Q3500	95

GUIDELINE

MAXIMUM CURRENT SPECIFICATION - INTERNAL CELLS

The Q700, Q1500 and Q3500 series arrays all provide either power (P) options or high-speed (H) options on many of their I/O and internal logic macros. These arrays have a maximum current specifictions for the internal matrix (L and B cell area).

MAXIMUM INTERNAL CURRENT SPECIFICATION

Array:	Maximum Current (mA)	
Q700	-TBS-	
Q720	-TBS-	**NO LIMIT**
Q710	-TBS-	
Q1500S	600	
QH1500S	630	
Q3500A	788	*1.4 To match Q1500 spec
Q2400A	612	
QM1600A	352	
Q1300A	378	

MAXIMUM CURRENT SPECIFICATION - BY ROW

If preplacement is being done external to AMCC, then the designer needs to be aware of the restrictions on macro placement. One of these is the maximum row current, derived from the maximum internal current on the previous page.

MAXIMUM INTERNAL CURRENT SPECIFICATION

Array:	Maximum Row Current (mA)
Q700	-TBS-
Q720	-TBS- } no limit
Q710	-TBS- no restrictions
Q1500A *	30
	90 Rows 1, 16
QH1500A *	30
	90 Rows 1, 17
Q3500S	36 30% H
Q2400S	36 40% H
QM1600S	16 30% H
Q1300S	-TBS- can be 100% H option

This is the basis of the 30% H/P option guideline given to designers.

* FOR 1/2 ROW: USE 0.6 * ROW LIMIT FOR THE Q1500 SERIES

I/O RESOURCES

The flexible I/O of the AMCC logic arrays allows a broad selection of mode. TTL, TTL/ECL 10K, TTL/ECL 100K, +5V REF ECL, +5V REF ECL/TTL are among the modes supported (consult the individual design guides). TTL totem pole, open-collector and three-stated outputs are also supported as are ECL terminations of 50ohms, 100ohms and 200 ohms.

I/O CELL RESOURCE SUMMARY

Array Series	Array Name	Input Cells	Output Cells	I/O Cells
Q700	Q700	38		38
	Q710	28		28
	Q720	8		26
Q1500	Q1500A	46	38	
	QH1500A	60		60
Q3500	Q3500S	-		120
	Q2400S	-		98
	QM1600S	-		104
	Q1300S	-		76

I/O RESOURCE BY I/O MODE

The specific number of available I/O cells is dependent on the I/O mode: 100% TTL; TTL/ECL +5V/-5.2V mixed; 100% ECL -5.2V; and 100% ECL or ECL/TTL +5V REF.

INTERNAL ARRAY CELL RESOURCE SUMMARY BY I/O MODE

Array Name	I/O Mode	Total Function Cells	I Cells	O Cells	I/O Cells
Q700	TTL	208	37		38
	ECL, +5V	206	38		38
	TTL/ECL	206	37		37
	TTL/+5ECL	206	37		37
Q710	TTL	120	27		28
	ECL, +5V	118	28		28
	TTL/ECL	118	27		27
	TTL/+5ECL	118	27		27
Q720	TTL	56	8		26
	ECL, +5V	54	8		26
	TTL/ECL	54	8		26
	TTL/+5ECL	54	8		26
Q1500A	ANY STD	128	46	38	
QH1500A	ANY STD	136	60		60
Q3500S	ANY STD	242			120
Q2400S	ANY STD	153			98
QM1600S	ANY STD	110			104
Q1300S	ANY STD	84			76

Q700 DESIGN GUIDE ADDENDUM:

Q700 SERIES
INTERNAL ARRAY CELL RESOURCE SUMMARY

	Q700	Q710	Q720	
L CELLS	182/180	100/98	42/40	100% TTL / OTHER
B CELLS	26	20	14	
TOTAL-TTL	208	120	56	100% TTL SYSTEM
TOTAL	206	118	54	ANY SYSTEM WITH ECL

Any Q700 series array containing ECL, either: -5.2V REF ECL, +5V REF ECL or ECL/TTL mixed with dual or single power supply, will require the use of two (2) L cells for the development of the VTB, VTA and VRB threshold generator signals.

Q700 SERIES I/O RESOURCES

MODE	DESCRIPTION	Q700	Q710	Q720
TTL SYSTEM	Input cells	37*	27	8
	I/O cells	38	28	26
	D cells	2	-	-
	V_{CC} ($+5V_{DC}$ NOM)	4	4	3
	GROUND	5	5	3
ECL SYSTEM	Input cells	38*	28	8
	I/O cells	38	28	26
	V_{CC}	6	6	5
	V_{EE}	2	2	1
MIXED SYSTEM; ECL/ TTLMIX	Input cells	37*	27	8
	I/O cells	37	27	25
	D cells	2	-	-
	V_{CC} ($+5V_{DC}$ NOM)	3	3	3
	V_{EE} ($-5.2V_{DC}$ NOM)	2	2	1
	TTL GROUND	3	3	2
	ECL GROUND	2	2	1
MIXED +5V SYSTEM ECL/ TTL	Input cells	37*	27	8
	I/O cells	37	27	25
	D cells	2	-	-
	V_{CC} ($+5V_{DC}$ NOM)	5	5	4
	GROUND	5	5	3

* (Includes the dedicated 3-state D cells which are useable as simple input)

The interface to the Q1500A array is accomplished in the input (I) cells and the output (O) cells, to the QH1500A array in the input (I) and input-output (I/O) cells. Input and output cells can be configured to perform I/O operations on the Q1500A array (using two cells for each bidirectional pin). I/O cells on the QH1500A can perform input-only, output-only or bidirectional I/O.
The input, output and I/O cells can perform TTL I/O, ECL I/O or +5V REF ECL I/O. The QH1500A can perform ECL 100K interface with a -4.5V supply (commercial only).

TABLE 5
I/O RESOURCES

MODE	DESCRIPTION	Q1500A	QH1500A	
TTL SYSTEM	Input cells	46	60	MAX
	I/O cells	-	60	MAX
	Output cells	38	-	MAX
	V_{CC} (+5V)	6	14	
	GROUND	4	14	
ECL SYSTEM	Input cells	46	60	MAX
	I/O cells	-	60	MAX
	Output cells	38	-	MAX
	V_{CC}	8	22	
	V_{EE}	2	6	
MIXED SYSTEM; TTLMIX AND ECL	Input cells	46	60	MAX
	I/O cells	-	60	MAX
	Output cells	38	-	MAX
	V_{CC} (+5V)	5	6	
	V_{EE}	2	6	
	GROUND	4	16	
MIXED +5V SYSTEM; OR +5V ECL	Input cells	46	60	MAX
	I/O cells	-	60	MAX
	Output cells	38	-	MAX
	V_{CC}	6	12	
	V_{EE}	-	-	
	GROUND	4	16	

AMCC
APPLIED MICRO CIRCUITS CORPORATION

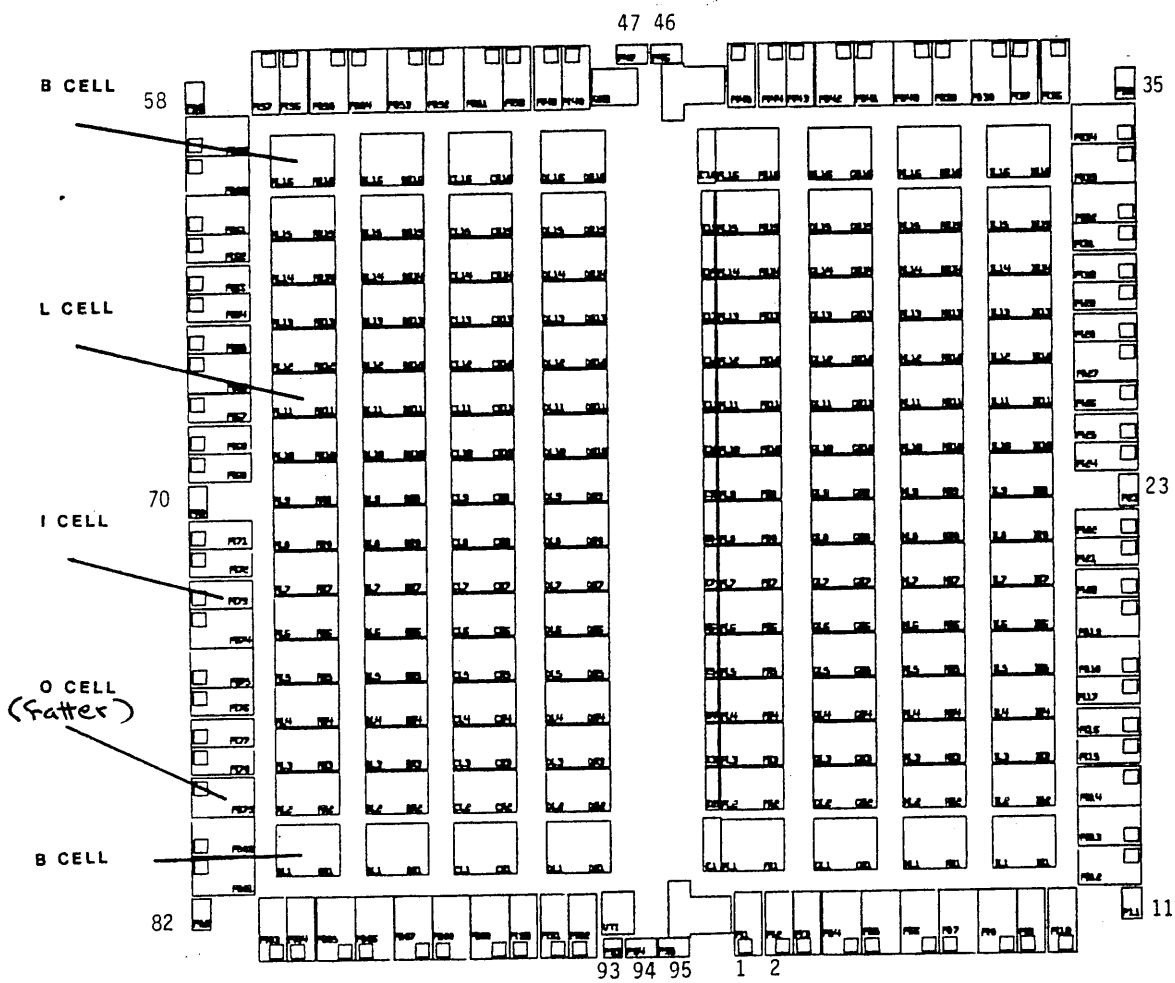
TABLE 3
I/O RESOURCES

MODE	DESCRIPTION	Q3500S	Q2400S	Q1300S	QM1600S
TTL SYSTEM	I/O Cells	120	98	76	104
	V_{CC} (+5V)	10	10	8	10
	GROUND	18	18	8	18
ECL SYSTEM	I/O Cells	120	98	76	104
	V_{CC} (GND)	22	22	8	22
	V_{EE} **	6	6	8	6
MIXED TTLMIX and ECL SYSTEM	I/O Cells	120	98	76	104
	V_{CC} (+5V_{DC} NOM)	4	4	4	4
	V_{EE} **	6	6	4	6
	TTL GROUND	8	8	4	8
	ECL GROUND	10	10	4	10
MIXED +5V SYSTEM; OR +5V ECL	I/O cells	120	98	76	104
	V_{CC} (+5V_{DC} NOM)	14	14	8	14
	GROUND	14	14	8	14

** (-4.5 V_{DC} to -5.2 V_{DC} NOMINAL for ECL 100K;
-5.2 V_{DC} NOMINAL for ECL 10K)

- A PLACEMENT WORKSHEET IS AVAILABLE FOR THE OTHER ARRAYS AS NEEDED

Q1500A CHIP PLAN

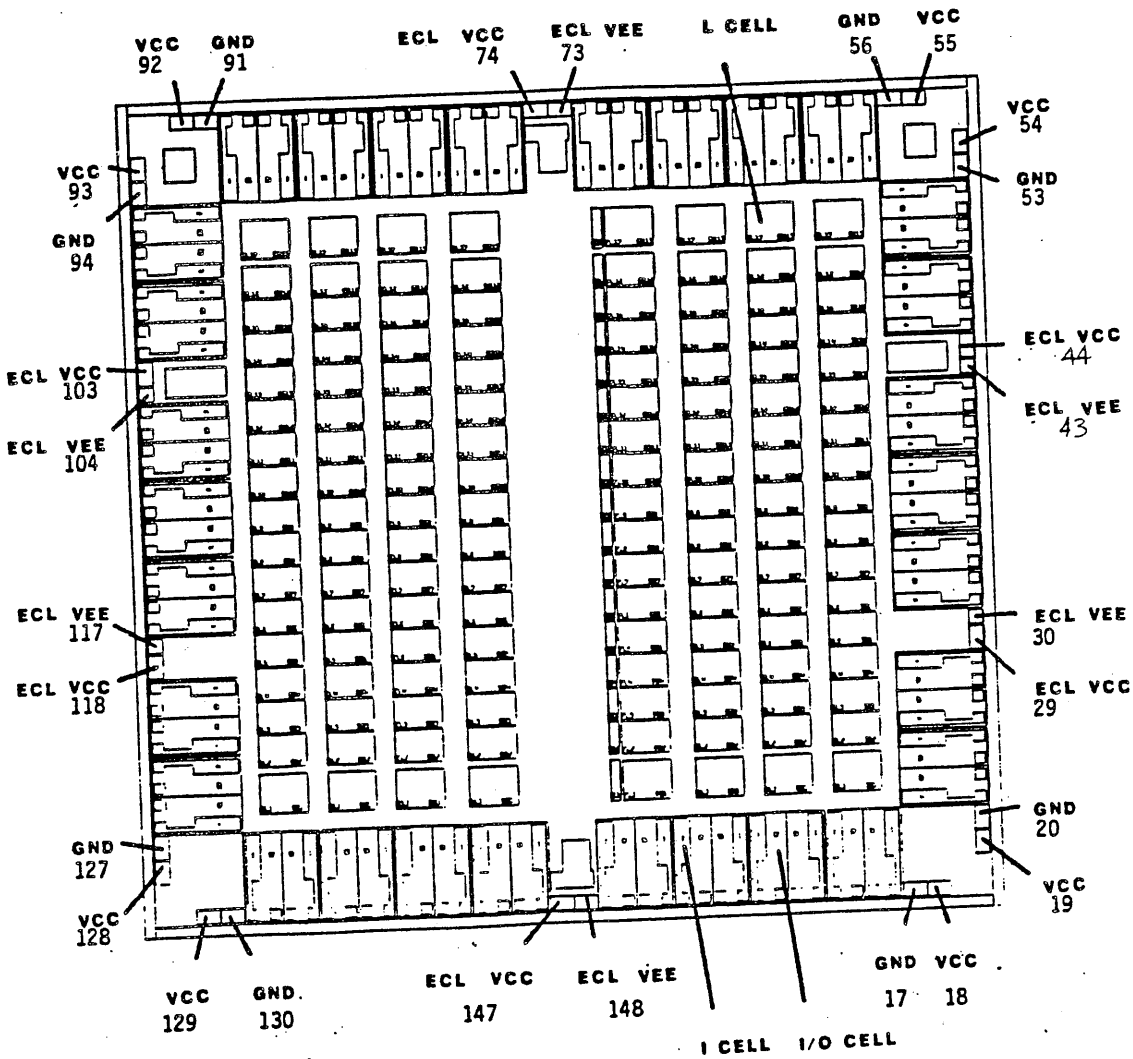


TTL MODE: +5V = 11, 35, 47, 58, 82, 94; GND = 23, 46, 70, 95

ECL MODE: -5.2V = 46, 95; GND = 11, 23, 35, 47, 58, 70, 82, 94

MIXED MODE: +5V = 11, 35, 58, 82, 93; GND = 23, 47, 70, 94; -5.2V = 46, 95

QH1500A CHIP PLAN



TTL MODE: +5V = 18, 19, 29, 44, 54, 55, 74, 92, 93, 103, 118, 128, 129, 147
GND = 17, 20, 30, 43, 53, 56, 73, 91, 94, 104, 117, 127, 130, 148

ECL MODE: -52.V = 30, 43, 73, 104, 117, 148
GND = 17, 18, 19, 20, 29, 44, 53, 54, 55, 56, 74, 91, 92, 93, 94, 103, 118, 127, 128, 129, 130, 147

MIXED MODE: +5V = 18, 19, 54, 93, 128, 129
-5.2V = 30, 43, 73, 104, 117, 148
GND = 17, 20, 29, 44, 53, 55, 56, 74, 91, 92, 94, 103, 118, 127, 130, 147

EXTRA POWER / GROUND

- THE I/O MIX ITSELF (TTL, ECL) ALSO HAS A BEARING ON THE NUMBER OF I/O PINS AVAILABLE

    - HEAVY USE OF SIMULTANEOUSLY SWITCHING TTL OUTPUTS REQUIRES EXTRA V_{CC} AND GROUND PINS, PLACED ON SPARE I/O OR I PIN SITES

    - Q700:

        M7EBPWR, M7EBGND I/O CELL
        M7EIPWR, M7EIGND I CELL

    - Q1500:

        M8TIPWR, M8TIGND I CELL
        M8TBPWR, M8TBGND O CELL

    - QH1500 DOES NOT REQUIRE EXTRA POWER OR GROUND PINS - IT HAS ENOUGH

- ADDING EXTRA GROUND - Q700 SERIES

  - AS A DESIGN GUIDELINE - AS A MINIMUM ADD 1 GND PAD TO ANY HALF OF THE CHIP THAT HAS MORE THAN SEVEN (7) SIMULTANEOUSLY SWITCHING OUTPUTS

  - ADD 1 GND PAD TO ANY HALF OF THE CHIP WHERE THE NUMBER OF SIMULTANEOUSLY SWITCHING OUTPUTS PLUS TWO-THIRDS (2/3) OF THE ECL OUTPUTS EQUALS (EIGHT) 8 OR MORE

  - WHENEVER THE D CELL IS USED, A GND PAD MUST BE ADDED

  - WHENEVER A 3-STATE I/O IS USED, AND IT IS NOT LOCATED NEXT TO AN EXISTING GROUND, A GND PAD MUST BE ADDED

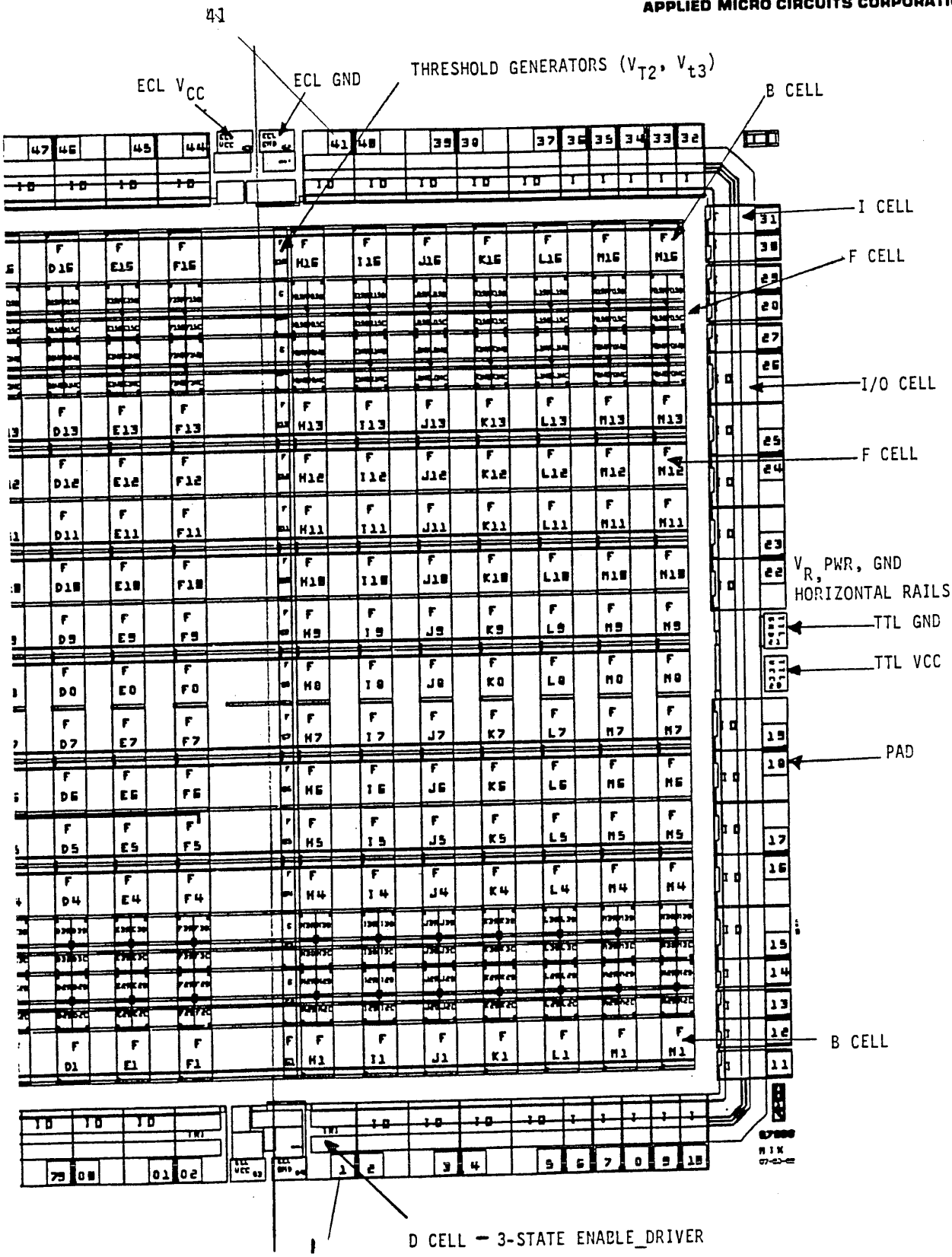
- ADDING EXTRA V_{CC} - Q700 SERIES; Q1500 ARRAY
  - THE NEXT PAGE SHOWS THE RIGHT HALF OF THE Q700 (THE LEFT IS A MIRROR IMAGE)
  - TTL POWER AND GROUND SUPPLIES ARE CONFIGURED AS TWO "C"s, TO REDUCE CAPACITIVE COUPLING BETWEEN ECL AND TTL ON THE CHIP
  - AS A DESIGN GUIDELINE - AS A MINIMUM ADD 1 V_{CC} PAD TO ANY HALF OF THE CHIP THAT HAS MORE THAN EIGHT (8) SIMULTANEOUSLY SWITCHING OUTPUTS (Q700, Q1500)

- EXAMPLE - Q700
  - TTL V_{CC} SERVES CELLS CONNECTED TO PADS:

PAD 20	1-41
PAD 64	44-82

  - IF THE NUMBER OF SIMULTANEOUSLY SWITCHING OUTPUTS ON PADS 1-41 EXCEEDS 8
    - THEN A SPARE I OR I/O CELL SHOULD BE ASSIGNED AS ANOTHER V_{CC} INPUT FOR THAT HALF OF THE CHIP

AMCC
APPLIED MICRO CIRCUITS CORPORATION



The Q700 series arrays require extra power and ground be added when the number of simultaneously switching TTL or TTL and ECL outputs exceeds 8 for any half of the array. There are other criteria for adding power and ground. Refer to the appropriate sections of the design guide.

Q700 SERIES ADDITIONAL POWER/GROUND REQUIREMENTS

When the number of simultaneously switching outputs on either half of the array is:		ADDITIONAL PINS:	
# TTL OUTPUTS:		TTL V_{CC}	TTL GROUND
TTL SYSTEM	0-7	-	-
	8	-	1
	9-15	1	1
	16	1	2
	17-19	2	2
# ECL OUTPUTS:		-	ECL GROUND
ECL SYSTEM (any)	0-7	-	-
	8-15	-	1
	15-19	-	2
(# TTL + # ECL):		TTL V_{CC}	TTL GROUND
MIXED SYSTEM*	0-7	-	-
	8-15	-	1
	15-19	1	2

* +5V ECL/TTL or ECL/TTLMIX

INPUT-OUTPUT AVAILABILITY

Adding extra power and ground pins will reduce the number of pins available for I/O signals.

ADDING EXTRA GROUND - Q1500A ONLY

As a design guideline the designer should allocate a minimum of one additional ground pad to any half of the chip where the number of simultaneously switching TTL outputs plus 2/3rds of the number of ECL outputs equals eight (8) or more. (i.e., 8 TTL; 12 ECL; 6 TTL + 3 ECL) Three-state TTL outputs should be located near ground pins. There is no need to add additional ground pins for these macros.

TABLE 6
Q1500A ADDITIONAL POWER/GROUND REQUIREMENTS

ON EITHER HALF OF CHIP:	ADDITIONAL PINS:		
	#TTL	V_{CC}	GROUND
TTL SYSTEM	0-7	-	-
	8	-	1
	9-15	1	1
	16	1	2
	17-19	2	2
	#ECL	-	GROUND
ECL SYSTEM	0-7	-	-
	8-15	-	1
	15-19	-	2
	#TTL + #ECL	V_{CC}	GROUND
MIXED SYSTEM	0-7	-	-
	8-15	-	1
	15-19	1	2

TABLE 5
ADDITIONAL POWER/GROUND

# OF SIMULTANEOUSLY SWITCHING TTL PER QUADRANT		ADD TTL V_{CC} - TTL GROUND PAIRS (2 pads)
100% TTL:	0 - 16	0
	17 - 24	1
	25 - 30*	2
MIXED ECL/TTL:	0 - 8	0
	9 - 16	1
	17 - 30*	2
# OF SIMULTANEOUSLY SWITCHING ECL PER QUADRANT		**ADD ECL GROUND:**
100% ECL:	0 - 16	0
	17 - 24	1
	25 - 30*	2
MIXED ECL/TTL:	0 - 8	0
	9 - 16	1
	17 - 24	2
	25 - 30*	3

* There is a MAXIMUM of 30 I/O cells per quadrant in the largest array. Adding extra power and ground will REDUCE the number of pins available for I/O signals. (See Table 6.) Added ground pins must be interspersed with the simultaneously switching signals.

TABLE 6
EXTERNAL PINS

ARRAY	POWER-GROUND PINS	I/O PINS	TOTAL PINS
Q3500S	28	120	148
Q2400S	28	98	126
QM1600S	28	104	132
Q1300S	16	76	92

VTI LIMIT

MAXIMUM H OPTION TTL I/O MACROS - Q700, Q1500 ARRAYS ONLY

There is a limit as to how many TTL inputs can be placed on a Q700 or Q1500 series array when high-speed (H) option I/O macros are used. This is not a current limitation, it is a limitation imposed by the VTI threshold generator. A standard TTL input macro counts as 1 VTI unit load. A high-speed TTL input counts as 6 VTI unit loads. A table summarizing the VTI limits is listed below.

MAXIMUM VTI UNIT LOADS PER ARRAY

Array:	Loads:
Q700 Series	50
Q1500A	50
QH1500A	120 (60 on the right; 60 on the left)
Q3500 Series	No restrictions

I/O INTERFACE

CHAP 4 - I/O INTERFACE
- Q700 Series Rules
- Q1500 Series Rules
- Q3500 Series (use Q1500 rules)

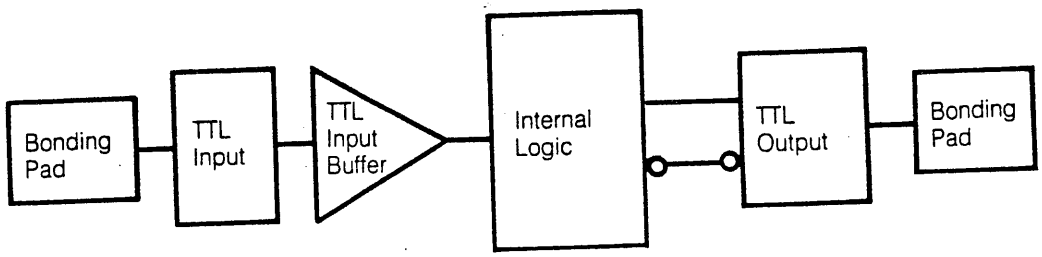
Macro Summary
- "Appendix A"
- ECL macro selection tables

- I/O IS OFTEN THE KEY IN A SELECTION
  - WHEN REPLACING A TTL DESIGN A FEW HIGH CURRENT OUTPUTS ARE NEEDED
  - NUMEROUS OPTIONS BECOME THE IMPORTANT FACTOR IN A DECISION

- THE NEXT PAGES SHOW THE INTERFACE REQUIREMENTS OF THE Q700, Q1500 AND Q3500 SERIES ARRAYS

Q700 SERIES INTERFACE MACRO GUIDELINES

100% TTL INTERFACE
Single +5V Power Supply

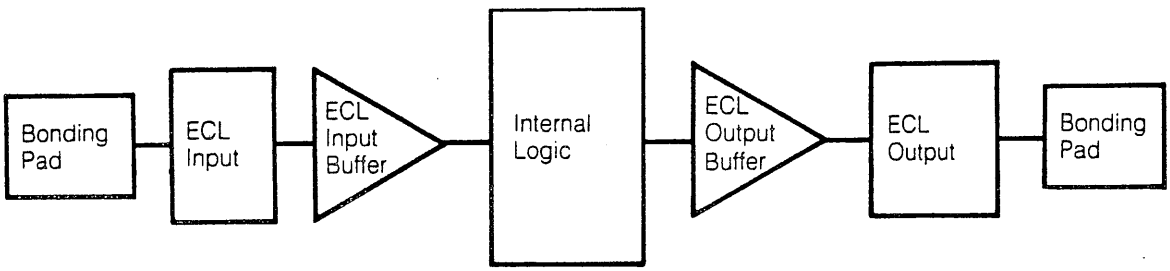


INPUT:
- Use TTL interface macros
- TTL input will be located on an I or I/O cell
- Buffer macros must be placed in internal array (L or B cell)

OUTPUT:
- Use TTL interface macros
- TTL output macros will be located on an I/O cell
- Bi-directional interface macros available
- Outputs must be differentially driven from the last stage of logic (no buffer)

FIGURE 3A

100% ECL INTERFACE
Single −5.2 Power Supply



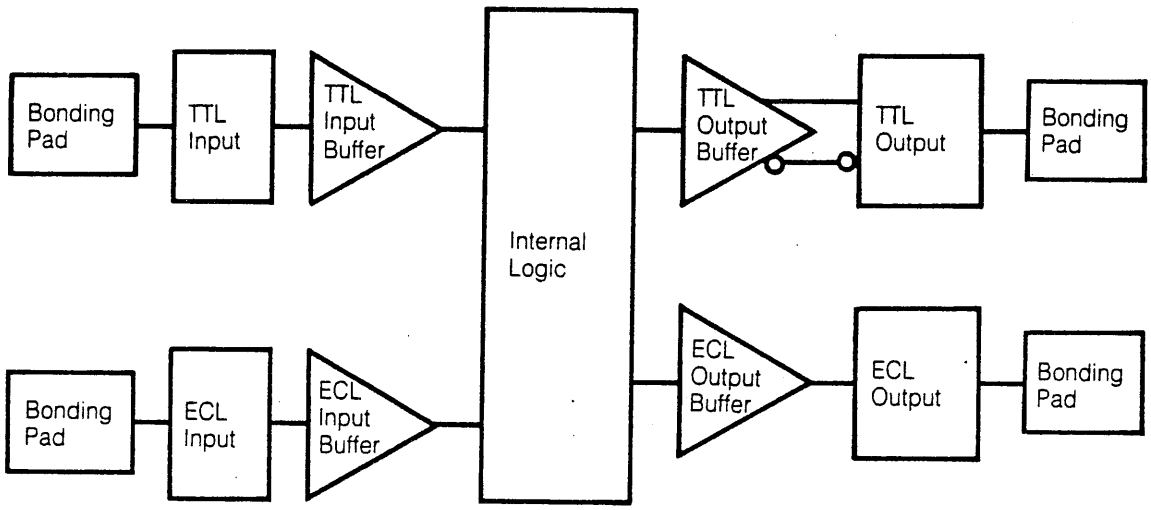
INPUT:
- Use ECL interface macros
- ECL input will be located on an I or I/O cell
- Use ECL buffer macros. Buffer macros must be placed in internal array (L or B cell)

OUTPUT:
- Use ECL interface macros
- ECL output buffer must be placed on B cell in internal array
- ECL output must be placed on an I/O cell
- On 50 ohm, and 200 ohm outputs a maximum of 26, 20 and 14 outputs can be used on the Q700, Q710 and Q720 respectively
- Some buffers have gating logic for last stage tasks.
- ECL output must be buffered

FIGURE 3B

Q700 SERIES INTERFACE MACRO GUIDELINES (CONTINUED)

MIXED ECL/TTL INTERFACE
+5V and −5.2V Power Supply

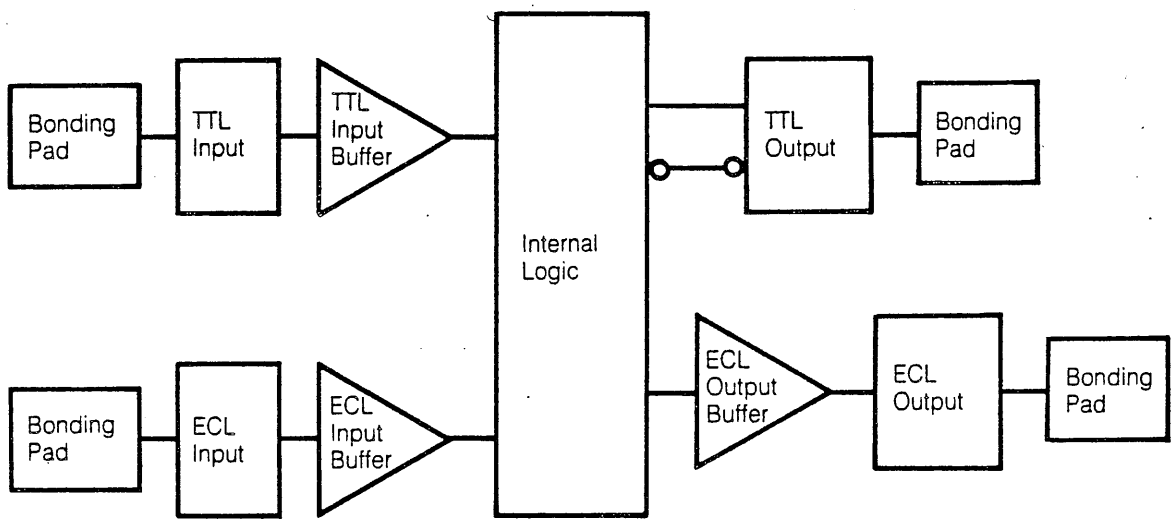


INPUT:
- Use TTLMIX interface macros
- Use ECLMIX interface macros
- Use ECL Buffers
- Buffer macros must be placed in internal array (L or B cell)
- TTL, ECL input will be located on I or I/O cells

OUTPUT:
- Use ECLMIX interface macros
- Use TTLMIX interface macros
- ECL buffer must be placed on B cell in internal array
- ECL output must be placed on an I/O cell
- Termination limits are the same

FIGURE 3C

MIXED ECL/TTL INTERFACE
Single +5V Power Supply



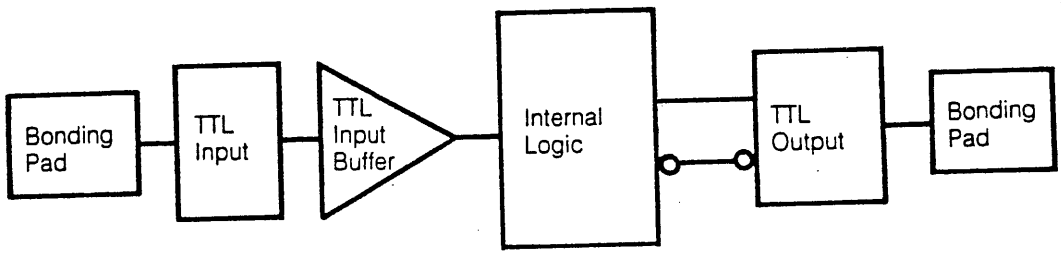
INPUT:
- TTL: Identical to guidelines for 100% TTL Interface
- ECL: Use special input macros identified for +5V referenced ECL
- Buffer macros must be placed in internal array (L or B cell)
- ECL input will be located on an I or I/O cell

OUTPUT:
- TTL: Identical to guidelines for 100% TTL interface
- ECL: use special output macros identified for +5V referenced ECL
- ECL buffer must be placed on B cell in internal array
- ECL output must be placed on an I/0 cell
- On 50 ohm, and 200 ohm outputs a maximum of 26, 20 and 14 outputs can be used on the Q700, 710 and Q720 respectively
- Some buffers have gating logic for last stage tasks

FIGURE 3D

Q1500 SERIES INTERFACE MACRO GUIDELINES

100% TTL INTERFACE
Single +5V Power Supply



Q1500 INPUT:
- Use TTL interface macros
- Must be located on I cell
- TTL input macros contain necessary buffers internally

QH1500 INPUT:
- Use TTL interface macros
- May be located on I or I/O
- TTL input macros contain necessary buffers internally

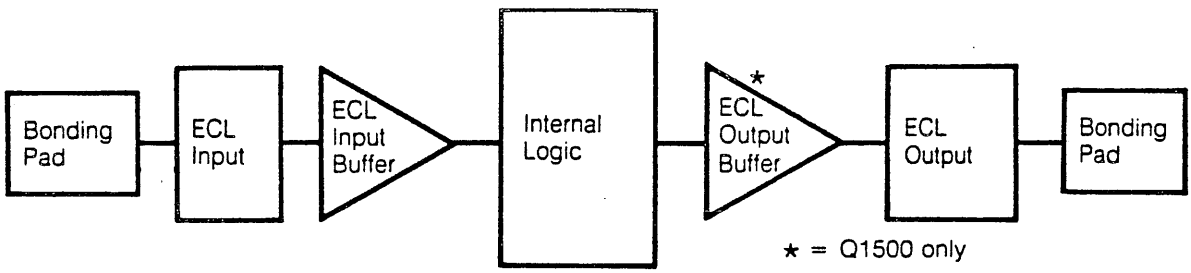
Q1500 OUTPUT:
- Use TTL interface macros
- Must be located on O cell
- TTL output macros contain necessary buffers internally or use output macros which must be differentially driven from the last stage of logic (for speed)

QH1500 OUTPUT MACROS:
- Use TTL interface macros
- Must be located on I/O cell
- TTL output macros contain necessary buffers internally or use output macros which must be differentially driven from the last stage of logic (for speed)
- Bi-directional interface macros are available

FIGURE 3A

Q1500 SERIES INTERFACE MACRO GUIDELINES (CONTINUED)

100% ECL INTERFACE
Single -5.2V Power Supply



Q1500 INPUT:
- Use ECL interface macros
- May be located on I or O cell
- ECL input macros contain necessary buffers internally or require a separate buffer in a logic function

QH1500 INPUT:
- Use ECL interface macros
- May be placed on I or I/O
- ECL input macros contain necessary buffers internally or require a separate buffer in a logic function

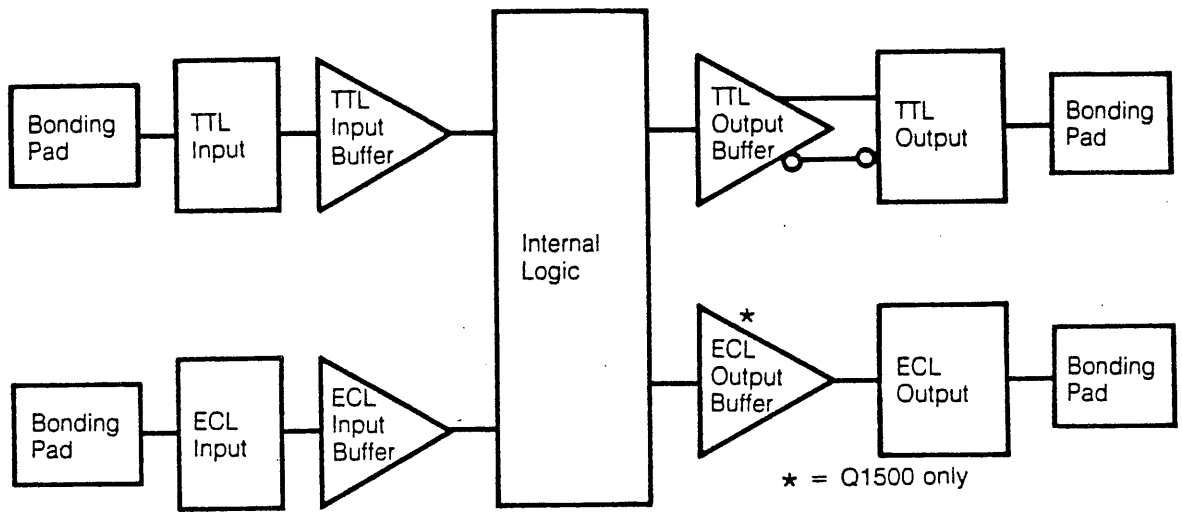
Q1500 OUTPUT:
- Use ECL interface macros
- ECL output buffer (BExx) must be placed on B cell in internal array
- ECL output must be placed on O cell
- Available in 50 ohm, 100 ohm and 200 ohm terminations
- Bus limitation permits a maximum of 32 50 ohm outputs

QH1500 OUTPUT:
- Use ECL interface macros
- No B cells —ECL output macros contain necessary buffers internally
- ECL output must be placed on I/O cell
- Available in 50 ohm termination only
- No limit on number of 50 ohm outputs
- Supports 10K and 100K ECL

FIGURE 3B

Q1500 SERIES INTERFACE MACRO GUIDELINES (CONTINUED)

MIXED ECL/TTL INTERFACE
+5V and −5.2V Power Supply



Q1500 INPUT:
- TTL: Identical to guidelines for 100% TTL circuits, except use TTLMIX interface macros
- ECL: Identical to guidelines for 100% ECL circuits

QH1500 INPUT:
- TTL: Identical to guidelines for 100% TTL circuits, except use TTLMIX interface macros
- ECL: Identical to guidelines for 100% ECL circuits

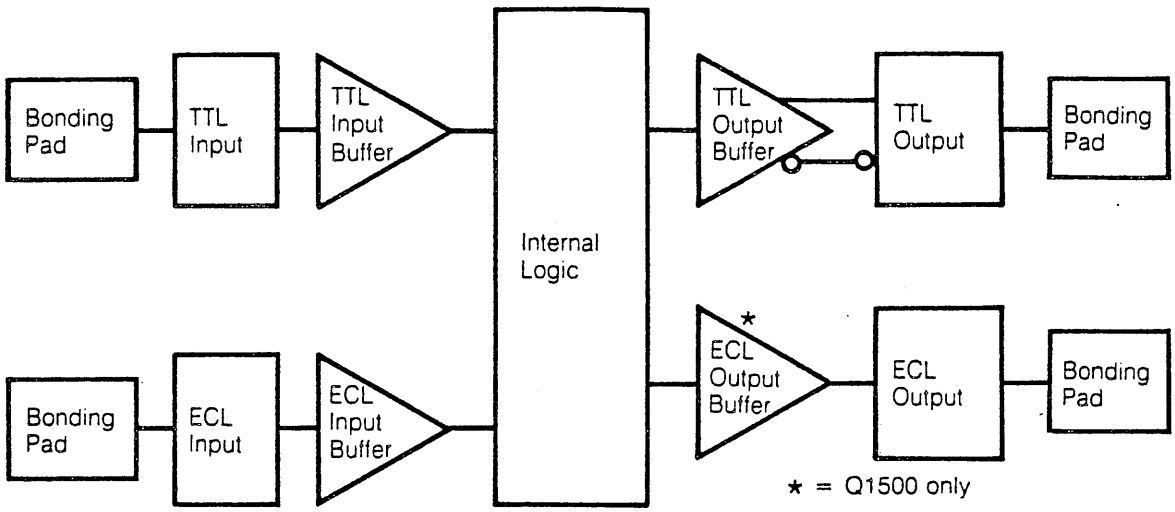
Q1500 OUTPUT:
- TTL: Identical to guidelines for 100% TTL circuits, except use TTLMIX interface macros
- ECL: Identical to guidelines for 100% ECL circuits

QH1500 OUTPUT:
- TTL: Identical to guidelines for 100% TTL circuits, except use TTLMIX interface macros
- ECL: Identical to guidelines for 100% ECL circuits
- No B cell —output macros contain necessary buffers internally
- Use ECL macros according to their labels (OP, OE, OQ, OK)
- Supports 10K and 100K ECL

FIGURE 3C

Q1500 SERIES INTERFACE MACRO GUIDELINES (CONTINUED)

MIXED ECL/TTL INTERFACE
Single +5V Power Supply



Q1500 INPUT:
- TTL: Identical to guidelines for 100% TTL circuits
- Use ECL macros (IExx)

QH1500 INPUT:
- TTL: Identical to guidelines for 100% TTL circuits
- ECL: Identical to guidelines for 100% +5V Ref ECL circuits
- Use +5V Ref ECL macros (IPxx)

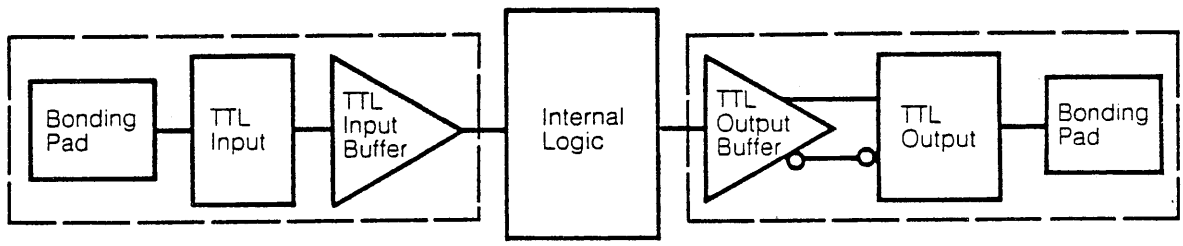
Q1500 OUTPUT:
- TTL: Identical to guidelines for 100% TTL circuits.
- ECL: Identical to guidelines for 100% +5V Ref ECL circuits
- +5V Ref ECL: Use the ECL I/O macros labeled for use in these circuits (OPxx)

QH1500 OUTPUT:
- TTL in a +5V Ref ECL mixed: Use 100% TTL interface
- Use ECL macros according to their labels (OP, OE, OQ, OK)
- Supports 10K and 100K +5V Ref ECL

FIGURE 3D

Q3500 SERIES INTERFACE MACRO GUIDELINES

100% TTL INTERFACE
Single +5V Power Supply



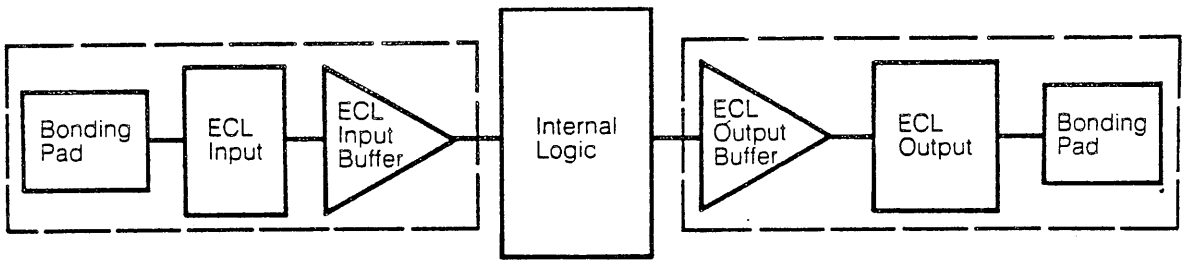
Q3500 SERIES INPUT:
- Use TTL interface macros
- TTL input macros contain necessary buffers internally

Q3500 SERIES OUTPUT:
- Use TTL interface macros
- TTL output macros contain necessary macros internally or use output macros which must be differentially driven from the last stage of logic (for speed)
- For simultaneously switching TTL outputs, use buffered output macros

FIGURE 3A

Q3500 SERIES INTERFACE MACRO GUIDELINES (CONTINUED)

100% ECL INTERFACE
Single −5.2V Power Supply



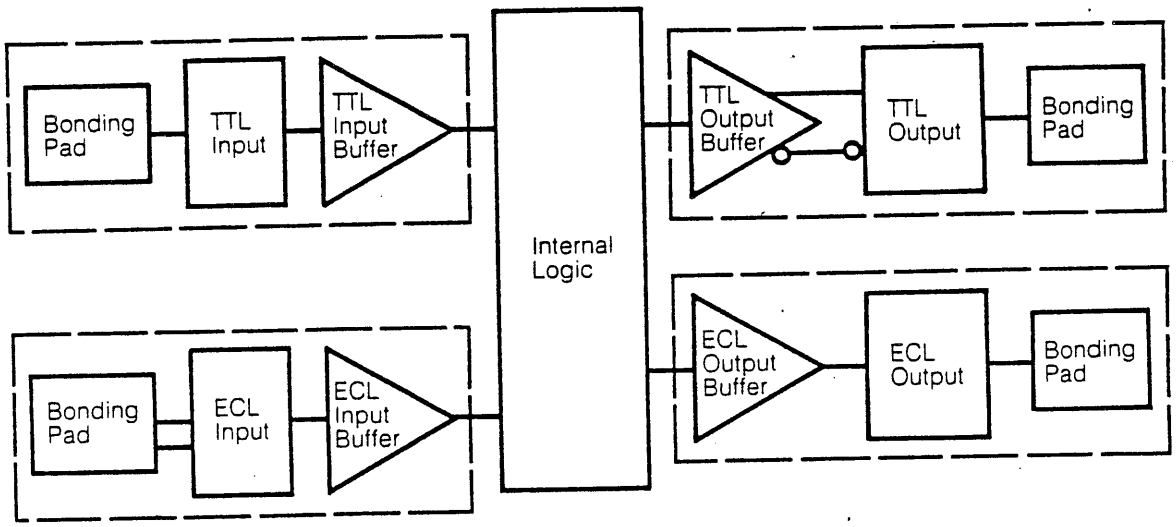
Q3500 SERIES INPUT:
- Use ECL interface macros
- ECL input macros contain necessary buffers internally
- IE85: connects to a buffered input macro or to the buffered logic BIxx series macros

Q3500 SERIES OUTPUT:
- Use ECL interface macros
- ECL available in 50 ohm terminations (use to drive 100, 200 ohm as well)
- ECL output macros contain necessary buffers internally
- Supports both ECL 10K (OExx) and ECL 100K (OKxx)

FIGURE 3B

Q3500 SERIES INTERFACE MACRO GUIDELINES (CONTINUED)

MIXED ECL/TTL INTERFACE
Single +5V Power Supply



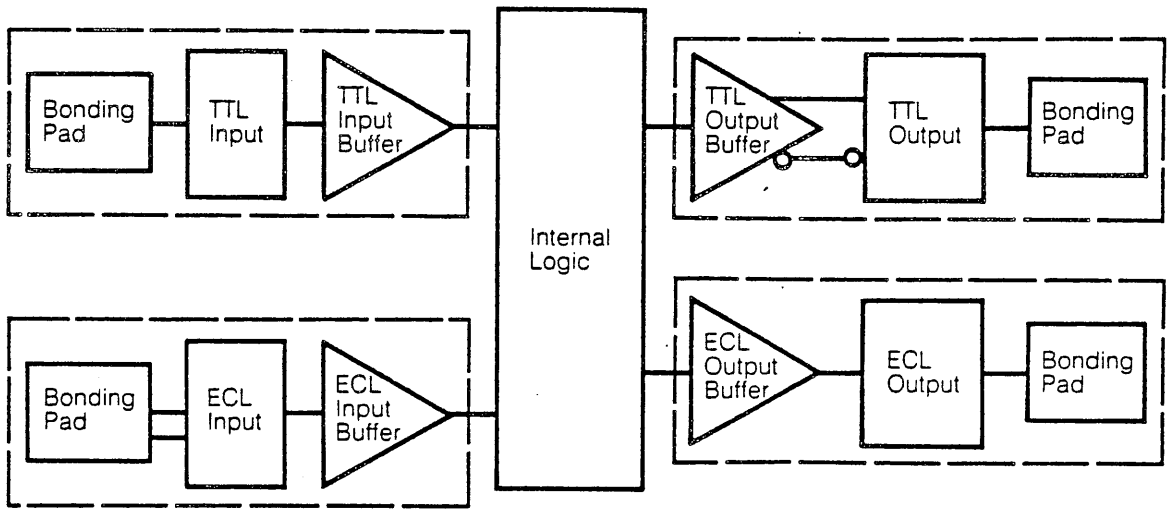
Q3500 SERIES INPUT:
- TLL: Identical to guidelines for 100% TTL circuits
- ECL: Identical to guidelines for 100% ECL circuits

Q3500 SERIES OUTPUT:
- Identical to guidelines for 100% TTL circuits except use buffered output macros
- ECL: Identical to guidelines for 100% ECL circuits

FIGURE 3C

Q3500 SERIES INTERFACE MACRO GUIDELINES (CONTINUED)

MIXED ECL/TTL INTERFACE
+5V and −5.2V Power Supply



Q3500 SERIES INPUT:
- TTL: Identical to guidelines for 100% TTL circuits
- ECL: Identical to guidelines for 100% ECL circuits

Q3500 SERIES OUTPUT:
- TTL: Identical to guidelines for 100% TTL circuits except use buffered output macros
- ECL: Identical to guidelines for 100% ECL circuits

FIGURE 3D

QUESTION: WHAT BUFFERS ARE INCLUDED IN I/O MACROS?

- Q700 - NONE
- Q1500 - SOME IN Q1500 ARRAY,
  MOST IN QH1500 ARRAY
- Q3500 - SAME AS QH1500 (BUFFERED)

QUESTION: WHAT BUFFER MACROS MUST BE ADDED?

- Q700 - SEE INTERFACE GUIDELINES
  NEED TTL I/O, ECL I/O BUFFERS
- Q1500 - NEED ECL I/O BUFFERS
  TTL DEPENDS
- QH1500 - SOME ECL BIXX IF DESIRED
  ELSE ALREADY INCLUDED
- Q3500 - SOME ECL BIXX IF DESIRED
  ELSE ALREADY INCLUDED

Buffered macros should be used for simultaneously switching TTL outputs to reduce noise and to avoid the added propagation delays due to heavy switching.

MACRO SUMMARY

The macro summary in Appendix A is divided into four segments, TTL, TTLMIX, ECL and Internal Logic Functions.

For +5V only circuits, the TTL macros will be selected from the TTL section of Appendix A. For dual power supply circuits, the TTL macros will be selected from the TTLMIX section of Appendix A.

The ECL macros will be selected from the ECL section of the appendix. The ECL macros are available for standard reference voltage and for +5V reference voltage circuits. The designer must select the version of the macro (not the option) which is required. For the QH1500A, ECL outputs are also differentiated between ECL 10K and ECL 100K. (And for the Q3500 as well.)

TABLE 8
ECL MACRO SELECTION

	Q1500A ECL 10K		QH1500A ECL 10K		QH1500A ECL 100K	
	+5V REF	GND REF	+5V REF	GND REF	+5V REF	GND REF
INPUTS	IExx	IExx	IPxx	IExx	IPxx	IExx
OUTPUTS	OPxx	OExx	OPxx	OExx	OQxx	OKxx

ECL MACRO SELECTION

	Q3500 ECL 10K		Q3500 ECL 100K	
	+5V REF	GND REF	+5V REF	GND REF
INPUTS	IExx	IExx	IExx	IExx
OUTPUTS	OExx	OExx	OKxx	OKxx

AMCC
APPLIED MICRO CIRCUITS CORPORATION

ARRAY

POPULATION

CHAP 5 - ARRAY POPULATION
Array Selection
- logic-heavy
- I/O intensive

Cell Assessment worksheet
Pin-Count - Limits
Introducing the AMCC Proprietary Software
Suport: - ERCs
- MACROCCUR
  - macro list
  - current dissipation
- Population
- Pin-Count

Sizing Guidelines

ARRAY SELECTION

- THE NUMBER OF CELLS:
  - CELL UTILIZATION OF THE INTERNAL L,B CELLS;
  - POPULATION OF THE I, O, I/O CELLS

  IS ONE MEASURE OF BUILDABILITY

- 85-95% UTILIZATION IS A GUIDELINE
  - 100% UTILIZATION IS NOT PRACTICAL
  - THE ARRAY SELECTED FOR LOGIC-HEAVY DESIGNS MAY BE BASED ON L/B CELL UTILIZATION AND NOT I/O

- I/O POPULATION IS ONE ARRAY SELECTION FACTOR
  - I/O LIMITED DESIGNS MAY HAVE LESS % UTILIZATION - THE ARRAY SELECTED MAY BE BASED ON I/O NEEDS

QUESTION: CAN YOUR DESIGN FIT THE TARGET ARRAY?

QUESTION: CAN WE BUILD IT?
(IS IT ROUTABLE?)

- ON THE COMPLETION OF THE DESIGN
  - INITIAL DESIGN
  - INITIAL CONVERSION
  - FINAL DESIGN AS SUBMITTED

- A MACRO LIST SHOULD BE PREPARED
  - MUST BE SUBMITTED WITH THE DESIGN
  - SHOULD HAVE AN INITIAL LIST ASAP
  - SHOULD KEEP THAT LIST UPDATED WITH
    - CUSTOM MACROS
    - PRELIMINARY MACROS WE SAID YOU COULD USE (AND SENT YOU A PATCH FOR)

- INITIAL LIST IS BY HAND

- THE SAMPLE WORKSHEET ON THE NEXT PAGE MAY COME IN HANDY IN DETERMINING IF YOU FIT THE TARGETED ARRAY (SEE THE DESIGN GUIDES)

DESIGN_____ DATE:_____ PAGE: ___

Q700 SERIES: ARRAY _____ TYPE:_____

(ECL, TTL, MIXED, +5V REF, +5V REF MIXED)

Q700 SERIES UTILIZATION WORKSHEET

MACRO (SEE MACRO_TAB.DOC)	PLACEMENT L/B	L	B	I	I/O	D
AVAILABLE:						

- AFTER ALL ADDITIONAL I/O, I, O CELLS HAVE BEEN DESIGNATED FOR POWER, GROUND, PROCEED WITH THE CELL ASSESSMENT

TOTAL THIS PAGE:						

- WHAT SIZE ARRAY SHOULD BE USED? - CELL ASSESSMENT
  - CELL ASSESSMENT INVOLVES A TALLY OF THE CELLS USED IN A DESIGN SUMMED BY TYPE
  - THIS INCLUDES I/O, BUFFERS (B), AND LOGIC (L) ALTHOUGH L AND B CELLS DETERMINE THE ACTUAL % UTILIZATION QUOTED ON THE DATA SHEET
  - HIGH-SPEED AND POWER OPTIONS NEED TO BE NOTED - KEEP THESE AT 30% OR LESS
  - DISTRIBUTE POWER, SPEED ACROSS THE ARRAY
  - BALANCE YOUR DESIGN IN TERMS OF I/O AND INTERNAL LOGIC

PIN-COUNT

- PIN-COUNT IS REQUIRED AT DESIGN SUBMISSION
- TOO MANY PINS AND THE DESIGN BECOMES "AT RISK"
- THE DESIGN COULD BECOME TOO RISKY TO ACCEPT
- ONCE THE MACRO LIST IS KNOWN, THE PIN-COUNT CAN BE ESTIMATED
    - COUNT ALL PINS ON ALL MACROS IF THE CONNECT IS NOT KNOWN
    - ADD Q700 THRESHOLD GENERATOR CONNECTS
    - USE ESTIMATED PINCOUNT LIMITS
- ONCE THE SCHEMATIC IS CAPTURED, THE PIN-COUNT IS A KNOWN
    - COUNT ALL CONNECTED PINS ON THE MACROS
    - Q700 THRESHOLD PINS ARE HANDLED THE SAME AS BEFORE

PIN COUNT LIMIT

An array is routable if the number of pins does not exceed the maximum pin count limit. It is considered to be a risky design if the number of pins is up to +10% of the maximum pin count limit. It is considered to be an extremely risky design if the number of pins is from +11% to +18% over the maximum pin count limit. A design is unacceptable is the number of pins is ≥+18% over the maximum allowed pin count.

MAXIMUM PIN-COUNT

Array	Actual Limit	Estimated Limit
Q700	1100	1045
Q710	650	615
Q720	315	300
Q1500A	1092	1040
QH1500A	1206	1140
Q3500S	2470	2346
Q2400S	1593	1513
Q1300S	906	860
QM1600S	1193	1133

AMCC
APPLIED MICRO CIRCUITS CORPORATION

AMCC SOFTWARE SUPPORT

ERCs

- AMCC PROPRIETARY ERC SOFTWARE PREPARES THE MACROCCUR REPORT THAT LISTS ALL MACROS IN THE SCHEMATIC - AND THEIR CURRENT DISSIPATION (USE FOR WORST-CASE POWER COMPUTATION)

- AMCC PROPRIETARY ERC SOFTWARE PREPARES A CELL POPULATION REPORT FOR YOU

- AMCC PROPRIETARY ERC SOFTWARE PREPARES A PIN-COUNT REPORT FOR YOU

PLUS OTHER CHECKS (more later)

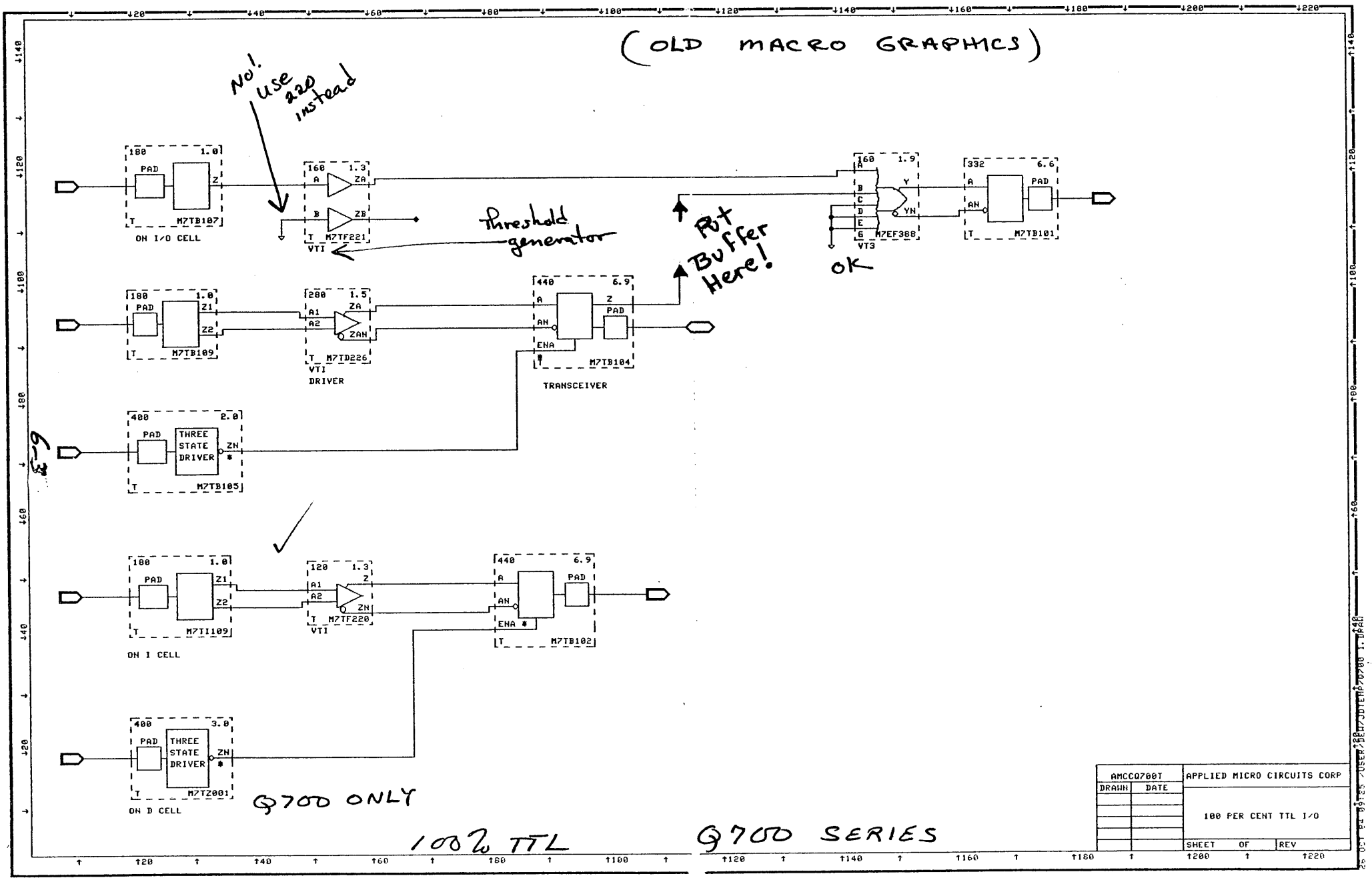
- GUIDELINES:
  - REMEMBER TO ALWAYS TRY TO LEAVE ROOM FOR ERROR OR ENHANCEMENT OR CHANGES, ETC.
  - DESIGN FOR 65% UTILIZATION WHEN THE DESIGN IS NOT "FIRM"
  - REMEMBER THAT 20-30% OF AN ARRAY SHOULD BE RESERVED FOR TEST HARDWARE - THE SAME RULES APPLY TO THE ARRAY AS WOULD APPLY TO A PCB
  - TEST POINTS REQUIRE I/O CELLS, SOME LOGIC
  - MULTIPLEXED TEST OUTPUTS REQUIRE LOGIC CELLS AS WELL
  - P L A N A H E A D

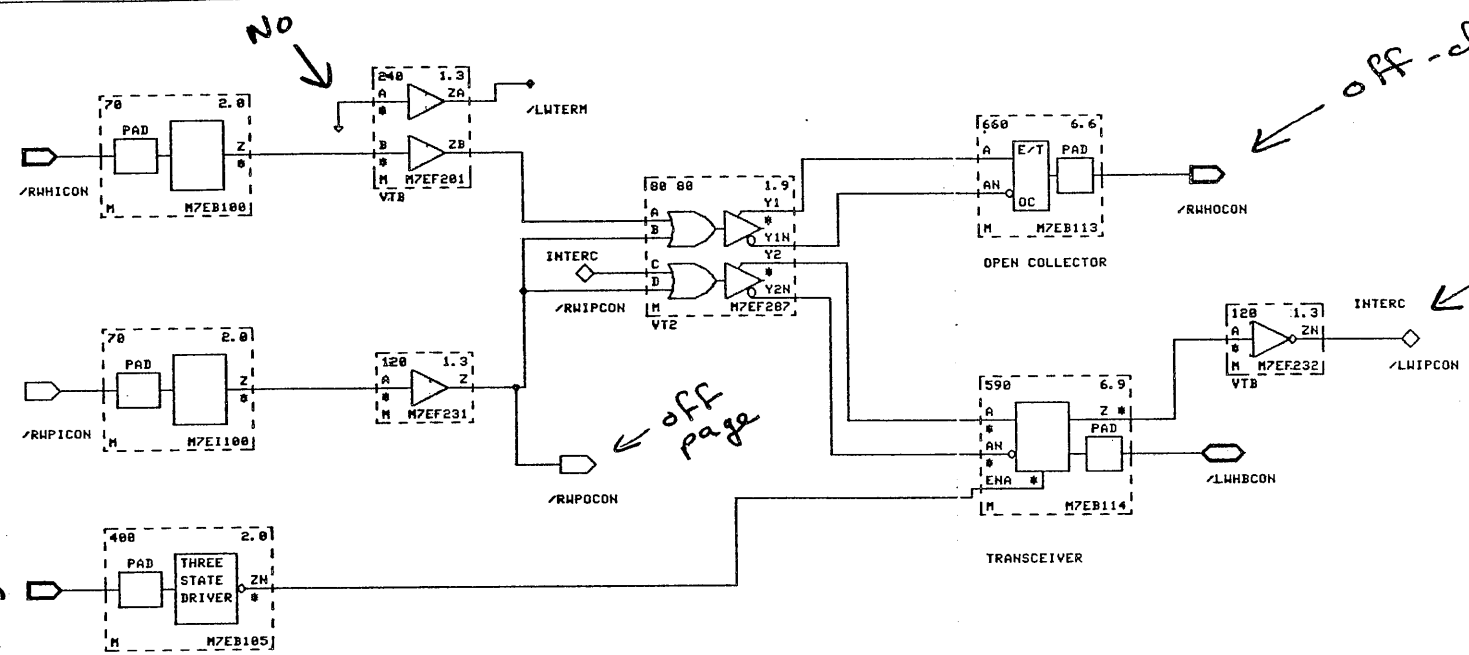
HINT: CREATE FOR MORE THAN ONE APPLICATION

- SIMILAR DESIGNS COULD BE BUILT ON THE DESIGN EFFORT ALREADY MADE
- KEEP THE ARRAY DESIGN SMALL
- SEVERAL SMALL CHIPS MIGHT BE MORE ECONOMICAL THAN ONE LARGE ONE
- LEAVE ROOM FOR CHANGES, GROWTH IN THE BASIC DESIGN
- <u>DON'T</u> USE THE BIGGEST AVAILABLE JUST BECAUSE IT'S THERE
- <u>DO</u> USE AN ARRAY THAT IS BIG ENOUGH

SAMPLE I/O CIRCUITS

CHAP 6 - SAMPLE I/O CIRCUITS
- Q700
- Q1500
- Q3500 TBS


(OLD MACRO GRAPHICS)
No! Use 220 instead
180 1.0
PAD
Z
T M7TB107
ON I/O CELL
160 1.3
A
ZA
B
ZB
T M7TF221
VTI
Threshold generator
Put Buffer Here!
160 1.9
A
B
C
D
E
G M7EF388
VT3
Y
YN
OK
332 6.6
A
AN
PAD
T M7TB101
180 1.0
PAD
Z1
Z2
T M7TB109
280 1.5
A1
A2
ZA
ZAN
T M7TD226
VTI
DRIVER
440 6.9
A
AN
Z
PAD
ENA
T M7TB104
TRANSCEIVER
400 2.0
PAD
THREE STATE DRIVER
ZN
T M7TB105
180 1.0
PAD
Z1
Z2
T M7II109
ON I CELL
120 1.3
A1
A2
Z
ZN
T M7TF220
VTI
440 6.9
A
AN
PAD
ENA
T M7TB102
400 3.0
PAD
THREE STATE DRIVER
ZN
T M7TZ001
ON D CELL
Q700 ONLY
100% TTL
Q700 SERIES
AMCCQ700T
APPLIED MICRO CIRCUITS CORP
DRAWN
DATE
100 PER CENT TTL I/O
SHEET
OF
REV



h-9

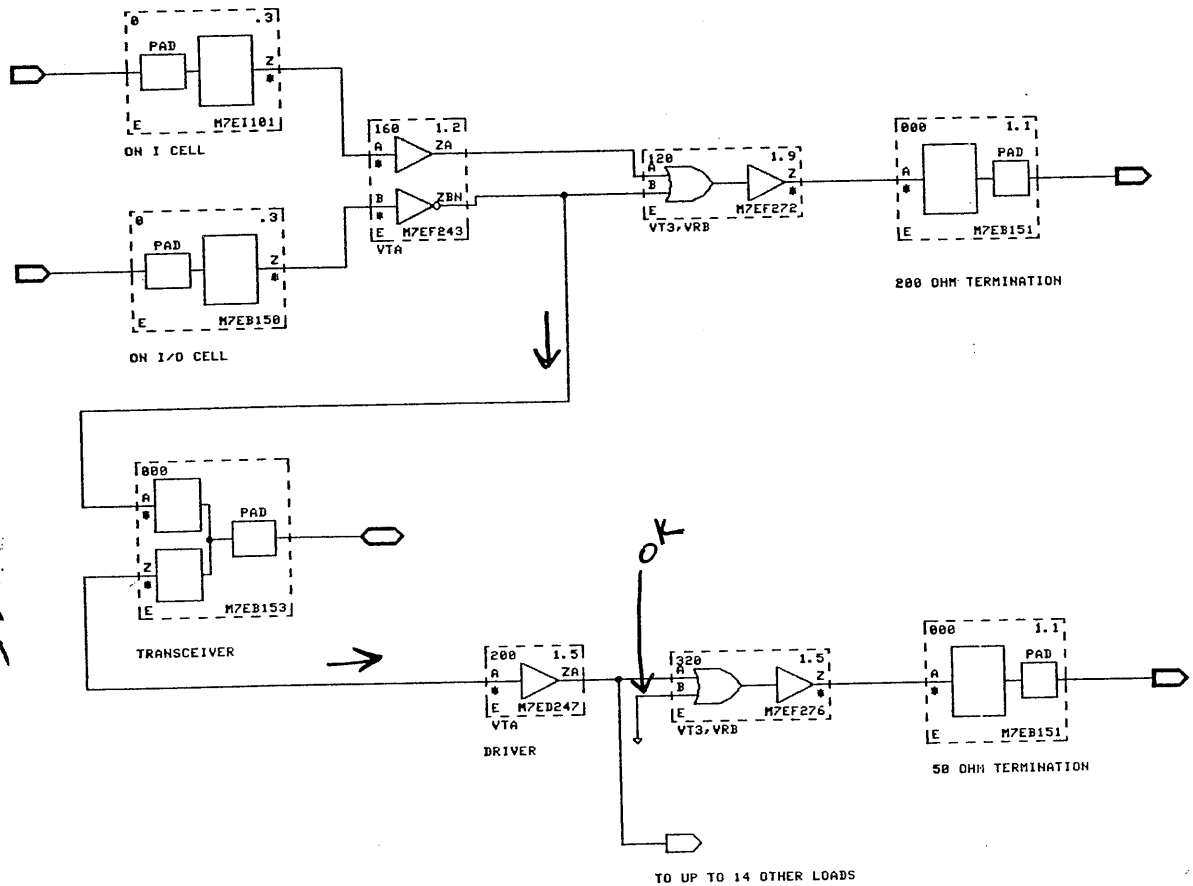
CONNECTORS COMMONLY USED:

OFF-CHIP	OFF-PAGE	INTRA-PAGE
/RWHICON	/RWPICON	/RWIPCON
/RWHOCON	/RWPOCON	/LWIPCON
/RWHBCON	/RWPBCON	/RWBPCON, /LWBPCON

/LWTERM GND AS NAME ON UNUSED INPUT

AMCC0700M		APPLIED MICRO CIRCUITS CORP
DRAWN	DATE	
		TTLMIX
		SHEET OF REV

TTL MIX Q700 SERIES

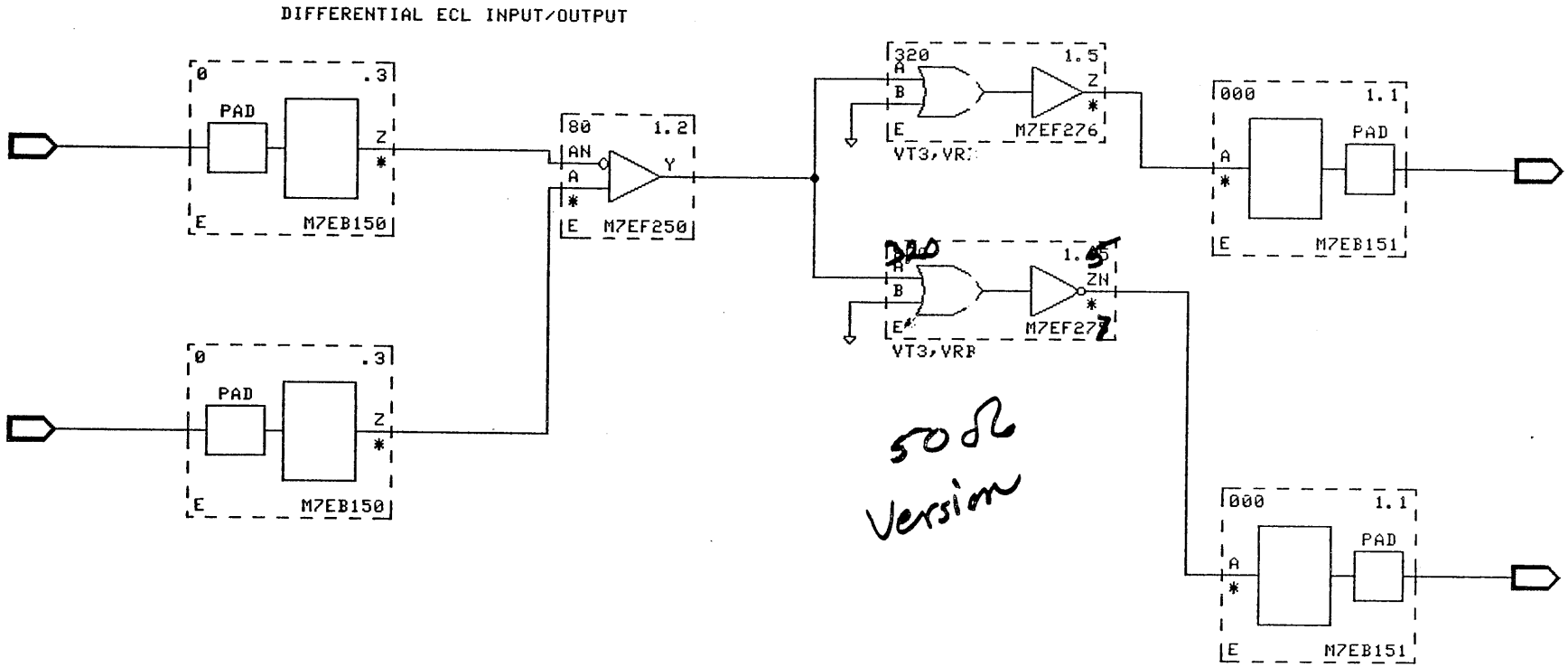


AMCCQ700E		APPLIED MICRO CIRCUITS CORP
DRAWN	DATE	ECL 10K OR 10K/TTL MIX
		SHEET OF REV

100% ECL Q700 SERIES

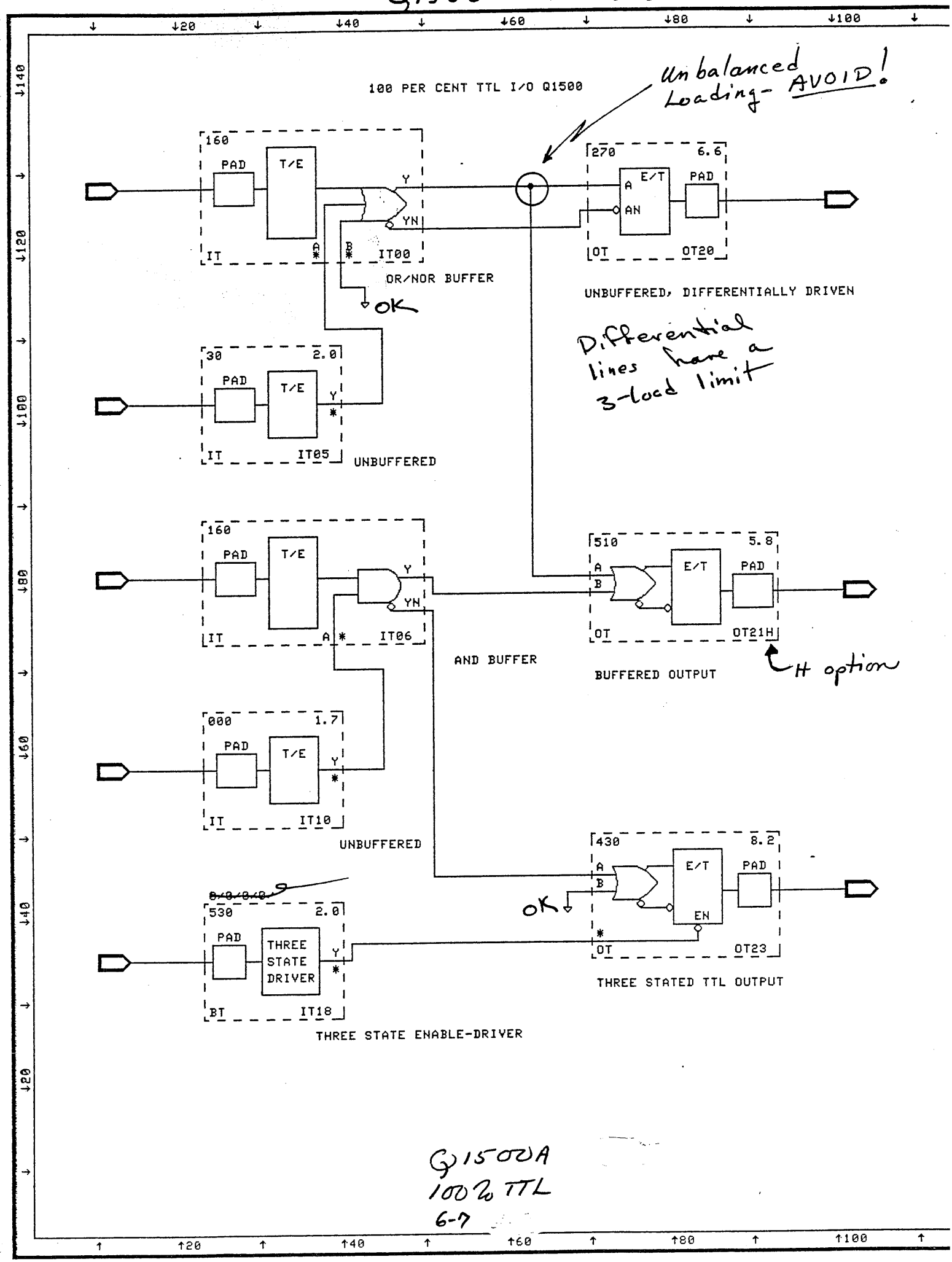
OR

ECL of an ECL/TTL MIXED MODE

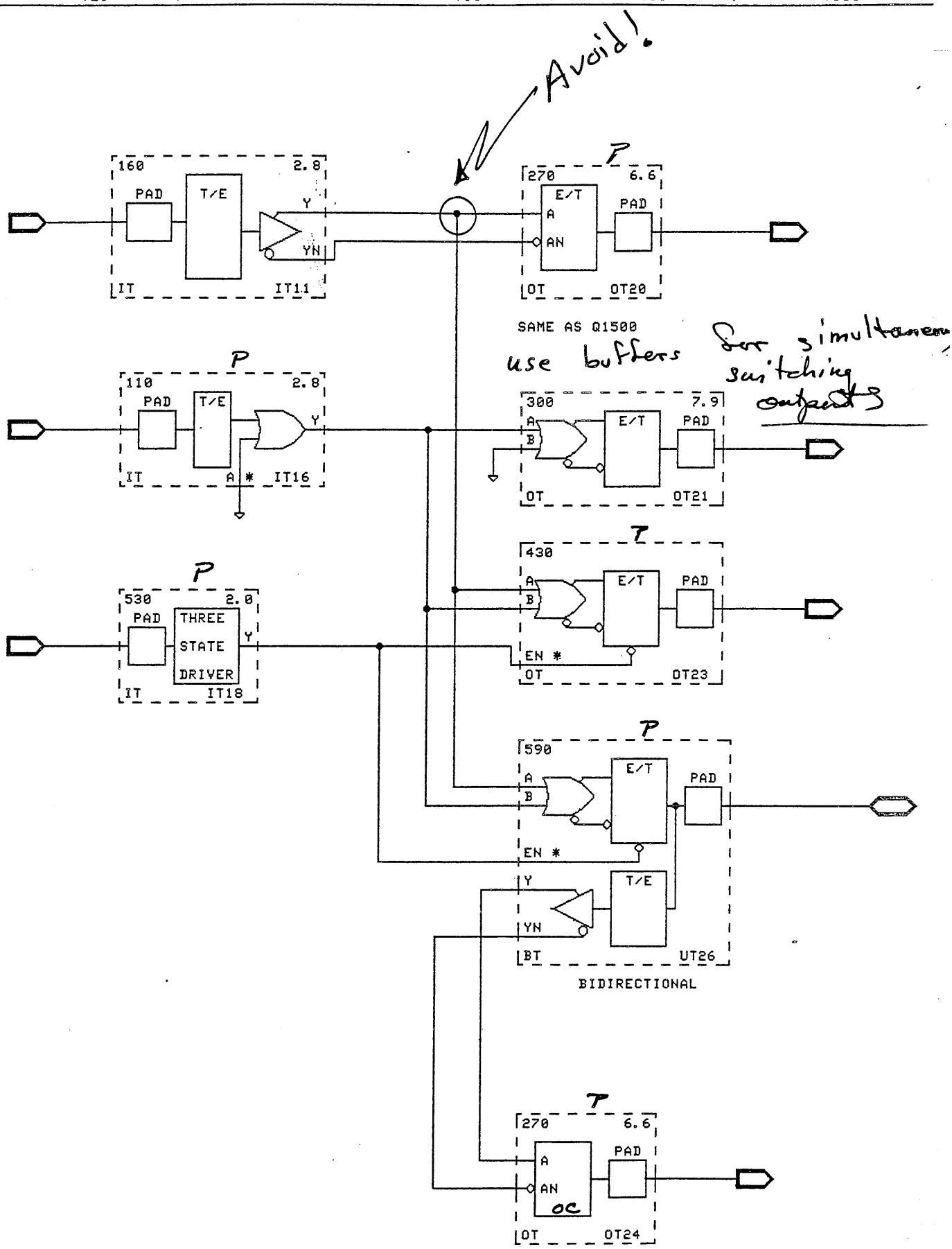


Q700 Differential
ECL Input

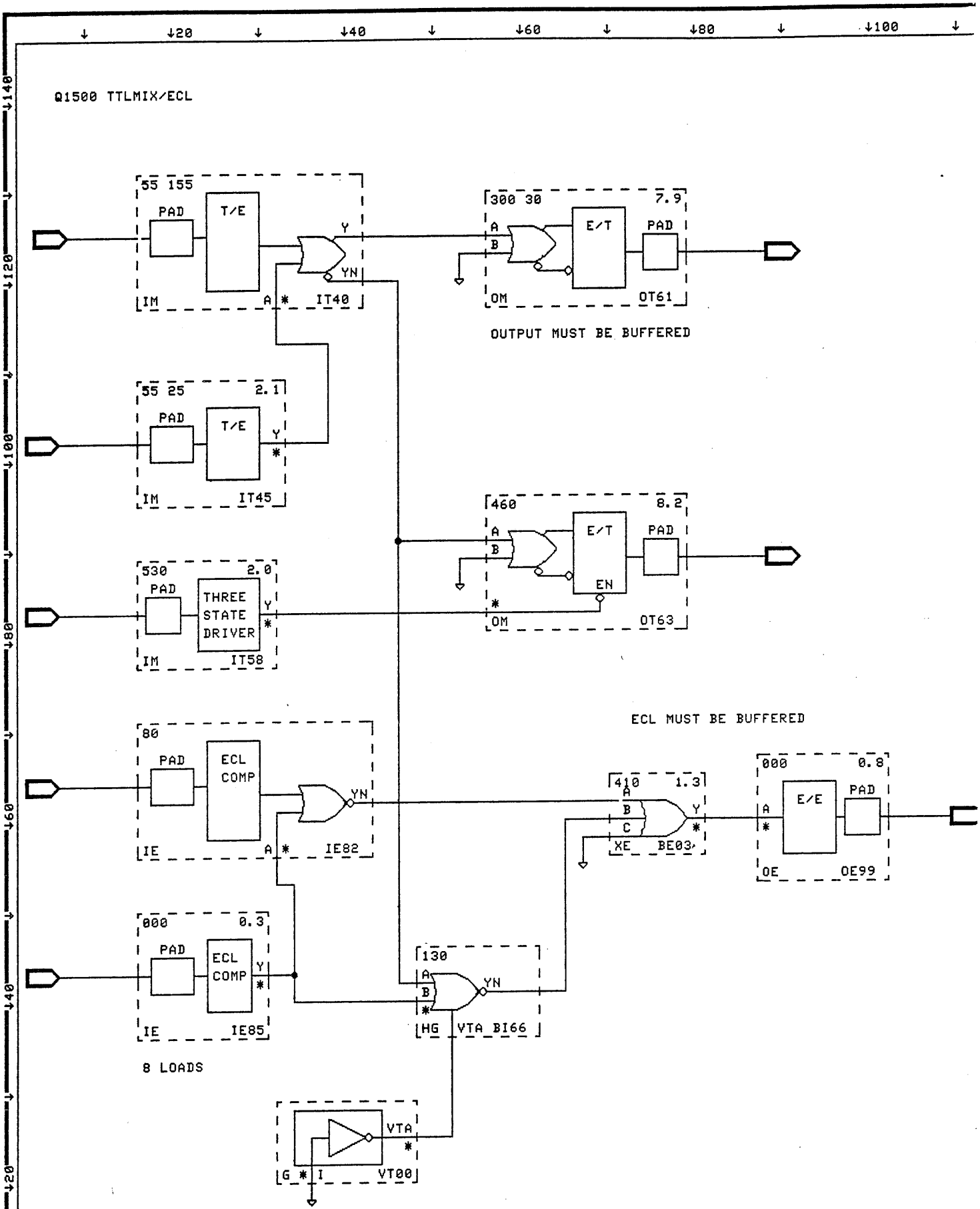
Q1500 100% TTL



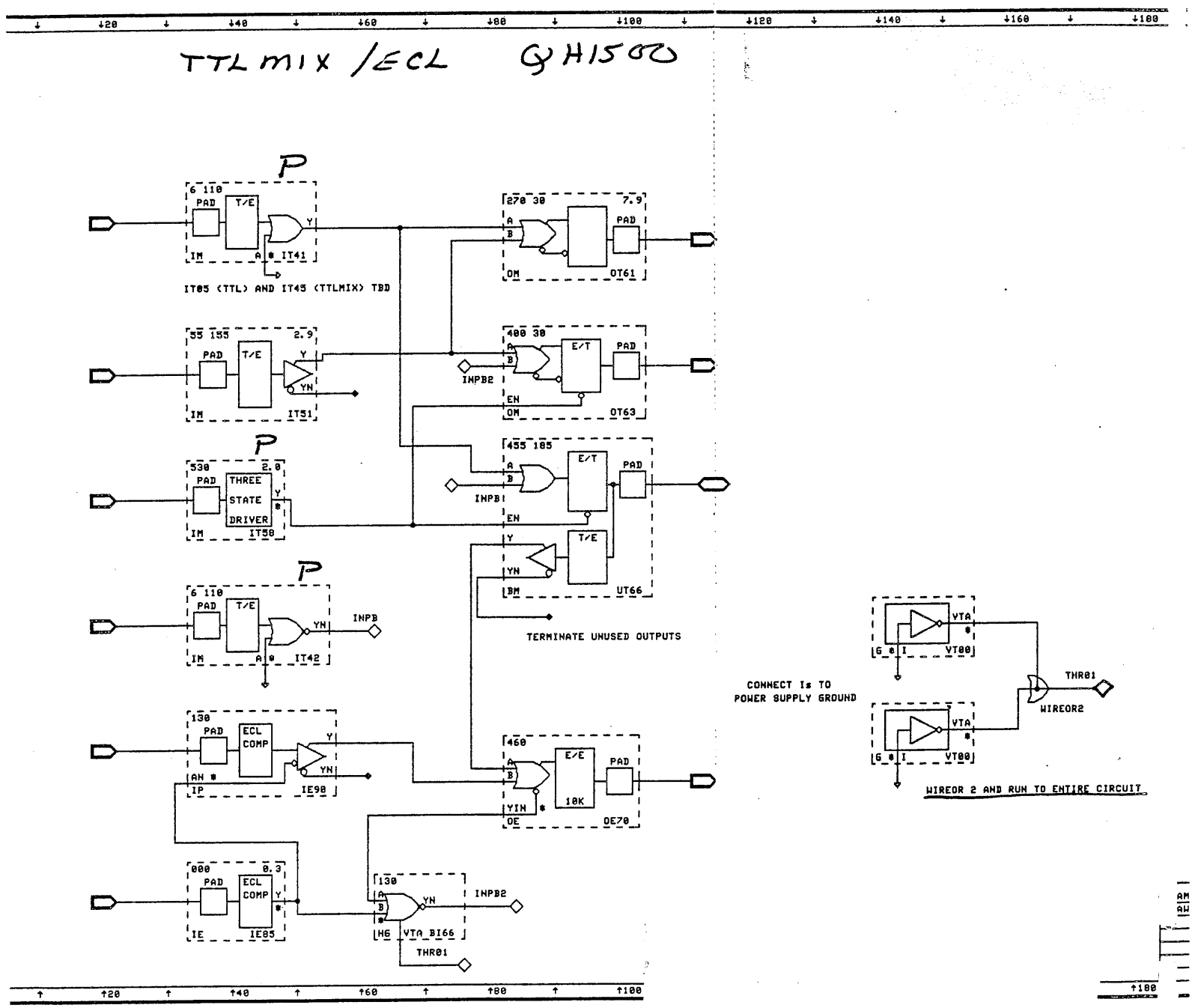
Q1500A
100% TTL
6-7



QH1500A
100% TTL



Q1500A
TTLMIX - ECL


TTL MIX /ECL @ H1500
P
6 110
PAD
T/E
Y
IM
A
IT41
IT05 (TTL) AND IT45 (TTLMIX) TBD
270 30
7.9
A
B
PAD
OM
OT61
55 155
2.9
PAD
T/E
Y
YN
IM
IT51
400 30
E/T
PAD
INPB2
EN
OM
OT63
P
530
2.0
PAD
THREE
STATE
DRIVER
Y
IM
IT58
455 185
E/T
PAD
INPB1
EN
Y
YN
T/E
BM
UT66
TERMINATE UNUSED OUTPUTS
P
6 110
PAD
T/E
YN
INPB
IM
A
IT42
130
PAD
ECL
COMP
Y
YN
AN
IP
IE98
460
E/E
PAD
10K
YIN
OE
OE70
000
0.3
PAD
ECL
COMP
Y
IE
IE85
130
YN
INPB2
H6
VTA_BI66
THR01
VTA
VT00
G
I
CONNECT Is TO
POWER SUPPLY GROUND
THR01
WIREOR2
WIREOR 2 AND RUN TO ENTIRE CIRCUIT

PARTITIONING

CHAP 7 - PARTITIONING A DESIGN
Start - Know thy Array!
Early Considerations
Designing for Testability

- TO SUCCESSFULLY CUSTOMIZE A LOGIC ARRAY YOU MUST BEGIN BY UNDERSTANDING
    - PARTITIONING
    - TESTING
    - LOGIC-MINIMIZATION

- THE NORMAL DESIGN PROCESS
  - PARTITION THE LARGE SYSTEM INTO BLOCKED SUBSYSTEMS
  - FLESH OUT THE HIERARCHY OF FUNCTIONAL BLOCKS
    - WELL-DEFINED INTERFACES
    - PERFORMANCE CONSTRAINTS
  - MAKE THE BLOCKS SMALL ENOUGH TO FIT THE TARGET ARRAYS
  - MAKE INTO EASILY TESTED MODULES
  - CREATE A LOGIC NETWORK
    - LOGIC GATES TO IMPLEMENT A FUNCTION
    - DESIGN DIRECTLY WITH THE MACRO LIBRARY
  - SIMULATE
  - EVALUATE

DESIGN METHODOLOGY

TOP-LEVEL:

- FUNCTIONAL SPECIFICATION
  - WHAT IS REQUIRED
  - DEFINE THE I/O REQUIREMENTS
  - IDENTIFY THE FUNCTIONAL BLOCKS AT THE DESIGN MODULE LEVEL
  - SPECIFY SPEED, POWER, PERFORMANCE REQUIREMENTS
  - PACKAGING
  - TESTABILITY

HIGH-LEVEL ARCHITECTURE:

- DESIGN SPECIFICATION
  - HOW YOU INTEND TO MEET THE FUNCTIONAL SPECIFICATION
  - IDENTIFY CONTROL AND DATA FLOWS
  - IDENTIFY SELECTION CRITERIA FOR INTERFACE BLOCKS
  - SOFTWARE PDL/HARDWARE EQUIVALENT DESCRIPTION
  - IDENTIFY THE FUNCTIONAL BLOCKS AT A LOWER LEVEL

LOWER-LEVEL:

- IMPLEMENTATION SPECIFICATION
  - HOW YOU WILL DO/ARE DOING/DID IT

  - DEFINE THE FUNCTIONAL BLOCKS AT THE LOGICAL DESIGN LEVEL
    - BLOCK DIAGRAM
    - FINAL FUNCTIONAL DESCRIPTION
  - IDENTIFY INTERNAL SIGNAL-PERFORMANCE REQUIREMENTS
    - INTER-BLOCK SIGNAL IDENTIFICATION
    - DETAILED I/O DESCRIPTION
    - DETAILED ELECTRICAL SPECIFICATION
    - DETAILED PACKAGING REQUIREMENTS
    - DETAILED TIMING DIAGRAMS

- START BY PARTITIONING

    - ENSURE THAT EACH MAJOR FUNCTION BLOCK FITS INTO THE TARGET ARRAY
        - MODULAR COMPLEXITY
        - ROUTING

      THESE ARE LIMITING FACTORS FOR UTILIZATION

    - SEGMENT LARGE CIRCUITS INTO BLOCKS WITH AN EFFICIENT RATIO OF LOGIC/I/O

    - SEGMENT INTO EASILY TESTABLE MODULES REMEMBERING THAT TEST GENERATION AND SIMULATION INCREASES WITH THE CUBE OF THE NETWORK SIZE (GENERALLY)

    - PHYSICAL AND LOGICAL PARTITIONING AIDES SYSTEM AND FAULT ANALYSIS

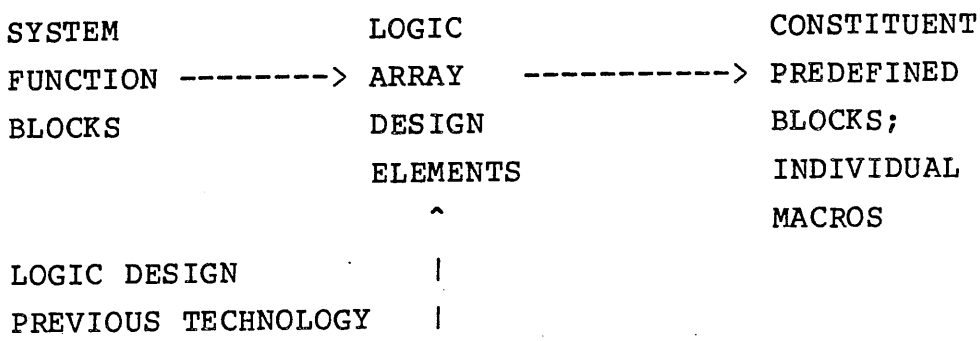
- PARTITION BY GROUPING BY LOGIC FUNCTION
  - SIMPLIFIES SIMULATION
  - SIMPLIFIES TEST GENERATION
  - EASILY RECOGNIZABLE FUNCTIONS

- PARTITION BY GROUPING LOGIC FAMILY
  (TTL, ECL, +5V ECL)

- PARTITION BY CIRCUIT TYPE (DIGITAL, ANALOG)

- PARTITION THE DESIGN VIA:
  - POWER REQUIREMENTS
  - DENSITY
  - I/O QUALITY AND MIX
  - PROPAGATION DELAYS (SPEED, CRITICAL PATHS)
  - INTERCONNECTIONS - MINIMIZE
  - PERFORMANCE
  - SYSTEM MODULARITY
  - TRISTATE ABILITY
  - MECHANICAL CONSTRAINTS
  - TESTABILITY <----------

- A DESIGN CAN BE CONVERTED INTO AN AMCC LOGIC ARRAY FROM THE GATE LEVEL OR FROM THE FUNCTIONAL LEVEL



- STUDY THE MACRO LIBRARY YOU WILL USE
  - LOOK AT OPTIONS FOR THE [redacted] MACROS
  - LOOK AT OPTIONS FOR THE DESIGN
  - LOOK FOR THE LARGER MSI MACROS FIRST

    THEY CAN KEEP SILICON USE DOWN

  - REVIEW MACRO LIBRARY
  - SELECT THE MACROS NEEDED
  - IF NEED A SPECIAL ONE, TALK TO AMCC

- DEVICE CONSIDERATIONS FOR MACRO CONVERSION
  - DEVICE I/O ABILITY
  - CIRCUIT SIZE
  - % UTILIZATION
  - REQUIRED SPEED
  - REQUIRED PERFORMANCE
  - PACKAGE/POWER REQUIREMENTS
  - TESTABILITY

- IF CONVERTING AN EXISTING SSI, MSI DESIGN:
  - DON'T CARRY OVER UNNEEDED FUNCTIONS
    - MULTIPLE ENABLES
    - UNUSED PRESET, CLEAR
    - EXCESS CARRY LOGIC
    - EXCESS LOAD LOGIC
  - DO USE THESE ITEMS IF THEY CAN GO ON AN I/O PIN AND ENHANCE TESTABILITY

  - USE A BOUNDARY LINE DRAWN ON THE EXISTING SCHEMATIC TO DETERMINE THE I/O PINS REQUIRED WHEN FUNCTIONS CROSS BETWEEN ARRAYS

- PARTITION SO PINOUTS ARE CONSISTENT WITH THE SCHEMATIC'S LOGIC FLOW - EASIER TO ROUTE
  - GROUP A REGISTER'S INPUTS TOGETHER AND NEAR THE REGISTER'S CIRCUITRY

- NEVER ALLOW BOUNDARY LINES TO CROSS SPEED CRITICAL SIGNAL PATHS
    - ON-CHIP PROPAGATION IS ALWAYS SHORTER THAN INTER-ARRAY DELAYS

- COMPROMISE BETWEEN TOP-DOWN (STRUCTURED, ORDERLY) AND BOTTOM-UP (BUILD AND TEST SMALL MODULES THEN ADD TO THE DESIGN)
    - ONCE A DESIGN SPECIFICATION EXISTS THE MODULES ARE IDENTIFIED
        - TEST SMALL UNIT FIRST
        - TEST LARGER BLOCKS OF THE DESIGN
        - THEN TEST THE WHOLE DESIGN

- INVESTIGATE YOUR TESTER LIMITATIONS - CAN TEST TTL AND ECL MIXED? OR SEPARATE TESTS? SHOULD YOU NOT MIX TTL/ECL OR TTL/~~PSEUDO~~ +5V ECL?

- BALANCE SILICON EFFICIENCY vs. TESTABILITY

- BALANCE SPEED vs. TESTABILITY

- SERIAL INPUTS SAVE PIN COUNTS BUT ARE HARDER TO TEST

- DON'T FORGET MULTIPLE POWER/GROUND PINS REQUIREMENTS OF THE ARRAY - THIS ALSO CAN REDUCE AVAILABLE I/O
    - TTL INPUTS AND OUTPUTS ARE A HEAVY FACTOR IN THE NEED FOR EXTRA POWER AND GROUND PINS

(THIS WILL BE COVERED IN MORE DETAIL)

- Q7000
- Q15000
- Q3500

} check their Design Guides as well

- SPARE PIN? - ground it!

- DO NOT TIE COMBINATIONAL CELL INPUTS HIGH
    - YOU CAN TIE LOW (TIE ALL UNUSED INPUTS LOW FOR THE DAISY)
    - SEE IF THESE INPUTS COULD BE USED FOR CONTROLLABILITY OR OBSERVABILITY BEFORE GROUNDING THEM

- IF CERTAIN PARTS OF A DESIGN ARE "SOFT"
    - GROUP THESE FUNCTIONS TOGETHER IN A SINGLE ARRAY (IF POSSIBLE)
        - REDESIGN WON'T HURT THE MORE STABLE ARRAYS

- FOR MULTIPLE ARRAYS, LOOK FOR "SAME AS" OR "CLOSE TO" FUNCTIONS
    - IF TWO ARRAYS ARE SIMILAR EXCEPT FOR SOME VARIATIONS, EXPLORE PUTTING BOTH VARIATIONS ON ONE CHIP AND USING THE WIRING TO CONFIGURE THE SPECIFIC VERSION
        - SAVE DESIGN, PRODUCTION COSTS

- PARTITION INTO SMALLER ARRAYS

- DESIGN TO ENHANCE TESTABILITY
- DESIGN TO EASE PRODUCTION PROBLEMS
- LOOK FOR MACROS THAT CAN HELP ESTABLISH CONTROL POINTS
- 3-STATE ELEMENTS ALLOW LOGICAL ISOLATION
- MULTIPLEXERS AND DEMULTIPLEXERS ALLOW MULTIPLE TEST SIGNALS TO APPEAR AT A SINGLE I/O PIN
- PROVIDE A MEANS TO SYNCHRONIZE TESTERS TO ON-CHIP SIGNALS
    - INCLUDE AN OVERRIDE FOR ON-CHIP CLOCK GENERATOR

AMCC
APPLIED MICRO CIRCUITS CORPORATION

- AMCC USES SPICE FOR THE MACRO BUILDING BLOCKS DURING MACRO CONSTRUCTION, EVALUAION
- THE BLOCKS CAN THEN BE VALIDLY UPGRADED TO THE FUNCTIONAL LEVEL SIMULATION FOR THE CIRCUIT
- THE BLOCKS ARE INDEPENDENT OF THEIR SURROUNDINGS

- FUNCTIONAL SIMULATION - LOGIC SIMULATOR
  - BOOLEAN (TEGAS, DLS, DTV)
    - COARSE MEASUREMENT
    - APPROXIMATE TIME DEPENDENCIES (RISE, FALL)
    - CAN TREAT A LARGER NUMBER OF NODES
    - THIS IS THE ONLY LEVEL OF SIMULATOR THAT CAN HANDLE FAULT COVERAGE
    - RUNS FASTER - FEWER CALCULATIONS

- TRANSISTOR SIMULATION (ANALOG)
  (ECAP, SCEPTRE, SPICE)
    - SLOWER
    - FULL VOLTAGE AND TEMPERATURE RANGE
    - HANDLES ANALOG CIRCUITS
    - DETERMINES CRITICAL PERFORMANCE
    - CAN MODEL UNUSUAL LOADING
    - PIECE-WISE INTEGRATION TECHNIQUES TO MODEL DIFFERENTIAL EQUATIONS

- TEST PROGRAM GENERATION
  - IF DONE BY DESIGNER, FASTER
  - DESIGNER KNOWS CIRCUIT BETTER
  - IF DONE BY VENDOR, LENGTHENS DESIGN CYCLE

- THE SUCCESS OF THE TEST VECTORS DEPENDS ON THE TESTABILITY OF THE DESIGN

- DESIGN FOR TEST
  - NO MORE THAN 120 PINS
  - FUNCTIONAL DATA RATES NO FASTER THAN 20 MHz
  - TWO DIFFERENT POWER REQUIREMENTS MAXIMUM
  - I/O SWITCHING: IF POSSIBLE, ALL BI-DIRECTIONAL LINES SHOULD HAVE 3-STATE CONTROL ACCESSIBLE TO A PAD

- USE SPARE INPUTS TO IMPROVE OBSERVABILITY, CONTROLLABILITY

- ADD TEST POINTS (SPARE INPUTS/OUTPUTS, ABOVE)

- AVOID ONE-SHOTS
  - WHERE COMBINATORIAL LOGIC GENERATES A PULSE - ADD A TEST POINT

- BUILD IN SOME SPARE HARDWARE
  - PARITY
  - SHIFT - SERIAL I/O
  - MULTIPLEXED I/O PINS
  - 10% ADDED HARDWARE COULD SAVE $$$ IN THE LONG RUN

- DESIGN DEGATING LOGIC SO THAT BLOCKS OF LOGIC CAN BE DISABLED FOR TESTING

- IN A BUS ORIENTED DESIGN, PLACE CONTROL INFORMATION ON THE BUS TO ENABLE/DISABLE BLOCKS OF LOGIC - NO ADDED I/O PINS USED IF DONE THIS WAY

- CONSIDER REPLACING J-K AND S-R F/F WITH D F/F
  - SIMPLER TESTING
  - OCCUPY LESS REAL-ESTATE

- CONSIDER REPLACING EDGE-TRIGGERED STORAGE WITH LATCHES
  - IF YOU DON'T ABSOLUTELY REQUIRE THE EDGE TRIGGERED STORAGE
  - LATCHES BECOME TRANSPARENT FROM I TO O AND ALLOW TESTING WITH RELATIVELY FEW I/O AND CLOCK CYCLES

- USE A TRANSPARENT LATCH INSTEAD OF A F/F FOR INITIALIZATION

- IF THE SEQUENTIAL CIRCUITS ARE NOT RESETTABLE, BE CERTAIN THEY INITIALIZE IN A FEW STEPS (< 100); MAKE CERTAIN THEY CAN BE INITIALIZED

- USE F/F WITH CLEAR PINS TIED TO RESET

- BREAK UP COUNTER CHAINS (<8)

- USE A SETTABLE COUNTER

- CONNECT ALL SEQUENTIAL LOGIC SO YOU CAN INITIALIZE THEM FROM PRIMARY CIRCUIT INPUTS

- USE CELLS WITH PRESET AND CLEAR LINES

  OR

  ENSURE THAT ALL DATA AND CLOCK LINES ARE ACCESSIBLE FOR TEST-PATTERN LOADING

- IF POSSIBLE, INCLUDE A MASTER RESET TO DRIVE ALL SEQUENTIAL DEVICES TO A KNOWN STATE

- PROVIDE ALL SYNCHRONOUS COUNTER CIRCUITS WITH INDEPENDENTLY CONTROLLABLE CLOCK, PRESET AND CLEAR INPUTS

- EXAMINE WAYS THAT UNUSED Q AND QN OUTPUTS CAN BE USED TO ENHANCE TESTABILITY
  - EXTRA OUTPUTS COULD BE CONNECTED TO A PARITY TREE - ONE PIN COULD SIGNAL INTERNAL ERRORS

- LATCHES

  COUNTERS

  SHIFTERS

  DATA REGISTERS:

    - "DATA" MUST BE HELD STEADY ONE UNIT PERIOD BEFORE AND ONE UNIT PERIOD AFTER THE ACTIVE OR TRIGGERING TRANSITION OF THE CLOCK SIGNAL

    - NO ZERO SETUP TIME

    - NO ZERO HOLD TIME

    - A.C. SPEED TESTS MUST BE SEPARATELY DEFINED AND QUOTED

- POINT OF OUTPUT INITIALIZATION MUST BE INDICATED

- KEEP TRACK OF THE LOADING CONNECTED TO EACH DEVICE
  - PROP TIME IS LOAD-DEPENDENT
  - USE HIGH-FANOUT DEVICES WHERE LOADING IS REQUIRED, (OR CASCADE SEVERAL STANDARD CELLS)
  - CLOCK AND ENABLE LINES ARE USUALLY HIGH-FANOUT
  - FOR OTHER FUNCTIONS - MODIFY THE DESIGN
    - WATCH RECOMMENDED MARGINS

- DERATE LOADING FOR CLOCK LINES
  FOR DISTORTION SENSITIVE LINES
  - USE 20% DERATING
  - USE P OPTION FOR 6 LOADS ON A CLOCK LINE
  - USE DRIVERS FOR 9-12 LOADS ON A CLOCK LINE
  - USE 2 MACROS IN PARALLEL, EVEN DISTRIBUTION OF LOAD FOR 15 LOADS - 24 LOADS, ETC.
- DERATE LOADING FOR TTL LOGIC DRIVING OUTPUTS (DIFFERENTIAL DRIVE, 100% TTL)

- DIFFERENT CLOCKS MAY BE APPLIED
- INTERMITTANT BURST CLOCK PATTERN PERMITTED
- IF USING MULTIPLE CLOCK FREQUENCIES, USE ONE MASTER CLOCK AND A CHAIN OF DIVIDE-BY-X COUNTERS
    - IMPROVE CIRCUIT SYNCHRONIZATION
    - CAN OVERRIDE WITH ONE SIGNAL
    - DON'T EXCEED THE MAXIMUM FANOUT FOR THE MASTER CLOCK!

- CONTROLLABILITY

  - THE DEGREE TO WHICH THE LOGIC STATES OF THE INTERNAL NODES CAN BE CONTROLLED FROM THE PRIMARY OUTPUTS
    - CAN IT BE INITIALIZED
    - CAN IT BE DRIVEN WITHOUT THE REST OF THE SYSTEM

- OBSERVABILITY

  - THE DEGREE TO WHICH THE LOGIC STATE OF THE INTERNAL NODES CAN BE DISCERNED AT THE PRIMARY OUTPUTS
    - CAN YOU SEE THE RESULT OF EVERY FAULT OR LEVEL CHANGE

- PREDICTABILITY
  - THE DEGREE TO WHICH THE BEHAVIOR OF THE SYSTEM NODES CAN BE INFERRED, ESP. THE BEHAVIOR OF THE PRIMARY OUTPUTS
    - DO YOU KNOW WHAT WILL HAPPEN WHEN A CHANGE IS MADE
    - DO YOU KNOW WHAT WILL HAPPEN WHEN A FAULT OCCURS
    - CONCERN IS WITH THE GENERATION OF AN INDETERMINENT STATE (SAX) OR ONE FROM WHICH THERE IS NO EXIT

- TESTABILITY

  - PROVIDING READILY ACCESSIBLE CONTROL AND OBSERVATION PATHS TO ALL FUNCTIONAL UNITS WITHIN A DEVICE

  - THE DEGREE TO WHICH A CIRCUIT MAY BE TESTED FOR FAILURE, HARD OR SOFT

- FAULT COVERAGE
  - HOW MANY SA1 AND SA0 FAULTS ARE DETECTED BY THE USER-SUPPLIED TEST VECTORS
  - 95% COVERAGE IS RECOMMENDED FOR A PRODUCTION RUN
  - 70% COVERAGE IS CONSIDERED ADEQUATE FOR A PROTOTYPE (70-75%)
- FAULTS ARE USUALLY SA1, SA0 SINGLE FAULTS
- SOME MULTIPLE FAULTS WILL BE DETECTED
- COMPLETE COVERAGE
  - ALL POSSIBLE, OBSERVABLE, SINGLE STUCK-AT (SA1, SA0) FAULTS ARE COVERED BY SOME TEST IN THE TEST SET
- FAULT GRADING
  - THE PROCESS OF DETERMINING THE % COVERAGE ACHIEVED BY A GIVEN SET OF TESTS

AMCC
APPLIED MICRO CIRCUITS CORPORATION

Schematic Rules

AMCC
APPLIED MICRO CIRCUITS CORPORATION

CHAP 8 - AMCC SCHEMATIC RULES
How to interface to our support software
as well as the software on the EWS
and the TEGAS fault grading, etc.

• DO NOT ALTER/MODIFY/CHANGE THE LIBRARIES, THE MACROS, OR THE SIFT FILE. THE RESULTING SCHEMATIC CANNOT BE MANUFACTURED.

• ONLY AMCC-CREATED COMPONENTS CAN BE USED ON THE SCHEMATIC, EXCEPT FOR THE DAISY STANDARD CONNECTORS AND TERMINATORS

EXAMPLES:

/LWTERM /RWHICON /RWHOCON

• ERC FILE MACRO_TAB.DOC WILL LIST MACRO USAGE
→ macroccur -VAX

• EVERY DRAWING PAGE (DED 1, DED 2, ETC.) MUST HAVE A BORDER. A BORDER IS CALLED UP LIKE ANY OTHER COMPONENT AND SHOULD TYPE MATCH THE COMPONENTS USED IN THE DESIGN. BORDERS WILL BE MOVED INTO THE LIBRARIES ON SOME FUTURE RELEASE.

EXAMPLES:

/AMCCQ700T	Q700 BASED, TTL ONLY
/AMCCQ1500E	Q1500 BASED, ECL GND REF. ONLY
/AMCCQ700M	Q700 BASED, TTL AND GND REF ECL MIXED

• ERC FILES BORDER_ERR.ERR WILL FLAG VIOLATIONS

• ALL MACRO COMPONENTS MUST HAVE A USER-DEFINED NAME. THE ONLY EXCEPTIONS ARE TERMINATORS. DAISY HAS DEFAULT NAMES, THE TEGAS FILES ARE MORE UNDERSTANDABLE WITH USER-DEFINED NAMES.

• ERC FILE VALIDNAMES.ERR WILL FLAG NAME VIOLATIONS
• ERC FILE UNNAMED.ERR WILL FLAG UNNAMED COMPONENTS
→ VALID NAME ON VAX ERCS

AGIF-BASED ERC'S

1) CHIP FAMILY - Checks to make sure all components are from same chip family (no mixing of Q700 and Q1500, etc.).

2) CHIP TECHNOLOGY - Checks to make sure all I/O's are of correct type (if 100% ECL, then all ECL I/O's).

3) FANOUT- Checks to make sure that fanout is not exceeded for each output pin.

4) ECL 10K/100K - Checks to make sure that if the circuit is 10K, that only 10K I/O's are used.

5) VALID NAMES - Checks to make sure that user-defined component and signal names are 6 alphanumeric characters maximum and that reserved words are not used. Also checks for uniqueness.

6) PIN CLASS - Checks to make sure that special pins are connected to pins of a like class.

7) UNUSED PINS - Checks to make sure that unused pins are grounded (inputs) or terminated (outputs).

8) WIREOR - Checks to make sure that wireors aren't connected to wireors and that parameterized wireor has correct parameter.

9) PIN COUNT - Does a count of pins. This is used as a guideline for routeability.

10) POWER DISSIPATION/MACRO OCCURANCE - This totals up power dissipated by the circuit and also shows macros used in circuit. Is formatted so that the table can be used in CSPEC.

11) POPULATION - Checks to see how many cells will be occupied on circuit so that over population cannot occur.

12) PIN HOOKUP - Checks to make sure that pins which must be hooked up are used by the designer.

****

MACRO OCCURENCE AND
POWER DISSIPATION TABLE
Revision 1.0.0

****

Path name /USER/DEW/MOBIUS
Family G1500
Work station DAISY
Technology T
Date 29-OCT-1984
Time 14:48

The following is the macro occurence table -

MACRO NAME	# USED	SPECS ICC	SPECS IEE	TOTALS ICC	TOTALS IEE
FF11	4	0.00	2.85	0.00	11.40
OT25	4	6.00	0.00	24.00	0.00
IT01	2	1.10	0.00	2.20	0.00
TOTAL TYP MACRO CURRENT				26.20	11.40
TOTAL TYP OVERHEAD CURRENT					
TOTAL TYP CHIP CURRENT					
TOTAL MAX CHIP CURRENT (TYP CURRENT TIMES 1.4) =					
TOTAL CURRENT =					
WORST CASE POWER DISSIPATION					
VCC ( )v X ( )ma =					Watts
VEE ( )v X ( )ma =					Watts
ECL OUTPUT POWER DISSIPATION					
( )ma X 1.3v X ( )outputs=					Watts
TOTAL POWER DISSIPATION					Watts

• MACRO NAMES SHOULD BE IN THE FORMAT Tnnn, where T DESIGNATES A FUNCTIONAL TYPE AND nnn IS A UNIQUE NUMBER WITHIN THE TYPE GROUP.

T: S => LEVEL SHIFTER, INPUT CELLS
B => BUFFERS
G => COMBINATIONAL GATES
L => LATCHES
F => FLIP-FLOP
M => MULTIPLEXORS
D => OUTPUT DRIVER (PAD MACRO)

See Next Page

• DIE PAD NUMBERS SHOULD BE PLACED INSIDE I/O MACRO PAD BLOCKS AS MACRO NOTES. (when known, esp preplacement)
USE THE FORMAT nn WHERE nn IS ANY ONE - TWO DIGIT NUMBER

• ADDITIONAL NOTES FOR RESTRICTIONS, COMMENTS ETC. CAN BE ADDED AS A DOCUMENTATION AID.

• CONNECTORS ARE NAMED BY NAMING THE WIRE TO WHICH THEY ARE ATTACHED.
PLACE THE WIRE NAME ON THE EXTREME LEFT (FOR INPUT CONNECTORS) OR THE EXTREME RIGHT (FOR OUTPUT CONNECTORS) OF THE CONNECTOR.

- ALL OFF-COMPONENT CONNECTORS (EXTERNAL PINS) MUST BE NAMED. - BY NAMING THE WIRE
- ALL OFF-PAGE CONNECTORS MUST BE NAMED, WITH AN ADDED NOTE (ALSO ATTACHED TO THE WIRE AND NOT TO THE CONNECTOR ITSELF) INDICATING THE CONNECTING PAGE. PLACE THE NOTE BENEATH THE CONNECTOR.

- ALL PINS OF ALL MACROS MUST BE CONNECTED TO A WIRE.

    - ALL UNUSED INPUTS MUST BE GROUNDED.
        - GROUND ALL UNUSED PINS OF ONE MACRO IN ONE NET NAMED GND

        - ERC FILE UNUSED_PIN.ERR WILL FLAG VIOLATIONS
          → UNUSED PINS — VAX
    - ALL UNUSED OUTPUTS MUST BE TERMINATED.
        - EACH UNUSED OUTPUT REQUIRES ITS OWN TERMINATOR AND THE TERMINATOR MUST BE WIRED TO THE COMPONENT (PLACING IT CLOSE WILL NOT CONNECT IT!)

        - ERC FILE GND_OUTP.ERR CHECKS THAT NO OUTPUTS HAVE BEEN CONNECTED TO GROUND
          → UNUSED PINS — VAX

- ALL NAMES OF A GIVEN CLASS (SXX, BXX, GXX, ETC) MUST BE UNIQUE FOR THE ENTIRE CIRCUIT. THIS INCLUDES THE NAMES GIVEN TO INPUT CONNECTOR AND PAGE CONNECTOR WIRES.

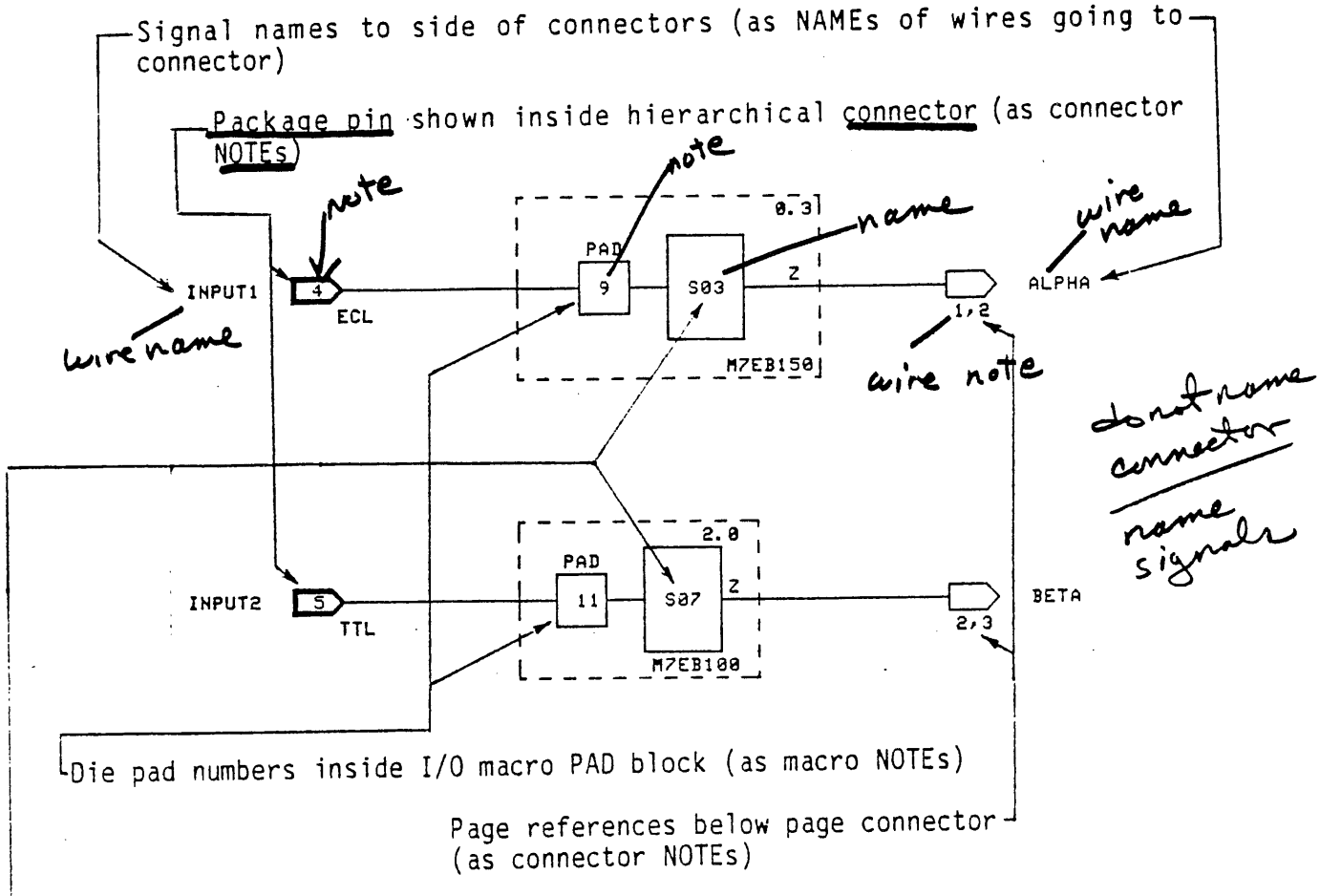
- GROUNDED INPUTS ARE NAMED GND, THE NAME DOES NOT APPEAR, BUT THE GROUND SYMBOL DOES. GND IS A GLOBAL NAME.

- NAMES MUST BE FORTRAN-RULES, (6 CHARACTERS, ALPHA-MERIC) THIS IS TRUE FOR WIRES. ADD NOTES IF FURTHER CLARITY IS DESIRED. (6 char limit is from Text)

- NAMES CANNOT BEGIN WITH THE LETTER Z (RESERVED FOR WIRE-ORS)

- NAMES SHOULD BE GREATER THAN 2 CHARACTERS TO AVOID USING PIN NAMES (I0, I1, Y, ETC)

- PACKAGE PIN NUMBERS ARE SHOWN INSIDE HIERARCHICAL CONNECTORS IN DECIMAL FORMAT (nn), A CONNECTOR NOTES (ATTACHED TO THE WIRE)
  - THESE NUMBERS ARE NOT NECESARY FOR PROCESSING, AND CAN BE ADDED LATER, BY HAND IF NECESSARY. THEY ARE FOR DOCUMENTATION ONLY.

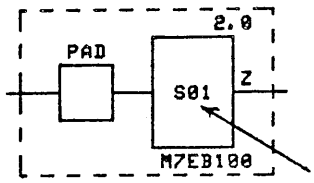


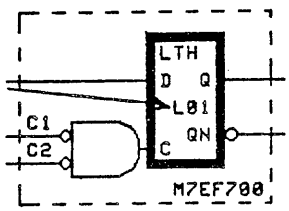
The macro reference designators are a maximum of four characters and have the following format:

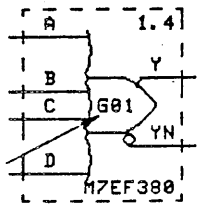
TNNN

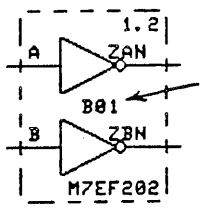
where T is the functional type and NNN is a number unique within the type group.

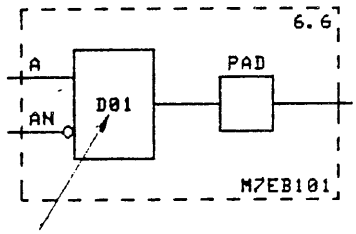
→ Use bidirectional connector for bidirectional macros: UTxx, etc

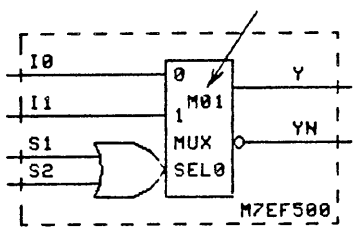




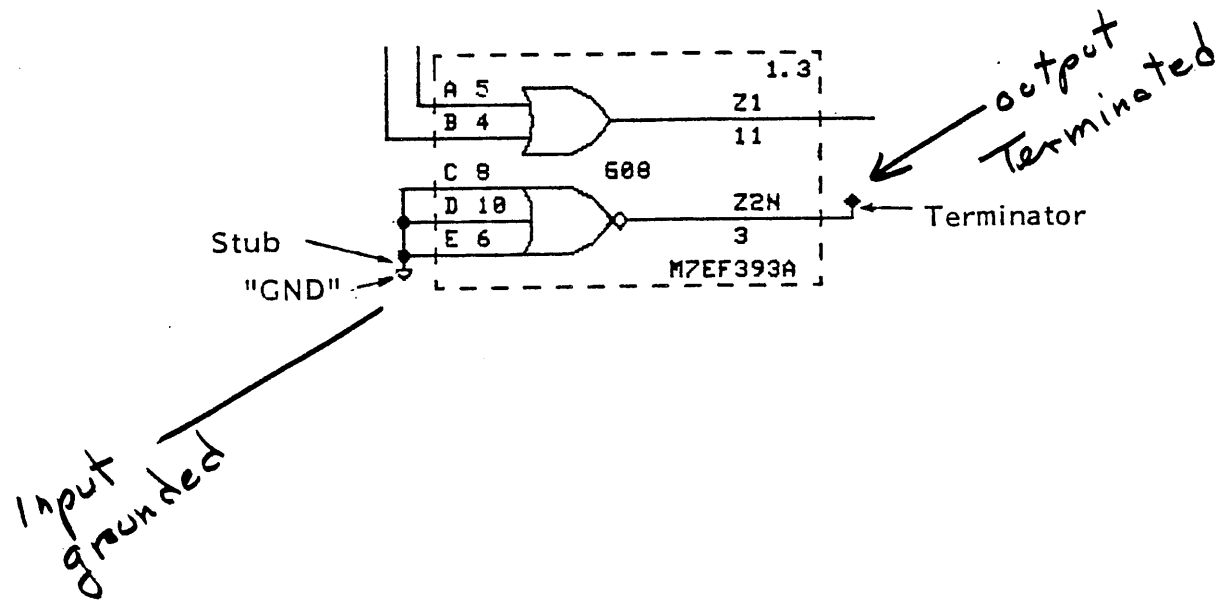








Reference Designator Conventions


1.3
A 5
B 4
Z1
11
C 8
600
D 10
E 6
Z2N
3
MZEF393A
Stub
"GND"
Terminator
output Terminated
Input grounded

- NO MACRO CAN BE USED TO DRIVE MORE OUTPUTS THAN ITS RATING. STANDARD MACROS DRIVE 6 LOADS, HIGH-SPEED POWER OPTIONS DRIVE UP TO 9 LOADS. SPECIAL DRIVER MACROS ARE THE ONLY EXCEPTIONS.

    - ERC FILE FANOUT.ERR FLAGS ALL MACROS WHICH HAVE EXCESSIVE FANOUT LOADS.

- ERC FILE PIN_COUNT.DOC CHECKS THE SCHEMATIC PIN COUNT. IT SHOULD BE USED AS A REFERENCE DOCUMENT.

- There is no check for derated limits — up to designer

AMCC SUMMARY OF CONVENTIONS FOR SCHEMATICS

AMCC
APPLIED MICRO CIRCUITS CORPORATION

- Use 4-6 Alphanumeric characters (A-Z, 0-9) for all macro names and for all wire names
- All macros must be named
- Do not use macro pin names as macro or wire names
- All names must be unique within a circuit
- All inter- and intra- page connections and all off-chip connections must be named - name the wire and NOT the connector
- All inter- and intra- page connections must be commented as to the pages to which they go to/come from
- All I/O macros must be commented as to type and use (ECL, TTL, TTLMIX, +5V ECL, simultaneously switching, etc.)
- All unused inputs are grounded (except AND inputs) - tie them to an inverter whose input is grounded
- Ground is a global name
- All unused outputs are terminated
- Terminators are not named
- All pages must be numbered, should be named for EWS
- WIREORx macros are named
- Follow AMCC naming conventions:

A____	=	Adder
B____	=	Buffer
G____	=	Gate
EX___	=	Exclusive or/nor
M____	=	Mux
DE___	=	Decoder
F____	=	Flip flop
L____	=	Latch
MM___	=	Memory module
MI___	=	MSI macro
SP___	=	Special cell
LS___	=	Inputs
D____	=	Outputs
BD___	=	Bidirectional I/O
W____	=	Wireors
X____	=	None of the above

APPLIED MICRO CIRCUITS CORPORATION

Q700 DESIGN EXAMPLES

CHAP 9 - SAMPLE DESIGNS
- Q700 (in design guide)
- Q1500
- Q3500 (a.k.a. Application Note 5)

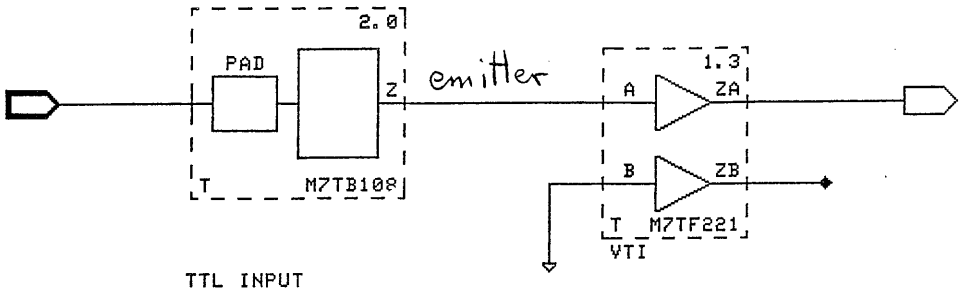
INPUT-BUFFER RESTRICTIONS

In applying the Q700 macros, care must be taken to honor the restrictions listed in the individual macro descriptions. For example, input macro M7TB108, for 100% TTL or TTL in a +5V-Ref ECL/TTL mixed circuit, is restricted as to the input buffer to which it can be connected. M7TB108 MUST be connected to an input buffer in the series M7TF22n, n = 1, 3, 4, 7, or 8.

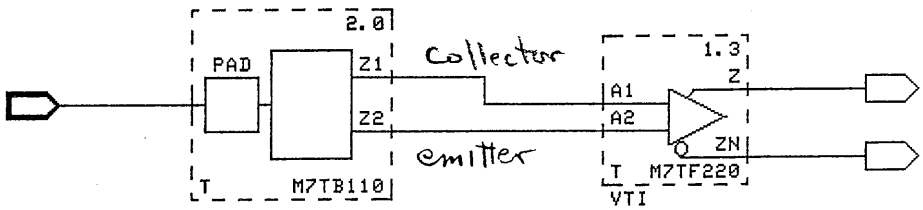
- THE FOLLOWING PAGE DEMONSTRATES SOME OF THE TTL BUFFER AND OUTPUT PAD MACROS AVAILABLE ON THE Q700
  Single Input output is Emitter
  Dual Input macro outpus is Emitter-Collector (inver
- INPUT, OUTPUT, EXTERNAL PINS AND INTER/INTRA PAGE CONNECTORS ARE REQUIRED TO MAKE A CIRCUIT SCHEMATIC COMPLETE

- DAISY ALSO REQUIRES THAT ALL UNUSED INPUTS BE GROUNDED (THEY ARE NOT ACTUALLY GROUNDED IN THE FINAL IMPLEMENTATION BUT FLOAT UNLESS REQUIRED TO BE OTHERWISE)

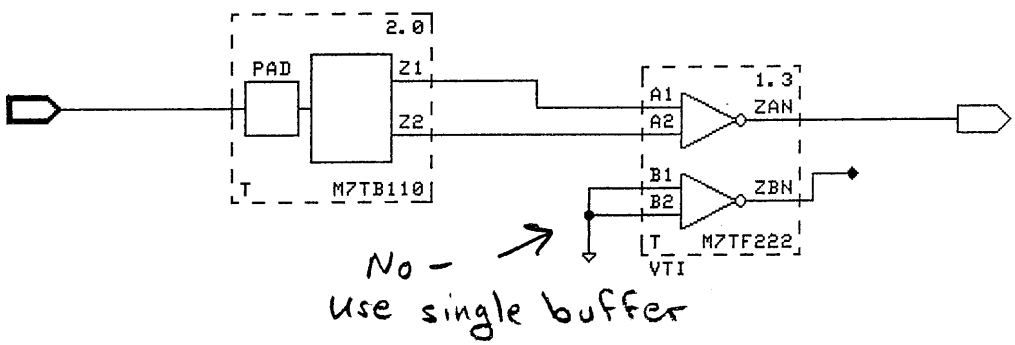
- ALL UNUSED OUTPUT PINS ARE TO BE TERMINATED USUALLY USING THE /LWTERM MACRO



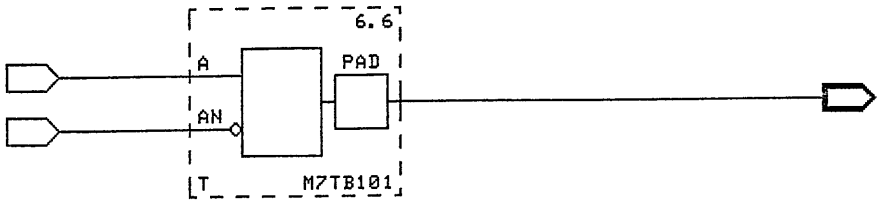
TTL INPUT



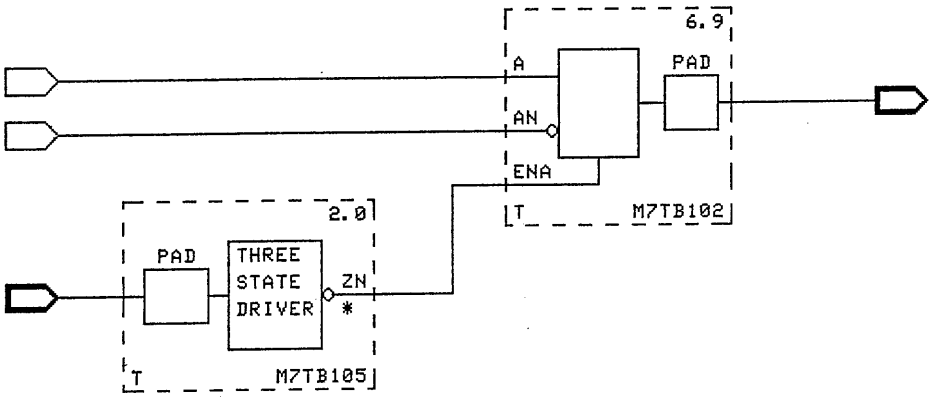
TTL INPUT - COMPLEMENTARY OUTPUTS



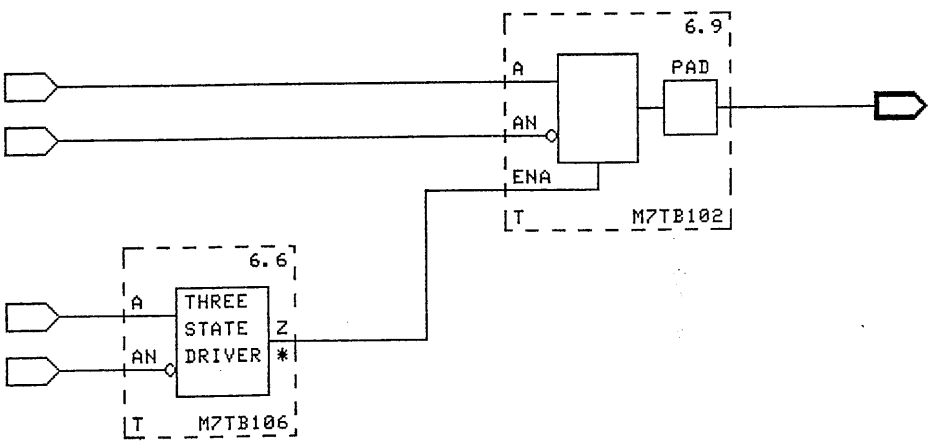
TTL INPUT - INVERTING



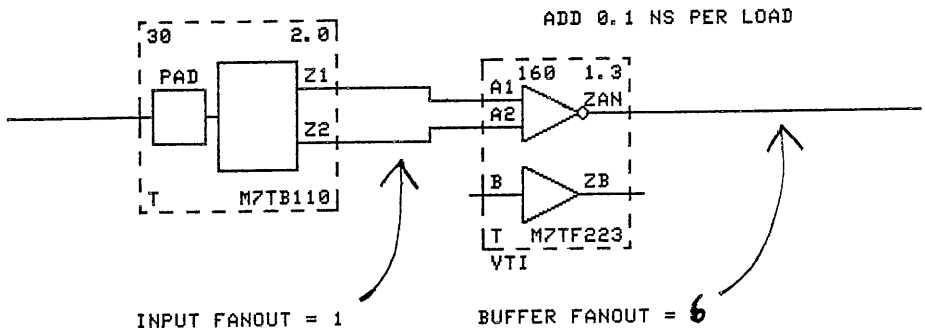
DIFFERENTIAL OUTPUT FROM INTERNAL LOGIC
(From same macro)



T T L OUTPUT



DIFFERENTIAL OUTPUT FROM INTERNAL LOGIC


ADD 0.1 NS PER LOAD
30
2.0
PAD
Z1
Z2
T
M7TB110
160
1.3
A1
A2
ZAN
B
ZB
T
M7TF223
VTI
INPUT FANOUT = 1
BUFFER FANOUT = 6
POWER-OPTION FANOUT = 9
SPECIAL DRIVERS FANOUT = 15
DERATE CLOCK 20-40 PER CENT

FANOUT RESTRICTIONS

Care must also be taken so that fan-out rules are not violated. A standard input buffer, M7TF228, can drive up to and including 6 loads. Two buffers wire-ORed cannot drive more than 6 loads. Given a requirement for a signal to drive 15 loads, a single buffer macro is inadequate. Two standard buffer macros can be used to drive a load of 12 if the load is DIVIDED between the two buffers. The general rule is to balance such divisions. Using the power option version of the buffer macro, each buffer can handle up to and including 9 loads.

Figure EX.1 diagrams input macro M7TB110 and the power-option version of the input buffer M7TP222, showing how to divide a 15-load fanout between buffers (split loading). Figure EX.2 shows another solution for the high-fanout problem, using the high-fan-out driver buffer M7TD228 to drive all 15 loads from one buffer.

NOTE: When driving high-fanout with a clock signal, the allowable fan-out should be derated by 20% MINIMUM in a standard circuit, or higher (up to 40% for high-speed applications).

- THE NEXT FOUR PAGES HIGHLIGHT THE OPTIONS AVAILABLE WHEN THERE IS A REQUIREMENT FOR HIGH FANOUT FOR A SIGNAL (NON-CLOCK)

- THE STANDARD MACRO FANOUT IS 6 LOADS ($n \leq 6$)
  THERE ARE POWER-OPTIONS AVAILABLE FOR MOST MACROS (IDENTIFIED IN THE DESIGN GUIDE)

- GIVEN A 15-LOAD REQUIREMENT, USE THE POWER OPTION FOR THE BUFFER AND USE TWO BUFFERS

    - DO NOT WIRE-OR TWO BUFFERS TO INCREASE FANOUT CAPABILITY!

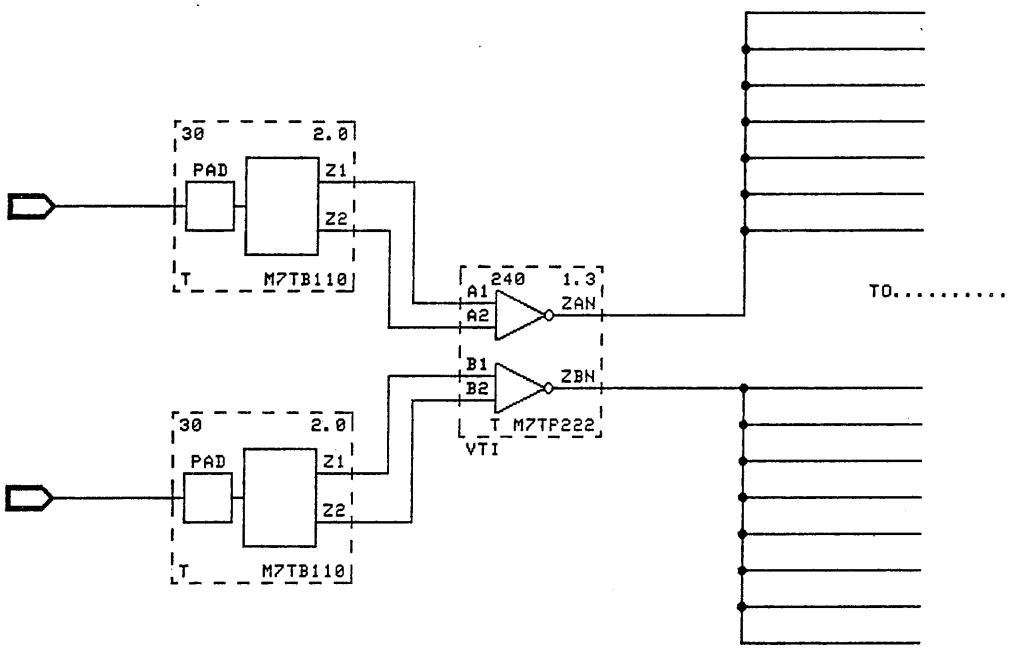
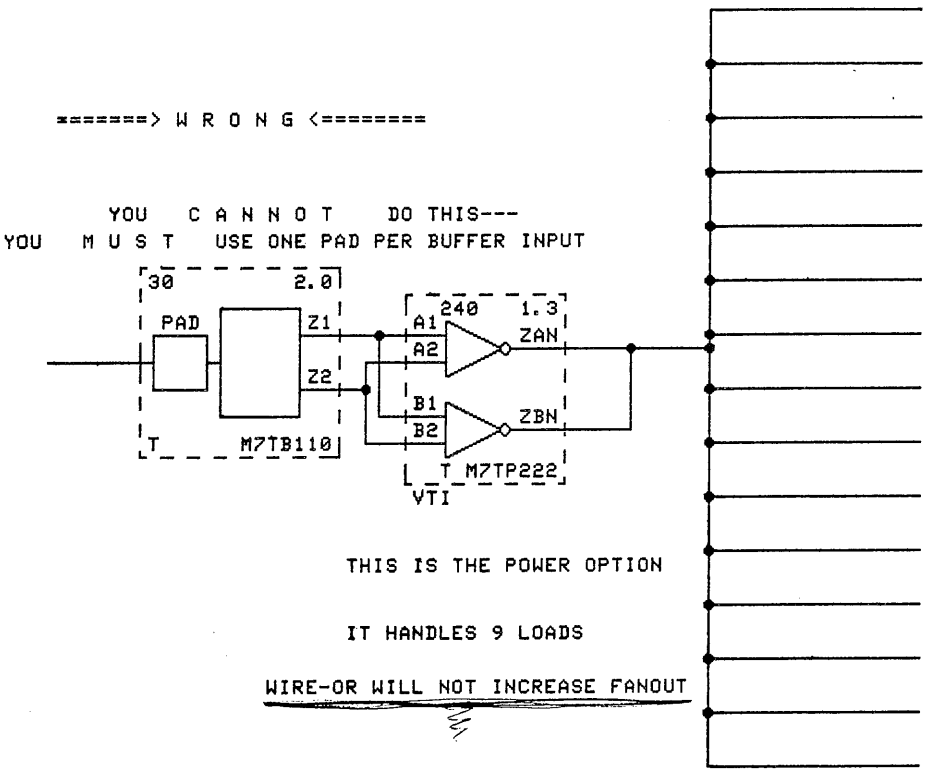
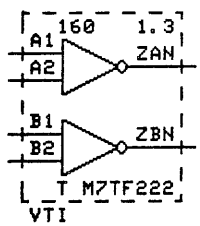


Figure EX.1. Power-option buffer loading. Buffer can drive up to and including 9 loads. Buffers cannot be wire-ORed to drive higher loads (common error).





THIS IS THE STANDARD MACRO

IT HANDLES 6 LOADS

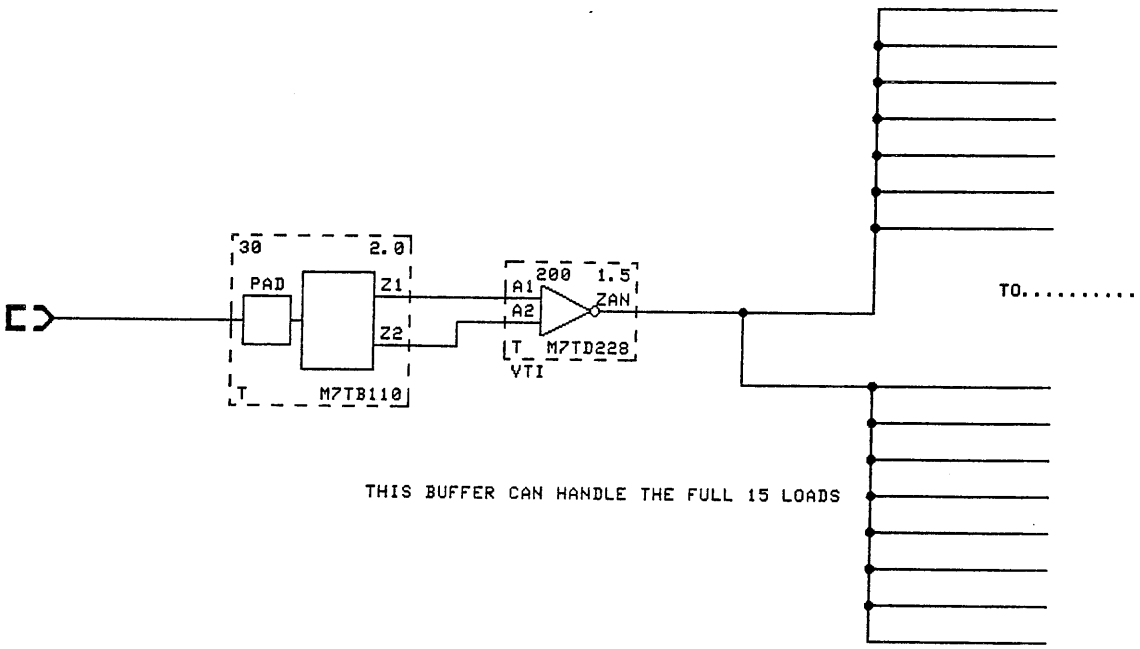


Figure EX.2. High fanout driver buffer.
Buffer can drive up to and including 15 loads.
(Clock signal fanout must be derated.)

- THE FOLLOWING PAGE DETAILS THE IMPLEMENTATION OF A 4:1 MUX FUNCTION FROM THE STANDARD MACROS
    - NOTE THAT THE OUTPUTS ARE WIRE-OR'D
    - THIS ASSUMES THAT BOTH S1N AND S1 ARE AVAILABLE
    - NOTE THAT A "1" ON THE SEL0 LINE SELECTS THE I0 INPUT

S1	S0	F
0	0	D0
0	1	D1
1	0	D2
1	1	D3

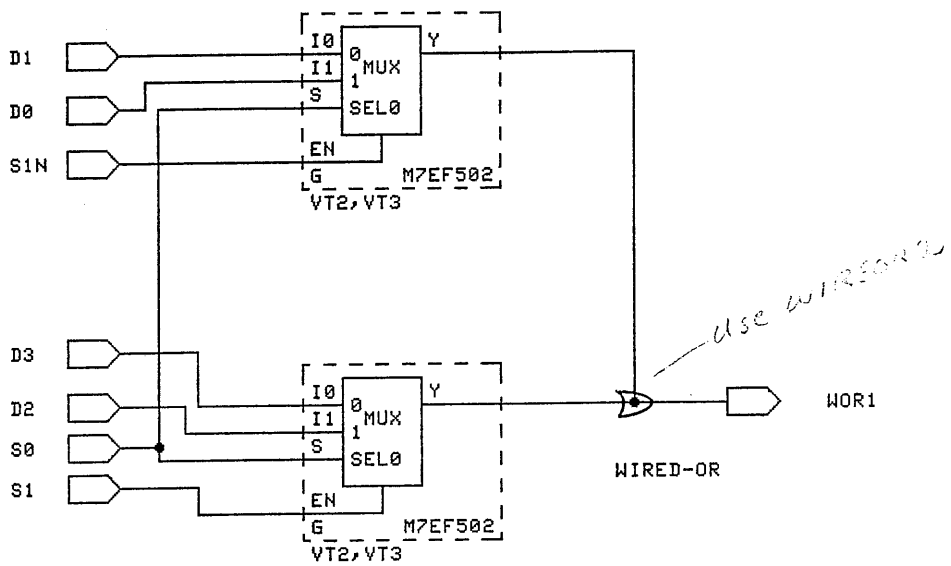
MUXS, DECODERS

One commonly used logic function is the large multiplexer or demultiplexer/decoder. Figure EX.4 diagrams an 8:1 MUX constructed from M7EF398 NOR-gates and the M7EF502 2:1 MUX macros. The output is wire-ORed, with a hand-drawn symbol added for documentation clarity. Figure EX.5 provides a 3:8 decoder constructed from the M7EF600 1:2 decoder macro. Note that the outputs are active low.

As a further example of fan-out restrictions, a 16:1 MUX is shown in figure EX.6, first with all 8 outputs wire-ORed (WRONG, a common error), then with the proper construction, namely, two groups of four wire-ORed outputs fed into an OR gate to produce the desired Y output. The complete drawing is shown in figure EX.7.

WIRE-OR MACROS ARE AVAILABLE IN ALL LIBRARIES

NOTE: SEL0 ON THE SELECT LINE: NOTE HIGH ENABLE



FOUR TO ONE MUX WITH ENABLE

Use WIREOR2 t_{pd-} t_{pd+} now part of component WIREORS

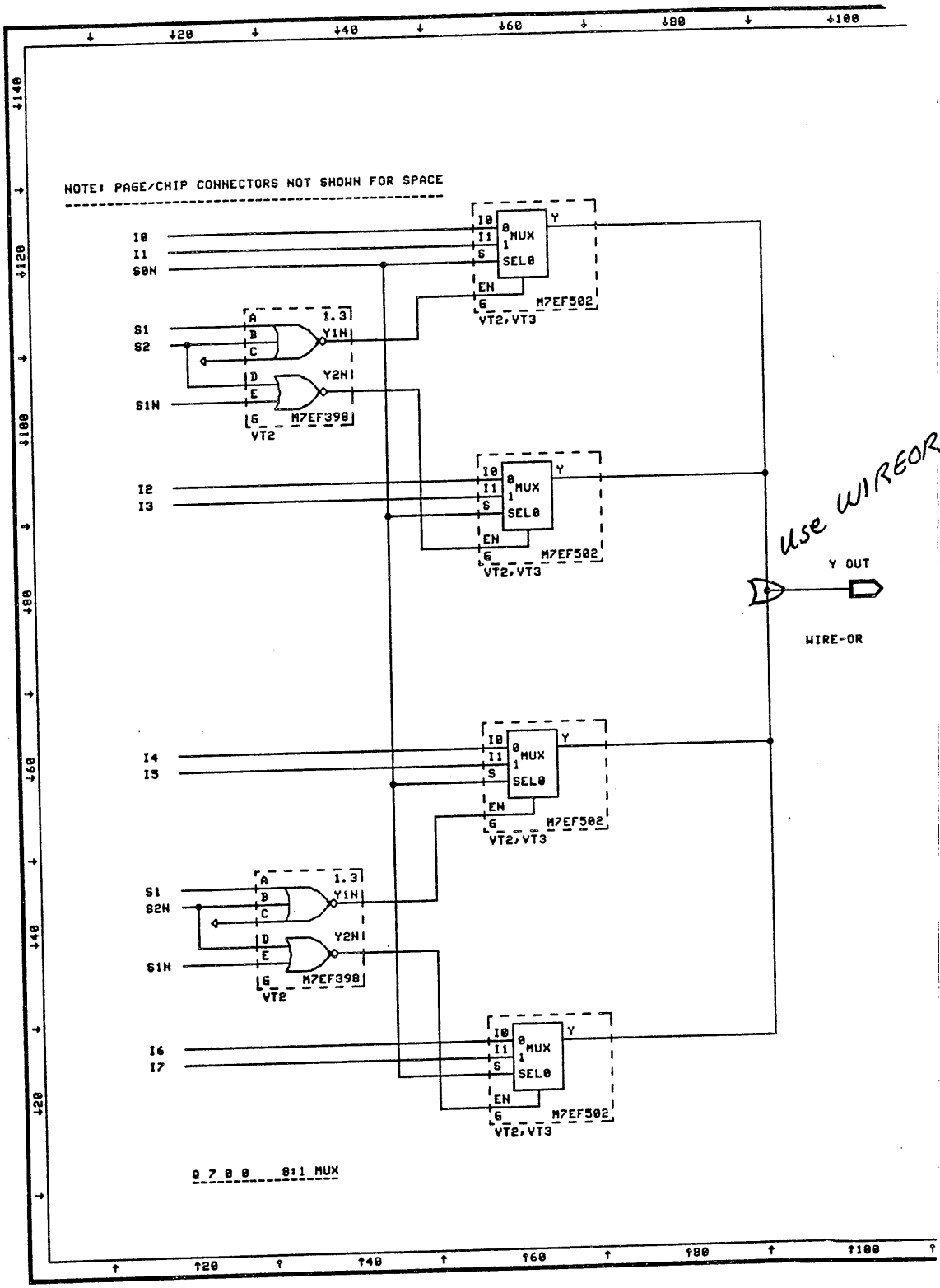


Figure EX.4. Q700 series 8:1 MUX from 4 2:1 MUXs with enables, NOR gates. The input page connectors are not shown - you must include them in a proper Daisy drawing. Y OUT must pass through the proper ECL or TTL output stages to go off-chip. The wire-OR must have a parameter added in a Daisy drawing.

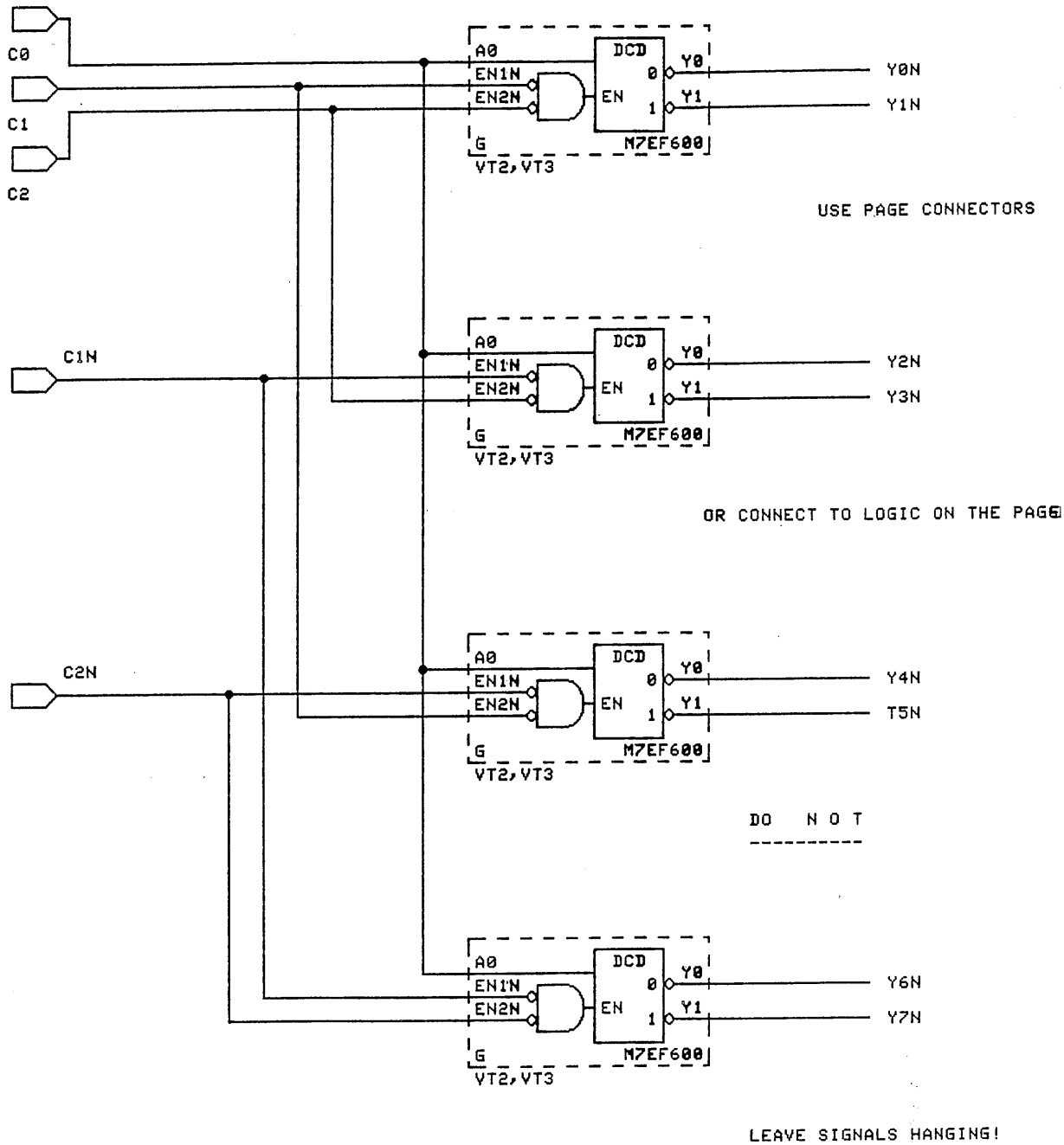
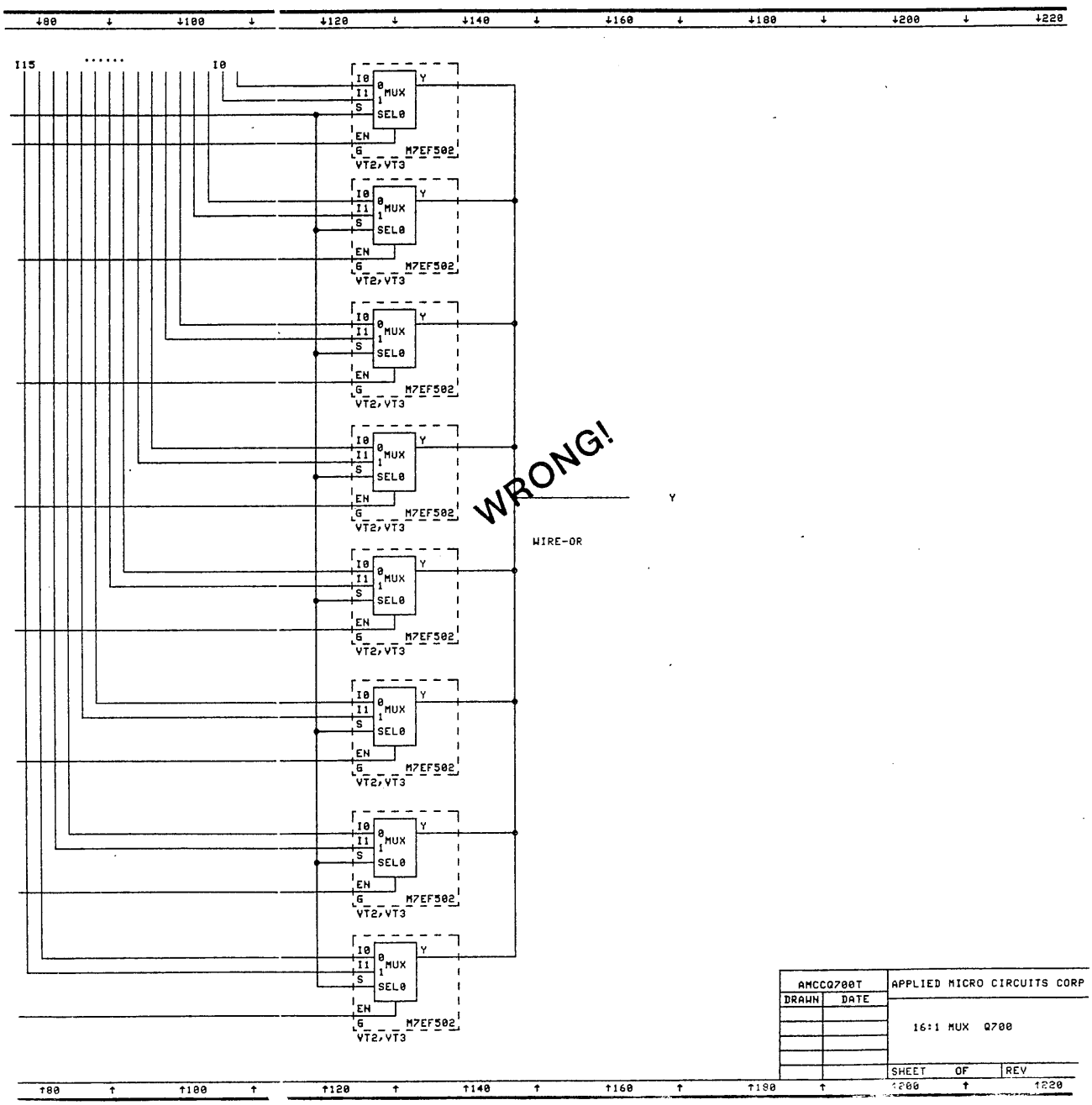


Figure EX.5. A 3:8 decoder for the Q700 series. Input page connectors are shown, but the outputs have been left hanging. All output lines must be terminated in Daisy, either connecting to logic on the page, connected to off-page connectors, or connected to terminators (for unused macro outputs).

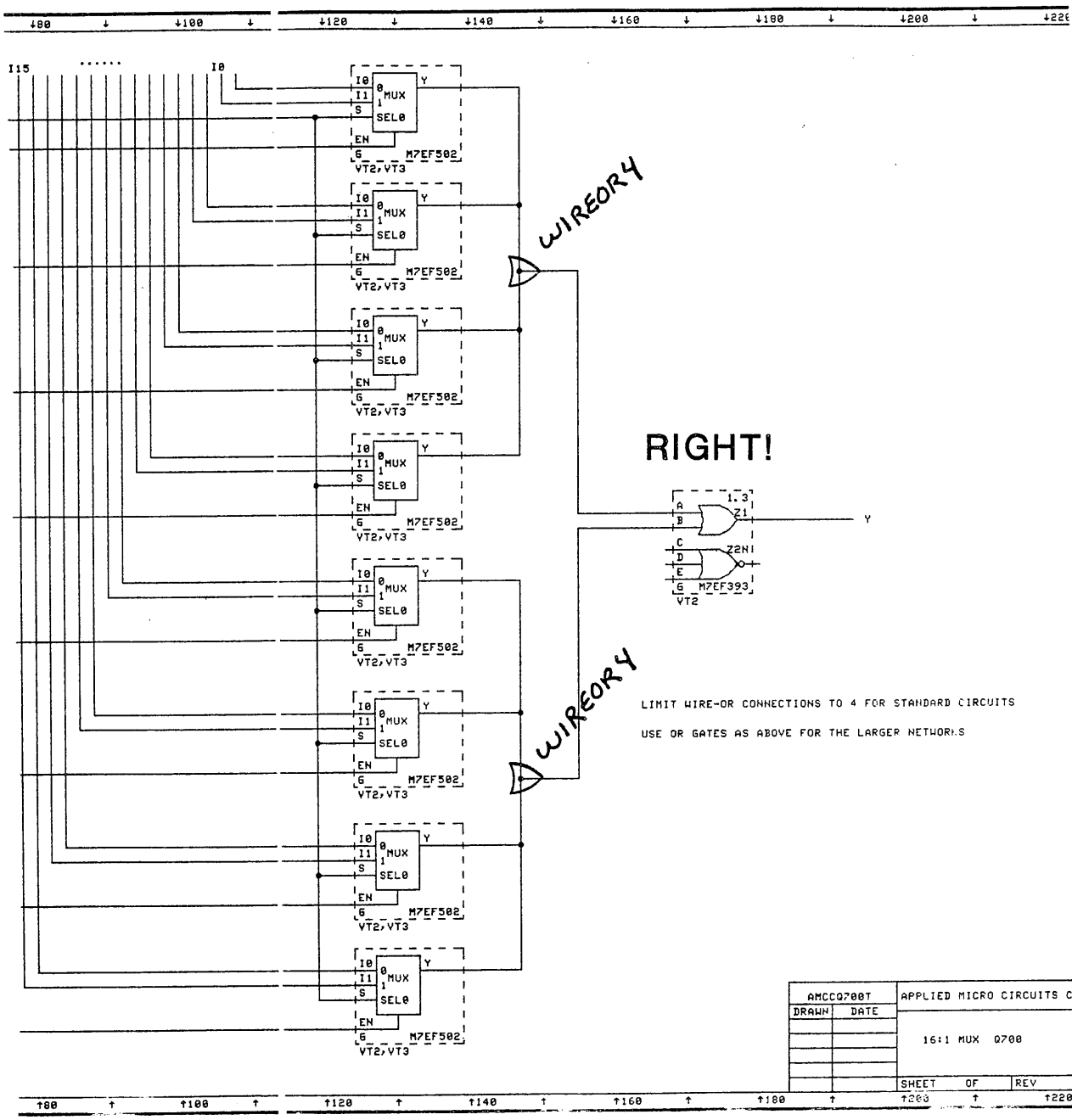
- THE FOLLOWING PAGES ILLUSTRATE A 16:1 MULTIPLEXER
    - THE FIRST PAGE SHOWS THE INCORRECT WAY TO FORM A LARGE WIRE-OR NET
        - NOTE: YOU CAN NOT TIE 8 WIRE-ORS TOGETHER - 4 IS THE LIMIT
          ==========
    - THE NEXT PAGE HIGHLIGHTS THE CORRECT WAY TO HANDLE A NET
        - THE WIRE-OR SYMBOLS WERE DRAWN IN USE WIREORY
    - THE LAST PAGE SHOWS THE COMPLETE 16:1 MUX

- THIS SAME FUNCTION WILL BE REPEATED IN THE SECTION ON THE Q1500 MACROS

Figure EX.6. The wrong way and the right way to connect multiple wire-OR nets together. No more than 4 lines may be wired together - use the OR-gate construct as shown to interconnect larger numbers of wires (8 in this case).



AMCC0700T		APPLIED MICRO CIRCUITS CORP
DRAWN	DATE	16:1 MUX Q700
		SHEET OF REV


I15
I0
MUX
SEL0
M7EF502
VT2,VT3
WIREOR4
RIGHT!
M7EF393
VT2
LIMIT WIRE-OR CONNECTIONS TO 4 FOR STANDARD CIRCUITS
USE OR GATES AS ABOVE FOR THE LARGER NETWORKS
AMCCQ700T
APPLIED MICRO CIRCUITS CORP
DRAWN
DATE
16:1 MUX 0700
SHEET
OF
REV

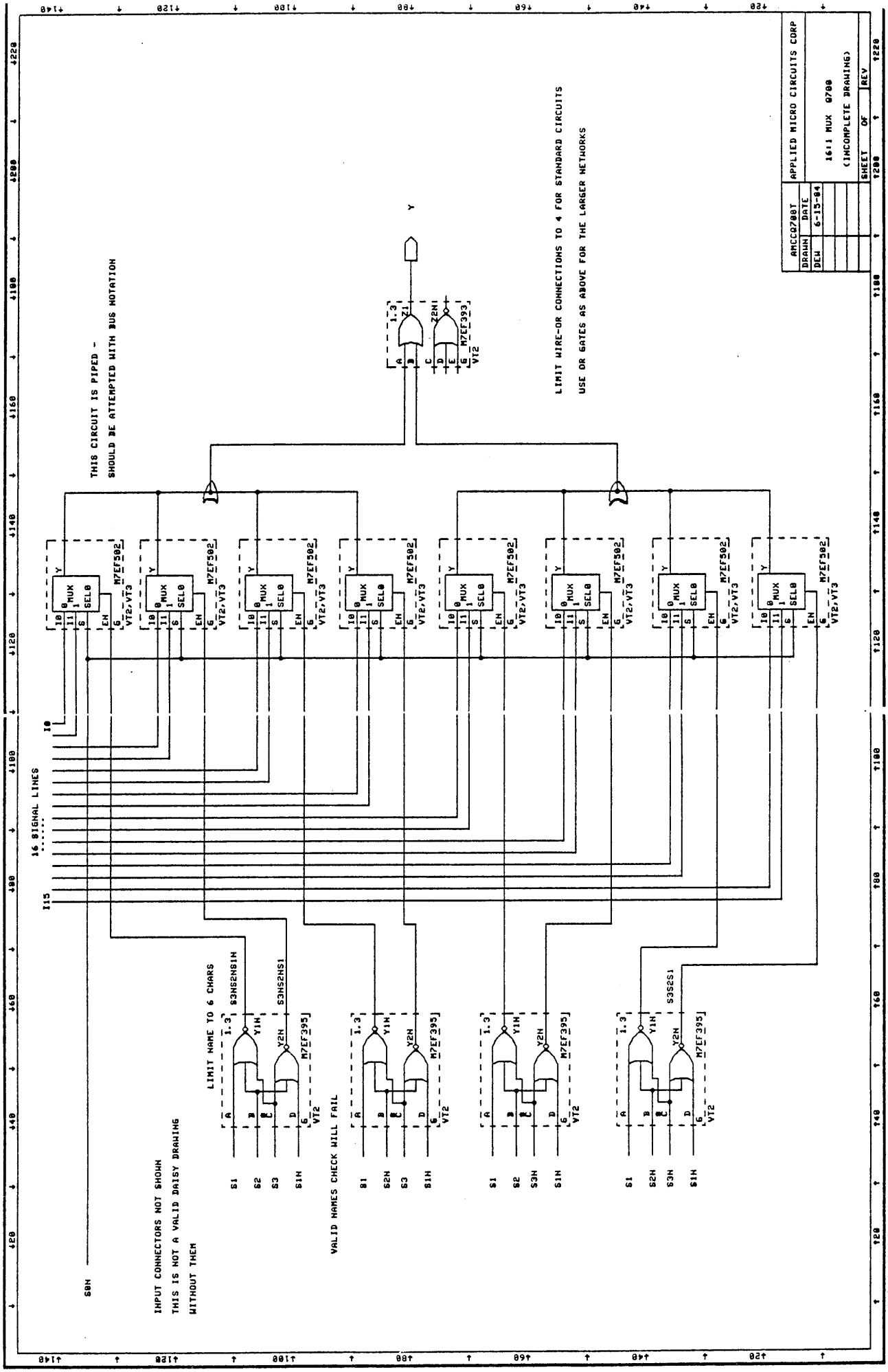


Figure EX.7. Q700 series 16:1 MUX (shown without input connectors).

D F/F FOR THE Q700 SERIES

Figure EX.8A shows a positive edge D F/F constructed from M7EF700 and M7EF701 macros. It is not resettable, and is a simple D F/F for D-type state latches, etc. Figure EX.8B shows the negative-edge version of this type of F/F. Registers and counters are usually constructed with a reset capability and this version of the D F/F is shown in figure EX.8C. This positive-edge triggered F/F with asynchronous reset is constructed from the M7EF730 and M7EF731 macros. The M7EF370 (or the M7EF371) clock buffer macro MUST be used to supply the clock to these macros.

The M7EF370 is essentially a wire-OR buffered gate. The reset line inputs to one input and the clock line to the other for the resulting circuit to properly reset. On reset, the clock line causes the M7EF730 to go into hold, and the M7EF731 goes transparent. The reset line pulls the M7EF730 reset-transistor on which pulls the latch into the reset mode. The M7EF731 has a minimum reset glitch on the output, blocked by the next M7EF731. This construct is the only way to do a reset on the Q700 series.

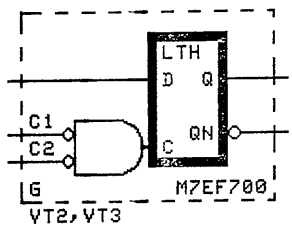
NOTE: The M7EF370 should be used when two buffers are required (they may be for separate registers, counters), else use the M7EF371. All inputs and outputs of the macro must be used.

The clock line from the M7EF370/371 cannot be distributed to more than one register or counter (all F/Fs driven should be in the same functional block). Figure EX.8D diagrams a Presettable D F/F, using the M7EF720 and M7EF731 macros.

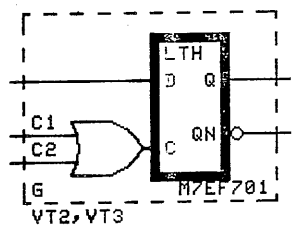
- THE FOLLOWING PAGE SHOWS THE NEGATIVE AND POSITIVE TRANSPARENT LATCHES

- THE NEXT PAGE DETAILS THE CONSTRUCTION OF A POSITIVE EDGE TRIGGERED D F/F AND OF A NEGATIVE EDGE TRIGGERED D F/F FROM THESE MACROS

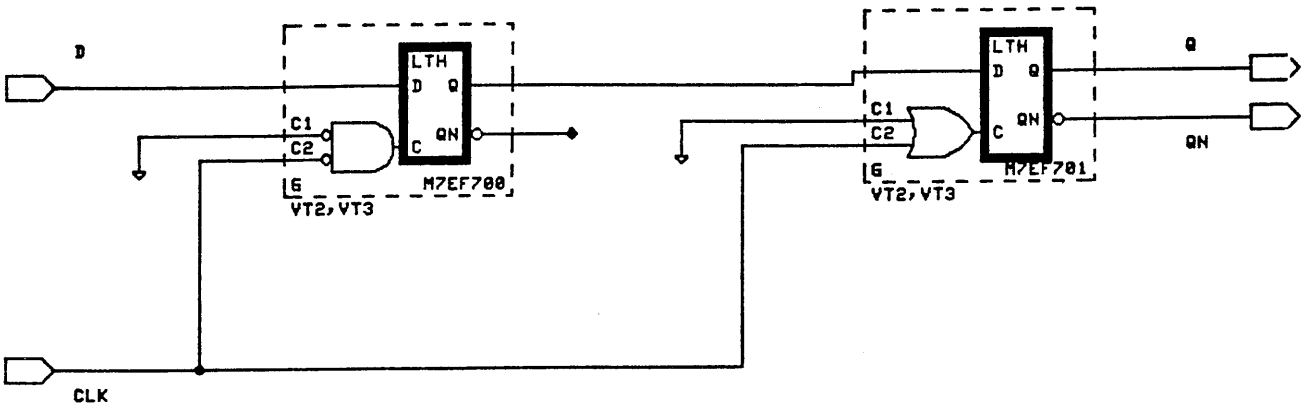
- THE THIRD PAGE DEMONSTRATES A POSITIVE EDGE TRIGGERED D F/F
    - WITH ASYNCHRONOUS RESET
    - WITH PRESET



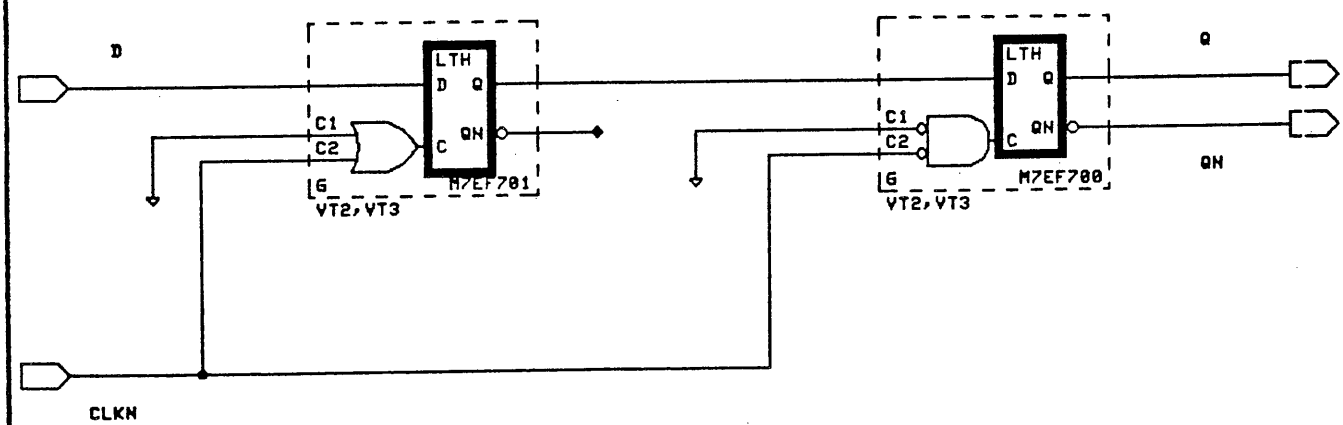
NEGATIVE TRANSPARENT LATCH



POSITIVE TRANSPARENT LATCH

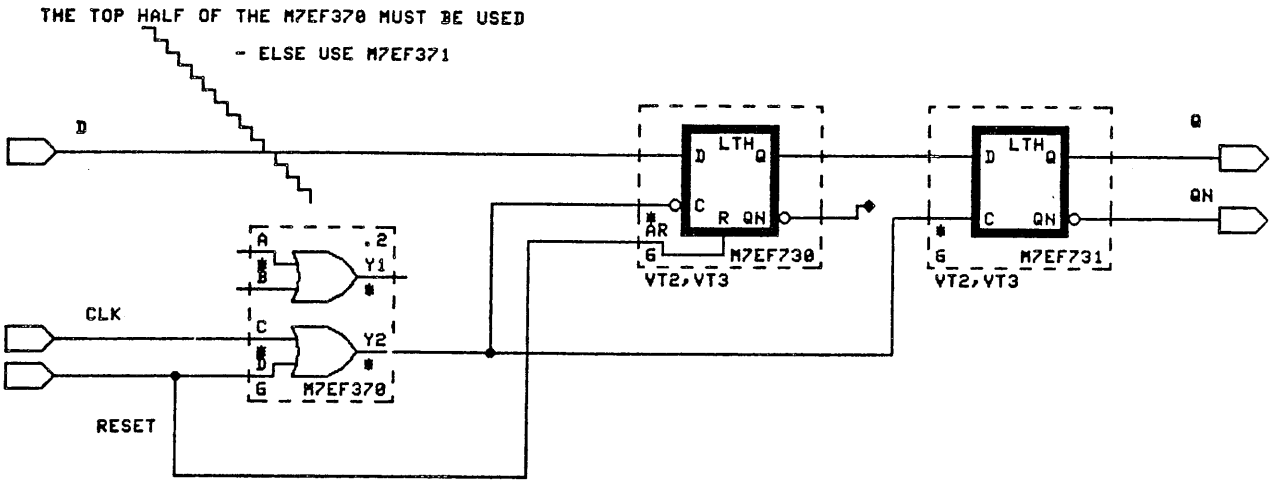


POSITIVE EDGE F/F

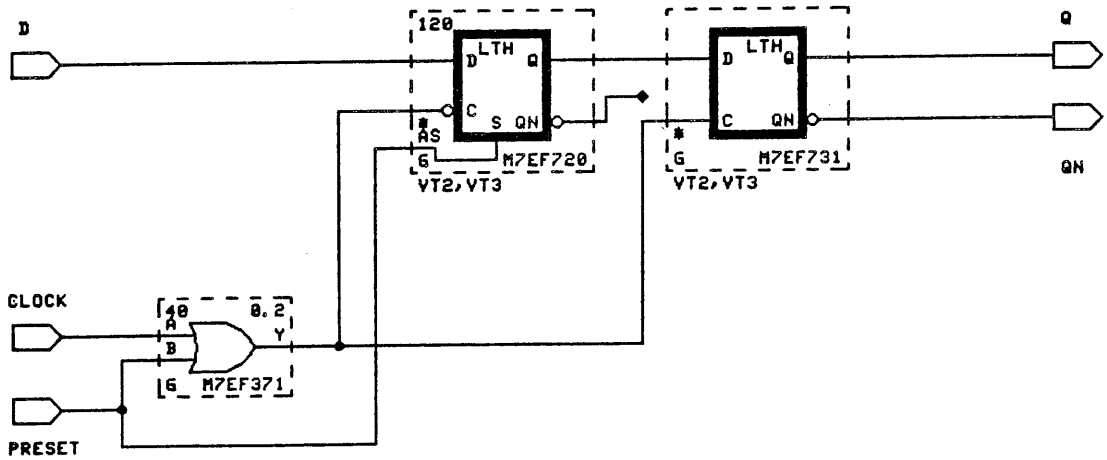


NEGATIVE EDGE F/F

Figure EX.8. D F/F for the Q700 series. (a) shows the positive-edge master-slave F/F, (b) shows the negative edge master-slave F/F.



POSITIVE EDGE TRIGGERED F/F WITH ASYNCHRONOUS RESET



PRESETTABLE D F/F

Figure EX.8 (con't). (c) shows the positive edge triggered D F/F with asynchronous reset. Note that the clock input on these F/Fs must come from a specific macro set, M7EF370 and M7EF371 are shown here. (d) shows a presettable version of the D F/F.

MOBIUS, TWISTED-TAIL RING, OR JOHNSON COUNTER

Figure EX.9A provides a basic Modulo-7 Johnson counter constructed of M7EF730 and M7EF731 latch pairs (D F/Fs). The clock line, since the fan-out is high, is split between two OR gates, both on the M7EF370, with each driving four loads. In this case, the loading on the reset line is only 4 loads, so the reset line has no high-fanout problem.

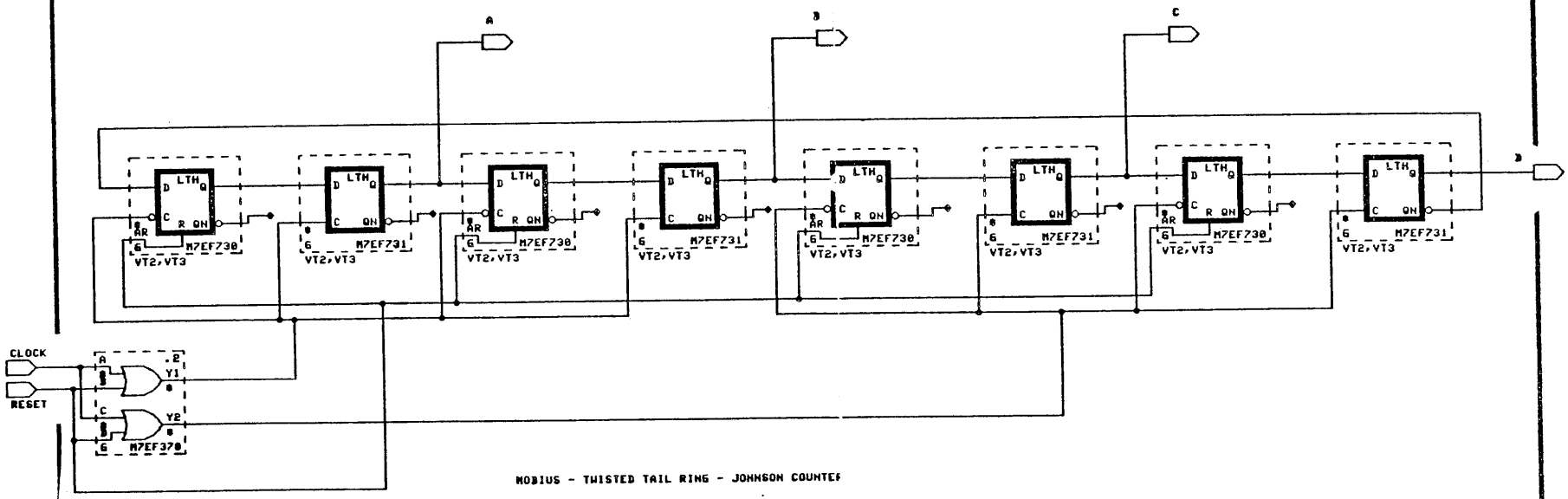
This design uses 9 function cells, or 9/208 = 4.3% of a Q700 logic array.

- THE FOLLOWING PAGE DIAGRAMS A MODULO 7 JOHNSON COUNTER USING THE Q700 M7EF730 MACRO

  (CALLED A MOBIUS OR A TWISTED-TAIL RING COUNTER)

- THIS SAME FUNCTION WILL BE REPEATED IN THE SECTION FOR THE Q1500

- THIS DESIGN USES 9 FUNCTION CELLS FOR 9/208% OF A Q700 (4%)



MOBIUS - TWISTED TAIL RING - JOHNSON COUNTER

SKEW

Another consideration for high-fanout on a clock line is pulse skew. In a shift register, for example, when the clock comes from more than one macro, M7EF370s or other clock buffers, the circuit must compenstate for skew between the clock lines. Skew is introduced by variations in the processing and loading. Macros that are electrically identical (reside on the same power-ground busses) and are therefore physically near will vary within ±10%, while macros located across the chip can vary up to ±20%. Loading differences in similar paths will also cause skew between the signals.

Without compensation for these effects, the later stages in a multiple-stage register could shift twice in one cycle while the clock buffers are changing.

Skew is compensated for by placing a buffer between the different clock sections, on the Q-D line on the connecting F/F (macro-pairs)

Loading adds 0.05ns/load to the rising edge delay path and 0.1ns/load to the falling edge delay path. Loading skew is compensated for by alternating the positive/negative forms of the signal down the path (using inverted outputs).

For critical paths, pulse width variations due to uncompensated loading skew can affect the allowable speed of operation. Pulse stretch and pulse shrinkage due to the differences in the rising and falling edge loading constants must be evaluated in a high-speed circuit.

PRELOADABLE COUNTER

The next pages diagram a 4-bit preloadable counter constructed from M7EF407 and M7EF402 EXNOR macros, M7EF500 2:1 gated select MUX macros, and M7EF700 and M7EF701 latch pairs (positive edge F/Fs). Figure EX.10A diagrams the design. Note the inverted inputs and remember that these examples (this and the previous) are PARTIAL solutions only since no input macros, buffer macros or output macros are shown.

This function uses 16 function cells for 7.7% of a Q700 logic array.

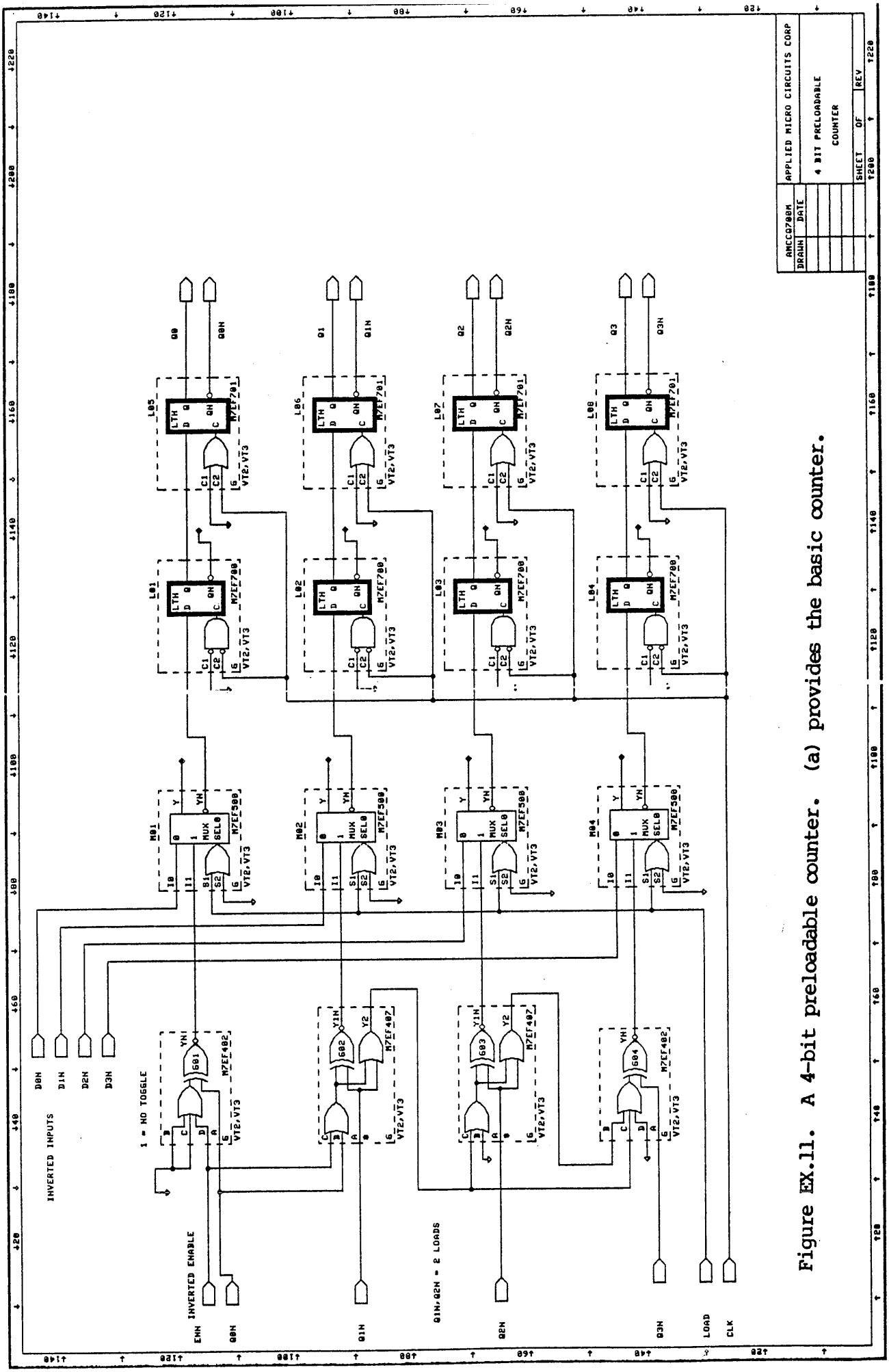


Figure EX.11. A 4-bit preloadable counter. (a) provides the basic counter.

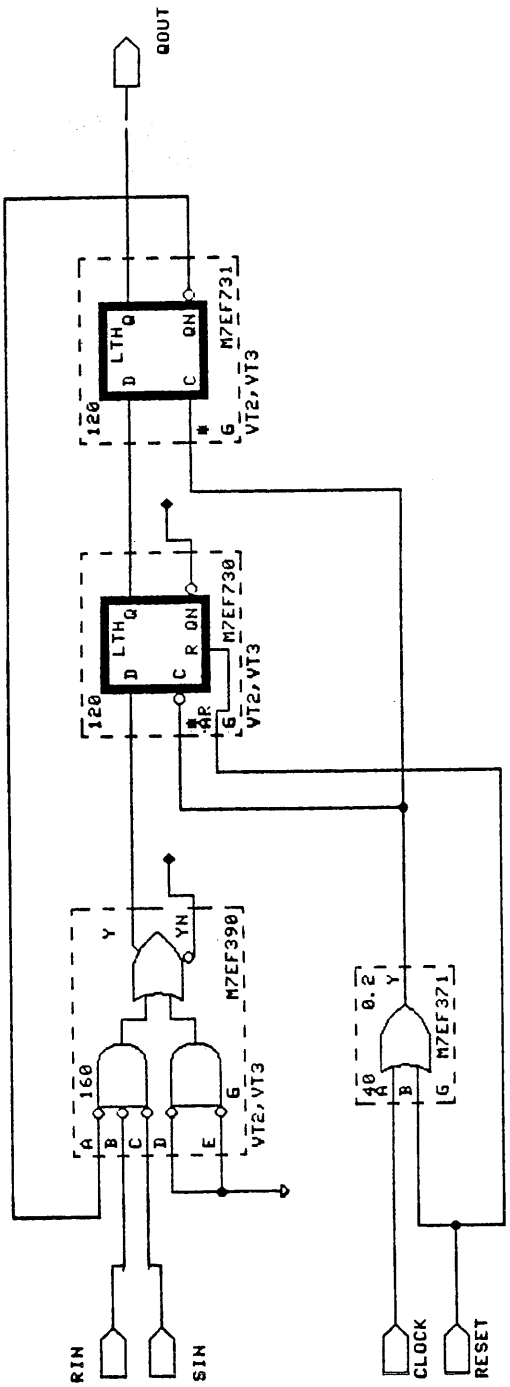
Q700 SERIES R-S F/F

The example shown in Figure EX.11 is an R-S F/F built from D latches and some 2-stage logic (no I/O interconnect macros are shown). The clock is driven by M7EF371, which satisfies the * restriction. Any "*" on a macro diagram means that the designer should refer to the macro summary for the restrictions on loading, interconnections (source/destination), or other information regarding the use of the macro.

Q700 SERIES J-K F/F

The example shown in Figure EX.12 is a J-K Master/Slave F/F, with ECL I/O and all required signal buffers. The F/F itself is composed of macros M7EF503, M7EF730, and M7EF731.

The M7EF503 2:1 MUX macro has a gated select-0 input, meaning that if Select = 1, the I_0 input is the selected input. This is compensated for by using Q to drive the select input as shown.



R-S F/F FROM A D F/F - Q700

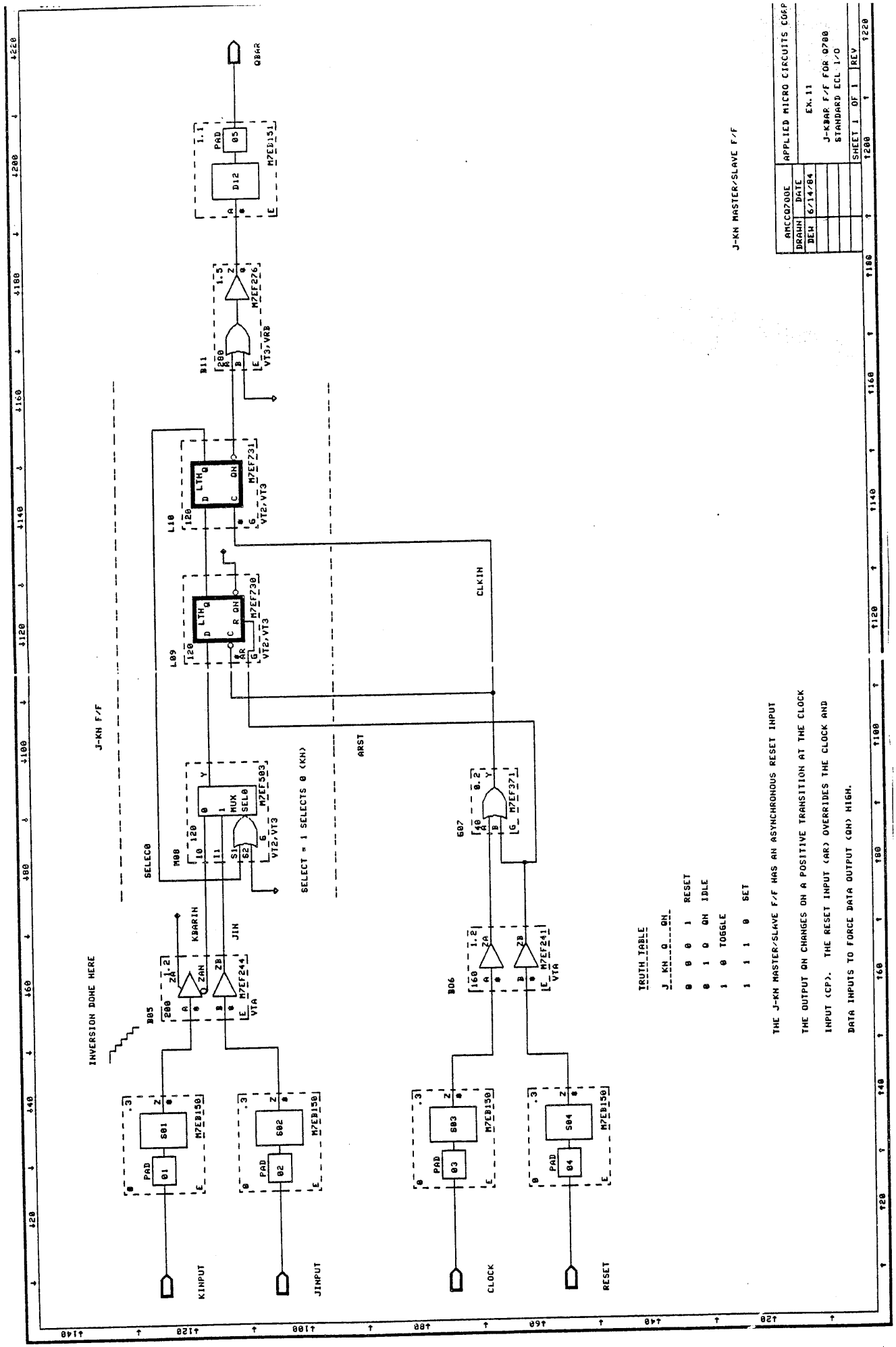
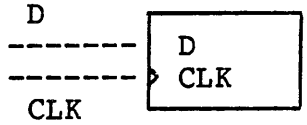


Figure EX.12. Q700 series J-K F/F built from D latches and a 2:1 MUX.

THE F/Fs:

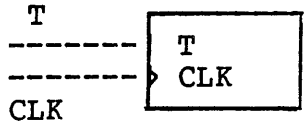
D (DELAY) F/F



$Q^{n+1} = D^n$

D^n	Q^n
0	0
1	1

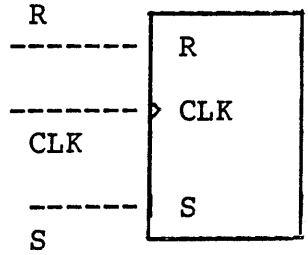
T (TOGGLE) F/F



$Q^{n+1} = (\bar{T}Q + T\bar{Q})^n$

T^n	Q^n
0	Q^n
1	$\bar{Q}^n$

R-S (RESET-SET) F/F

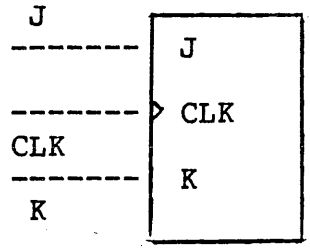


$Q^{n+1} = (S + \bar{R}\bar{S}Q)$

$RS \neq 1$

R^n	S^n	Q^{n+1}	
0	0	Q^n	HOLD
0	1	1	SET
1	0	0	CLEAR
1	1	x	x

J-K F/F

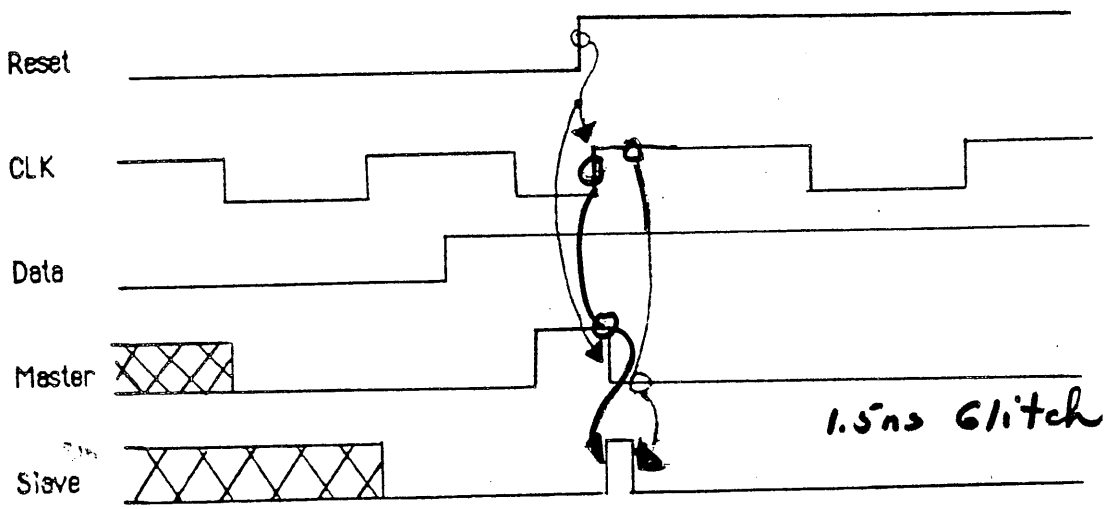


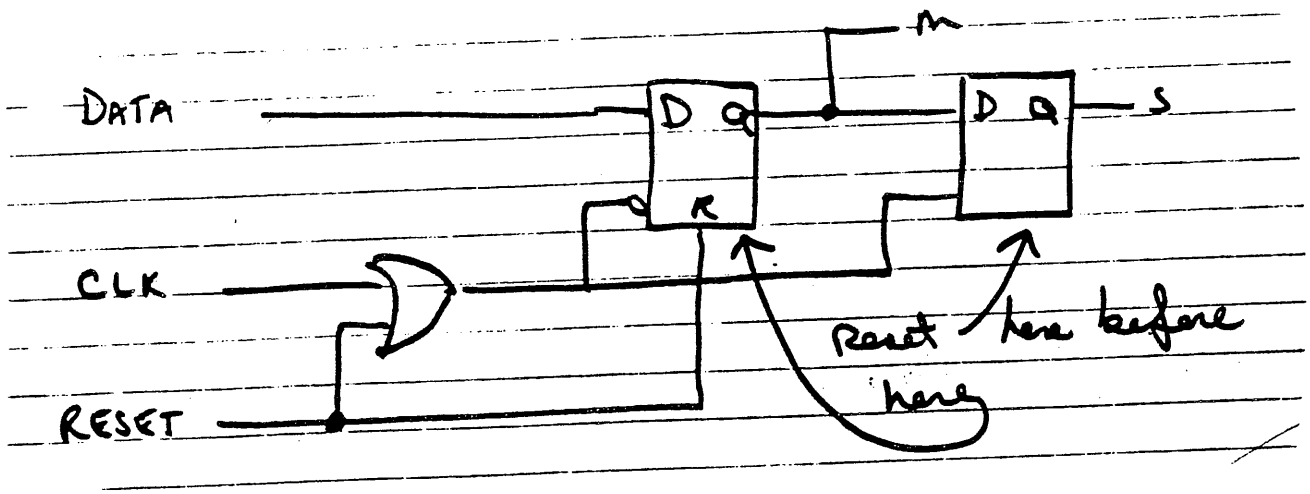
$Q^{n+1} = (J\bar{Q} + \bar{K}Q)^n$

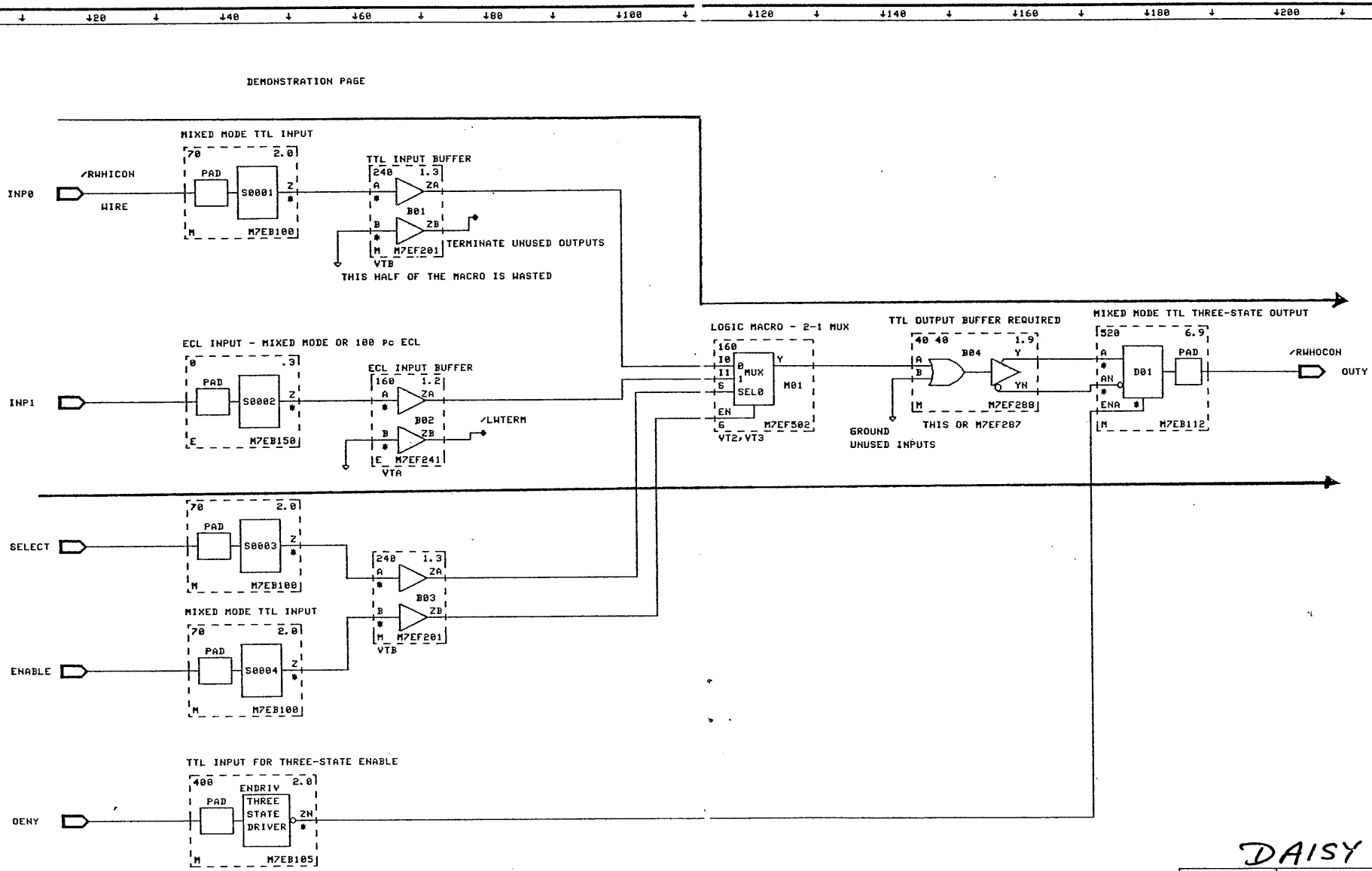
J^n	K^n	Q^{n+1}	
0	0	Q^n	RESET
0	1	Q	IDLE
1	0		TOGGLE
1	1	$\bar{Q}^n$	SET

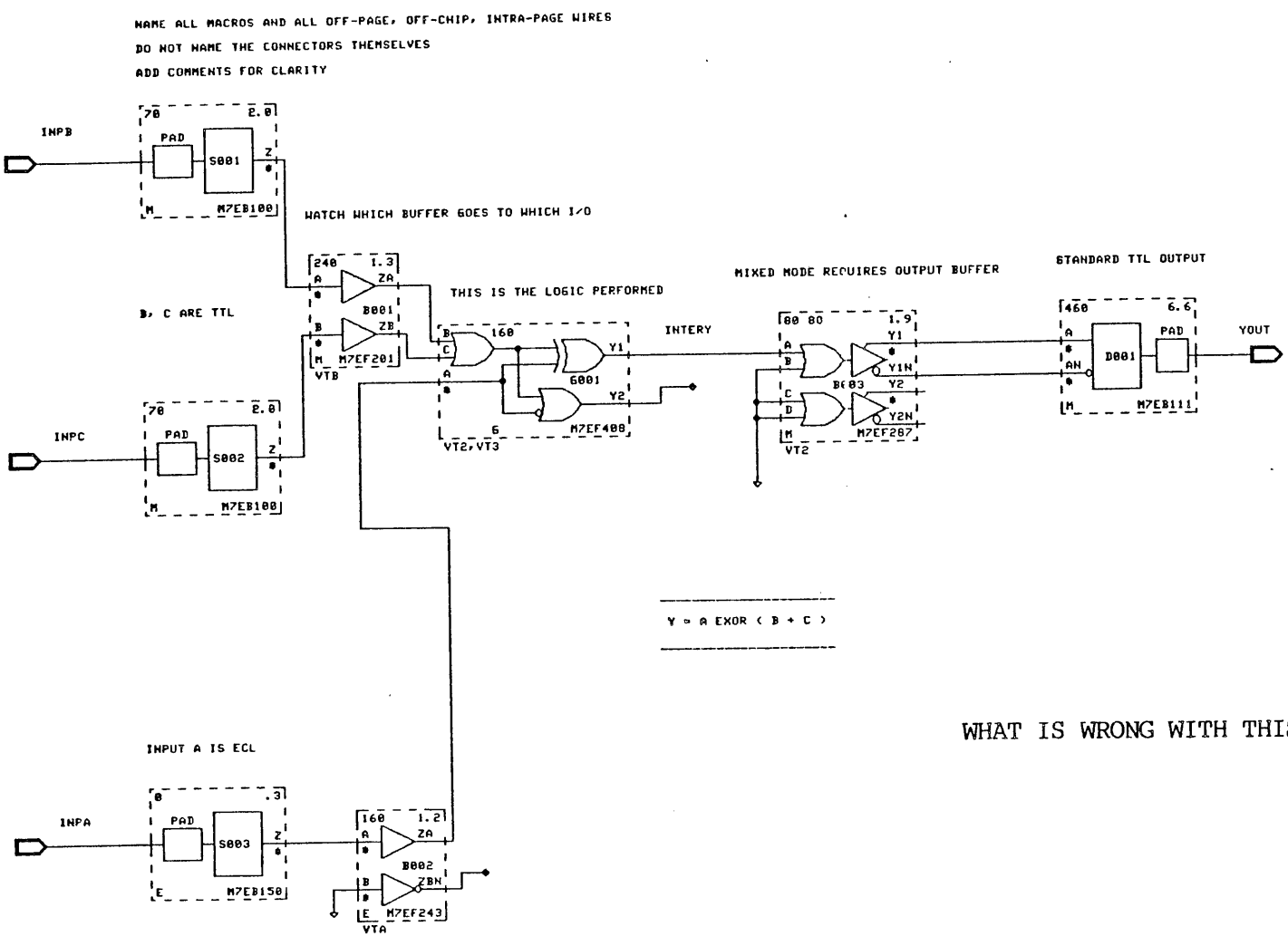
Modelling of Asynchronous Set and Reset on Memory Macros

A glitch exists when the master was in a logic 1 state and the slave was in a logic 0 state and asynchronous reset occurs when the normal clock is low (see diagram below).





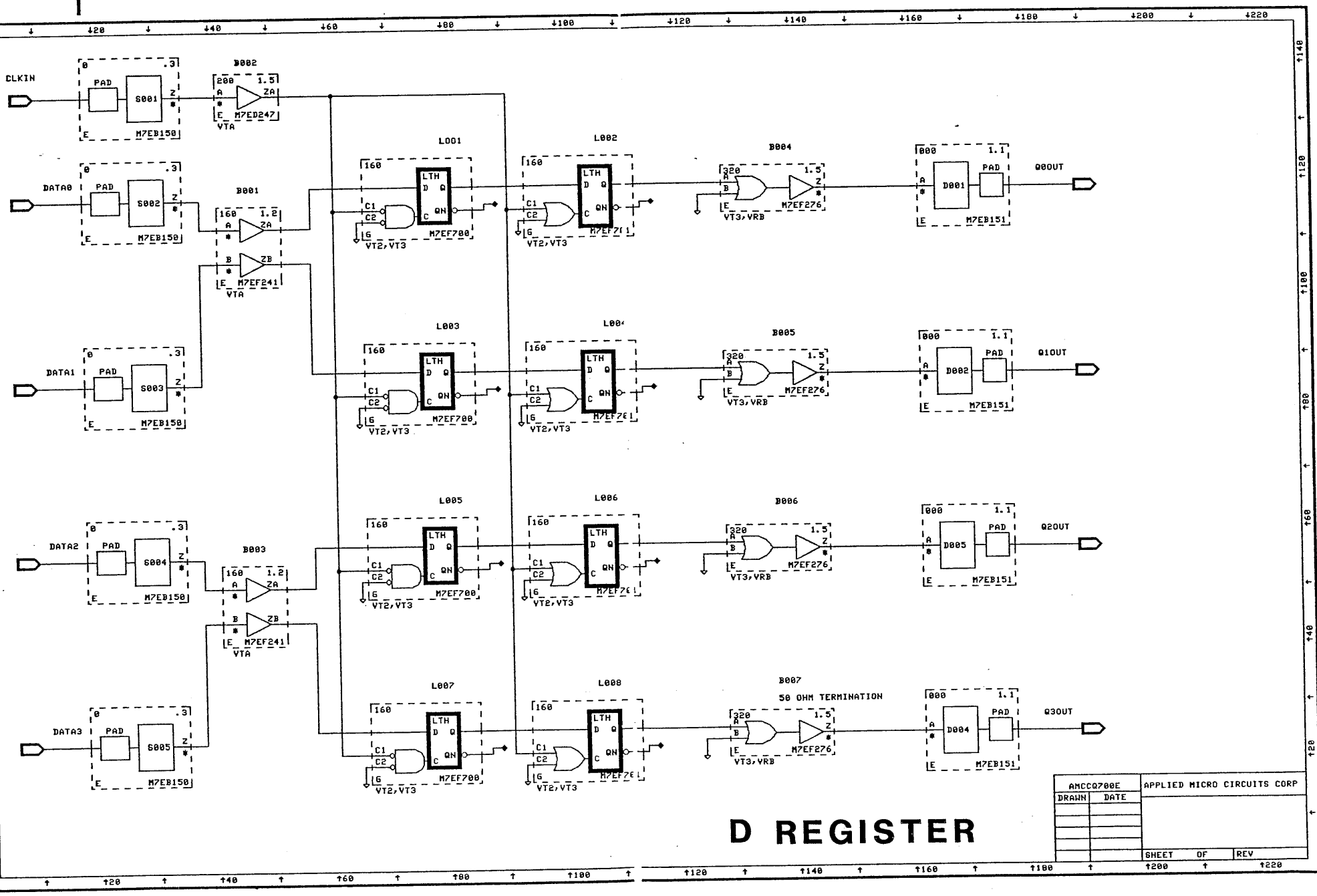

DEMONSTRATION PAGE
MIXED MODE TTL INPUT
INP0
/RWHICON
WIRE
PAD
S0001
M7EB100
TTL INPUT BUFFER
B01
TERMINATE UNUSED OUTPUTS
M7EF201
VTB
THIS HALF OF THE MACRO IS WASTED
ECL INPUT - MIXED MODE OR 100 Pc ECL
INP1
PAD
S0002
M7EB150
ECL INPUT BUFFER
B02
/LWTERM
M7EF241
VTA
LOGIC MACRO - 2-1 MUX
MUX
SEL0
M01
M7EF502
VT2, VT3
TTL OUTPUT BUFFER REQUIRED
B04
GROUND
UNUSED INPUTS
THIS OR M7EF287
MIXED MODE TTL THREE-STATE OUTPUT
D01
PAD
/RWHOCON
OUTY
M7EB112
SELECT
S0003
M7EB100
B03
MIXED MODE TTL INPUT
ENABLE
S0004
TTL INPUT FOR THREE-STATE ENABLE
OENY
ENDRIV
THREE STATE DRIVER
M7EB105
ALWAYS PUT CONNECTORS ON WIRES BEFORE NAMING WIRES
DAISY
AMCC0700M
APPLIED MICRO CIRCUITS CORP
DRAWN
DATE
DEMO
SHEET
OF
REV
9-35



WHAT IS WRONG WITH THIS DRAWING?

DAISY DEMO

AMCC0700M	APPLIED MICRO CIRCUITS COR
DRAWN / DATE	NAME
	SIMPLE CIRCUIT
	SHEET OF REV



D REGISTER

AMCCQ700E	APPLIED MICRO CIRCUITS CORP
DRAWN / DATE	
SHEET OF	REV

9-37

06 DEC 84 14:39 /USER/JEH/CLASSEX 1.DRAW

— OLD ERC FORMAT —

APPLIED MICRO CIRCUITS CORPORATION

Date/Time: 06-DEC-1984 15:10
Directory: /USER/DEW/CLASSEX/ERC
File: MACRO_TAB.DOC

NOTE: In the CURRENT CALCULATIONS TABLE, the subtotals columns will only
the Icc and/or Iee totals will exceed 320.00 mA. Addition is done
and its range is <-32000,+32000> ,where for our purposes cannot e
Therefore, values in either subtotals column must be added manuall

TABLE OF MACRO OCCURENCES			CURRENT CALC			
			SPECS		TOTAL	
INDEX	MACRO NAME	# OF OCCURENCES	ICC	IEE	ICC	IEE
1	M7EB150	5		0.00		00.0
2	M7EB151	4				
3	M7ED247	1		2.00		2.00
4	M7EF241	2		1.60		3.20
5	M7EF276	4		3.20		12.80
6	M7EF700	4		1.60		6.40
7	M7EF701	4		1.60		6.40
CELL TYPE		TOTAL	XXXXXXXX	TOTALS		30.80
I/O		9	Calculations for Icc and Iee subtotals			
FUNCTION		15				

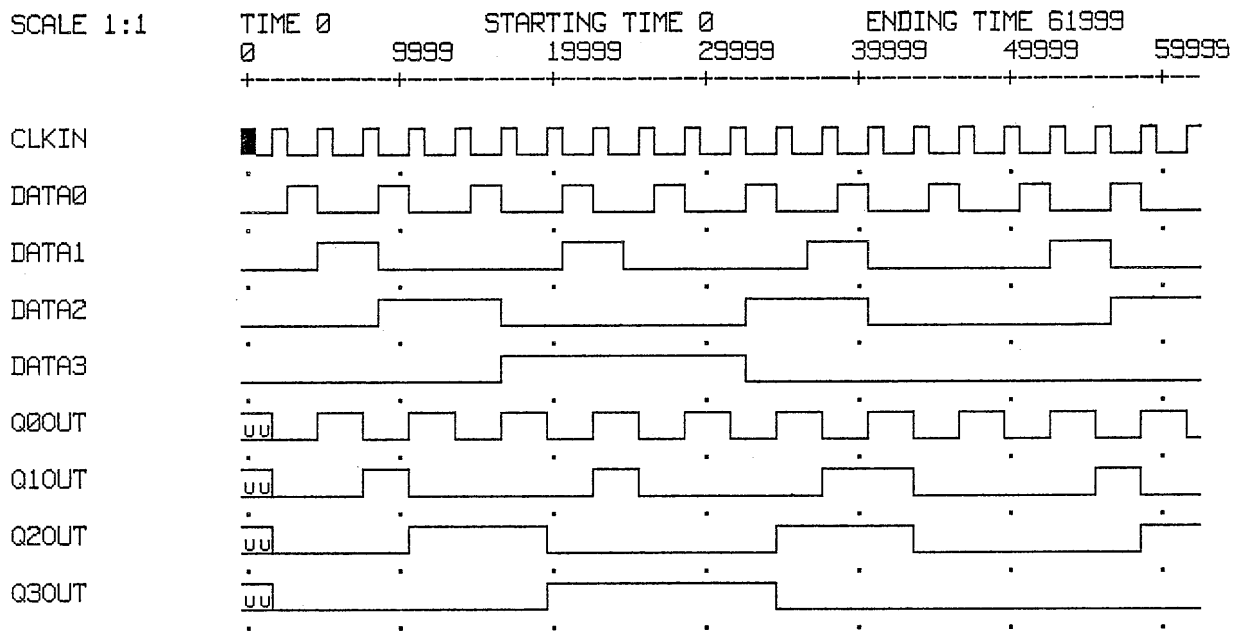
Date/Time: Ø6-DEC-1984 15:Ø8
Directory: /USER/DEW/CLASSEX/ERC
File: FANOUT.ERR

COMPONENT FANOUT TABLE

PAGE	COMPONENT	MACRO NAME	SIGNAL	FANOUT	ERROR
1	BØØ1	M7EF241	PØ_13	1	
1	BØØ1	M7EF241	PØ_21	1	
1	BØØ2	M7ED247	PØ_53	8	
1	BØØ3	M7EF241	PØ_32	1	
1	BØØ3	M7EF241	PØ_49	1	
1	BØØ4	M7EF276	PØ_3	1	
1	BØØ5	M7EF276	PØ_18	1	
1	BØØ6	M7EF276	PØ_29	1	
1	BØØ7	M7EF276	PØ_4Ø	1	
1	LØØ2	M7EF7Ø1	PØ_4	1	
1	LØØ3	M7EF7ØØ	PØ_25	1	
1	LØØ4	M7EF7Ø1	PØ_19	1	
1	LØØ5	M7EF7ØØ	PØ_38	1	
1	LØØ6	M7EF7Ø1	PØ_3Ø	1	
1	LØØ7	M7EF7ØØ	PØ_47	1	
1	LØØ8	M7EF7Ø1	PØ_41	1	
1	LOO1	M7EF7ØØ	PØ_1	1	
1	SØØ1	M7EB15Ø	PØ_51	1	
1	SØØ2	M7EB15Ø	PØ_12	1	
1	SØØ3	M7EB15Ø	PØ_16	1	
1	SØØ4	M7EB15Ø	PØ_27	1	
1	SØØ5	M7EB15Ø	PØ_5Ø	1	
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX				TOTAL	Ø

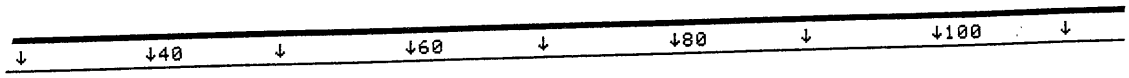
NOTE: An '' will appear in the error column
only if the output signal has too high a fanout.

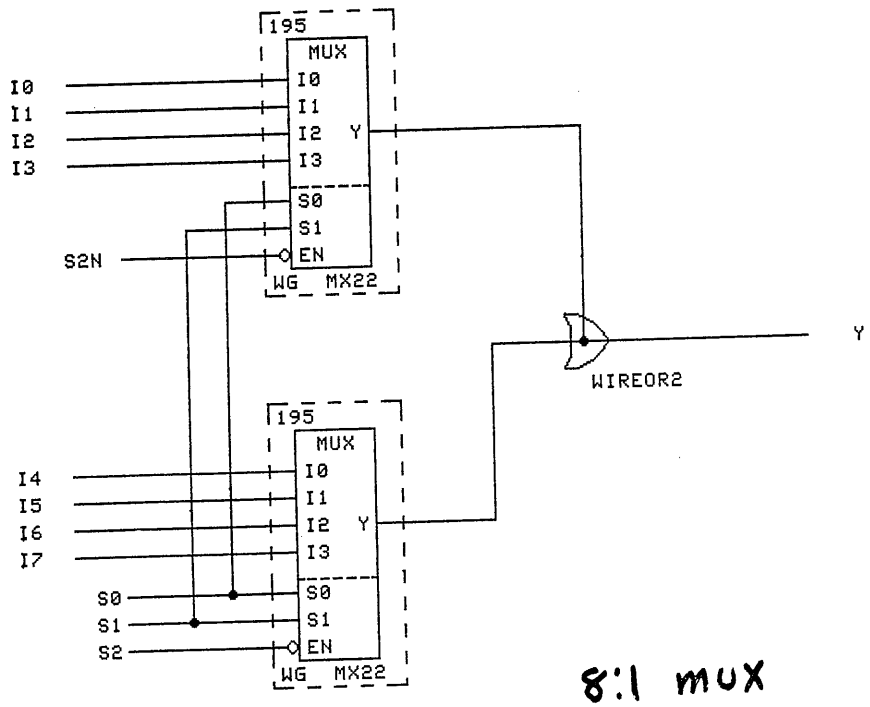
AMCC
APPLIED MICRO CIRCUITS CORPORATION



AMCC
APPLIED MICRO CIRCUITS CORPORATION

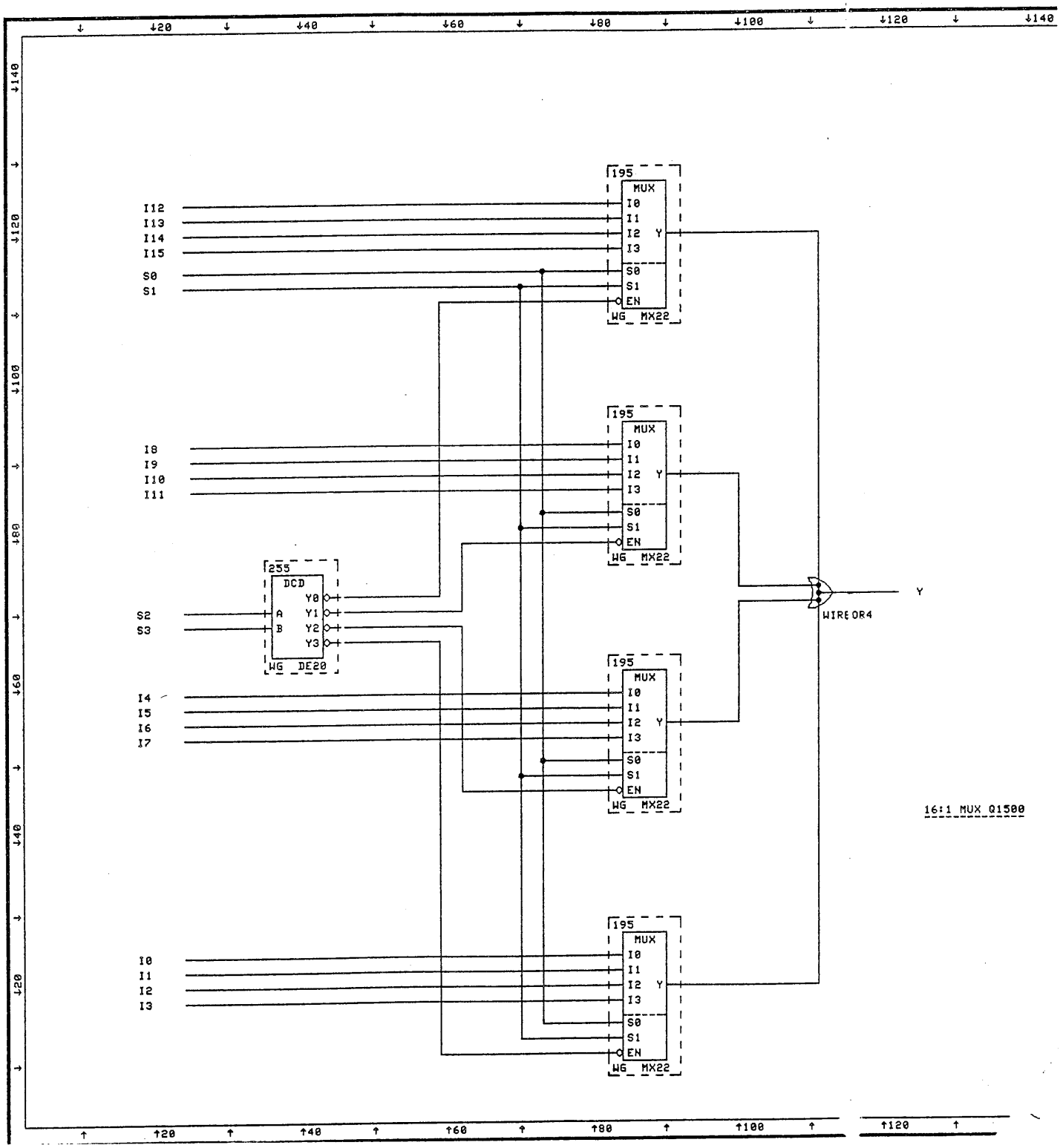
Q1500
DESIGN EXAMPLES

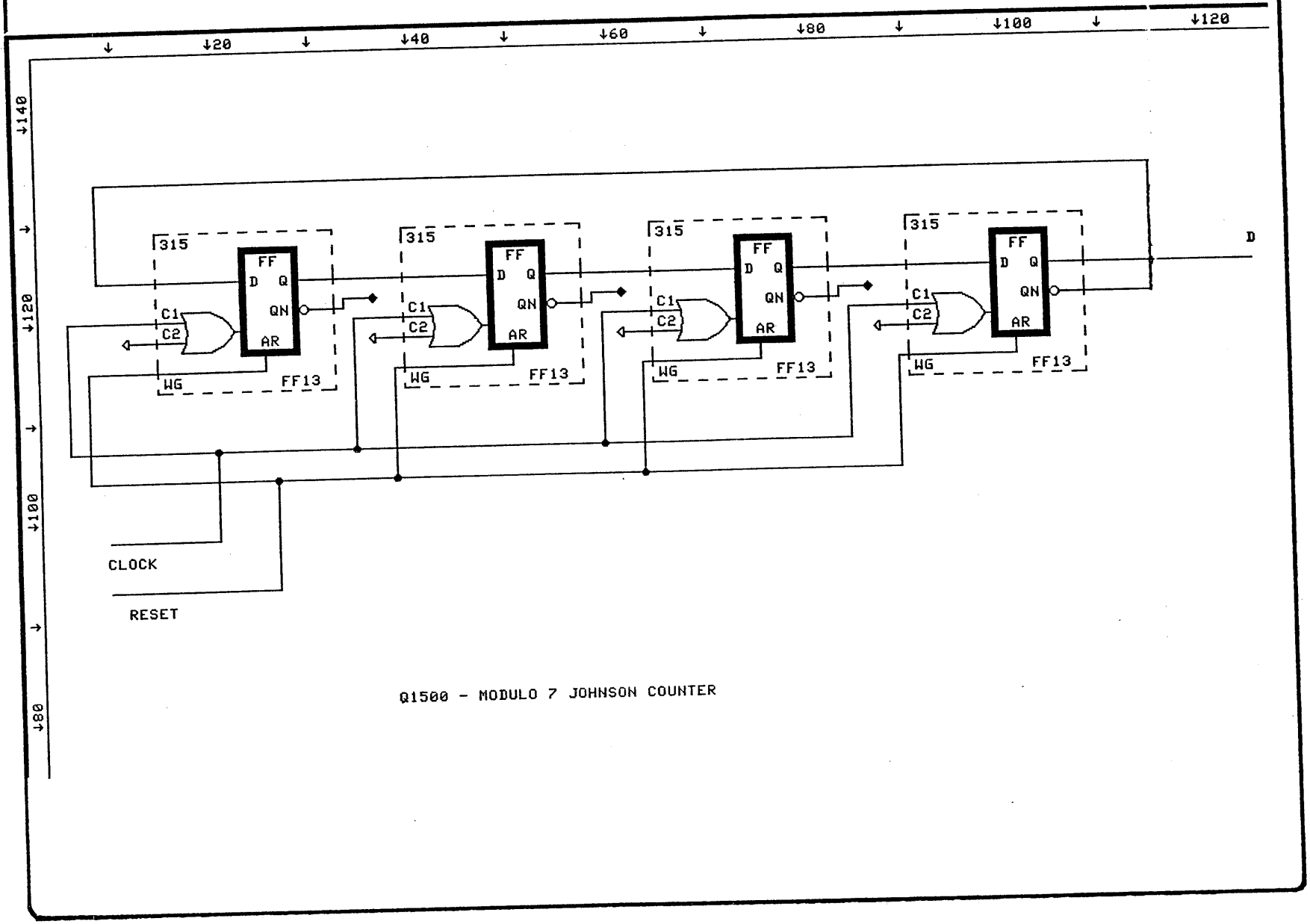




8:1 MUX

GI500/GH1500


195
MUX
I0
I1
I2
I3
S0
S1
EN
Y
WG MX22
I12
I13
I14
I15
S0
S1
I8
I9
I10
I11
I4
I5
I6
I7
I0
I1
I2
I3
255
DCD
A
B
Y0
Y1
Y2
Y3
WG DE20
S2
S3
WIREOR4
Y
16:1 MUX Q1500



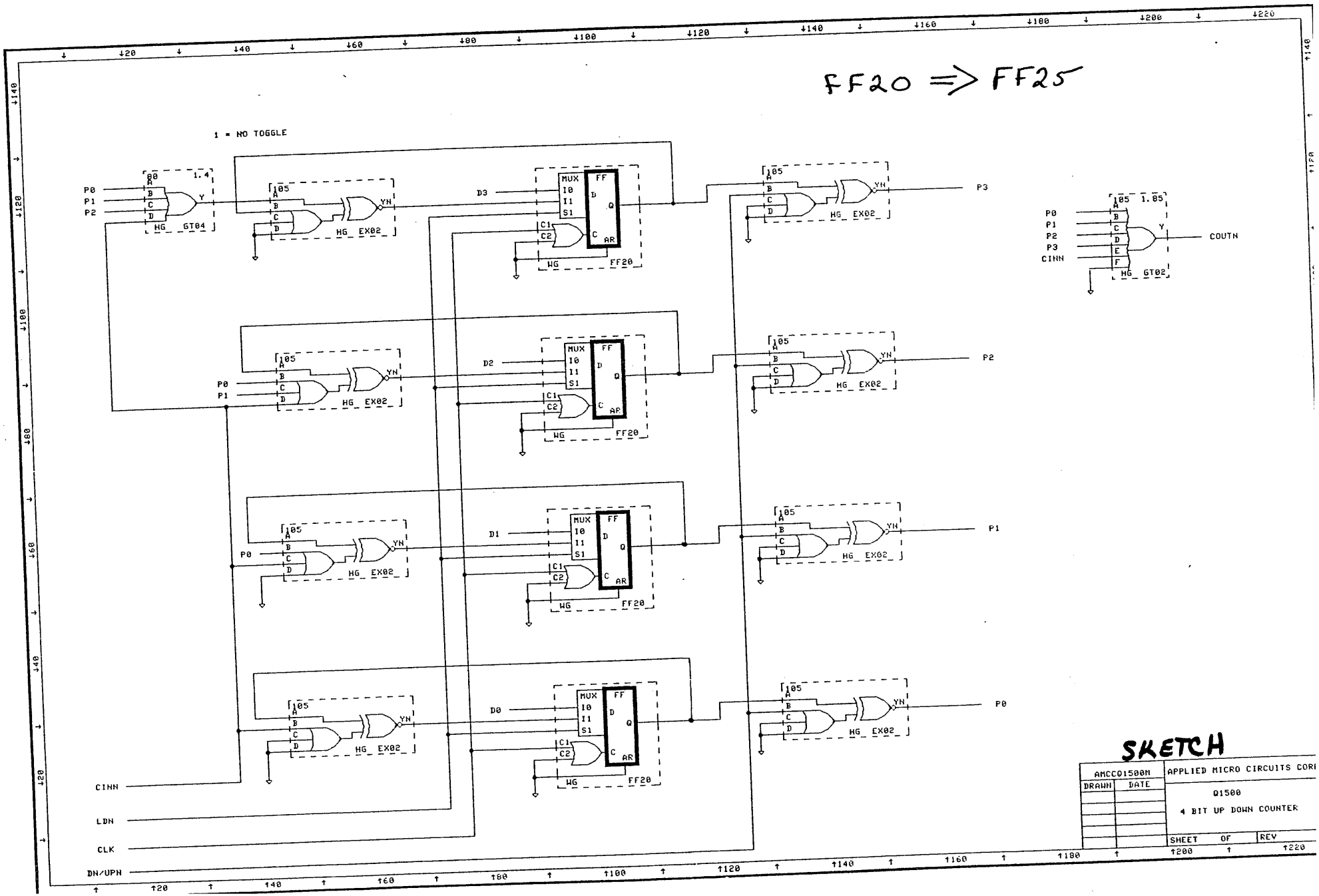
Q1500 - MODULO 7 JOHNSON COUNTER

P R E L I M I N A R Y

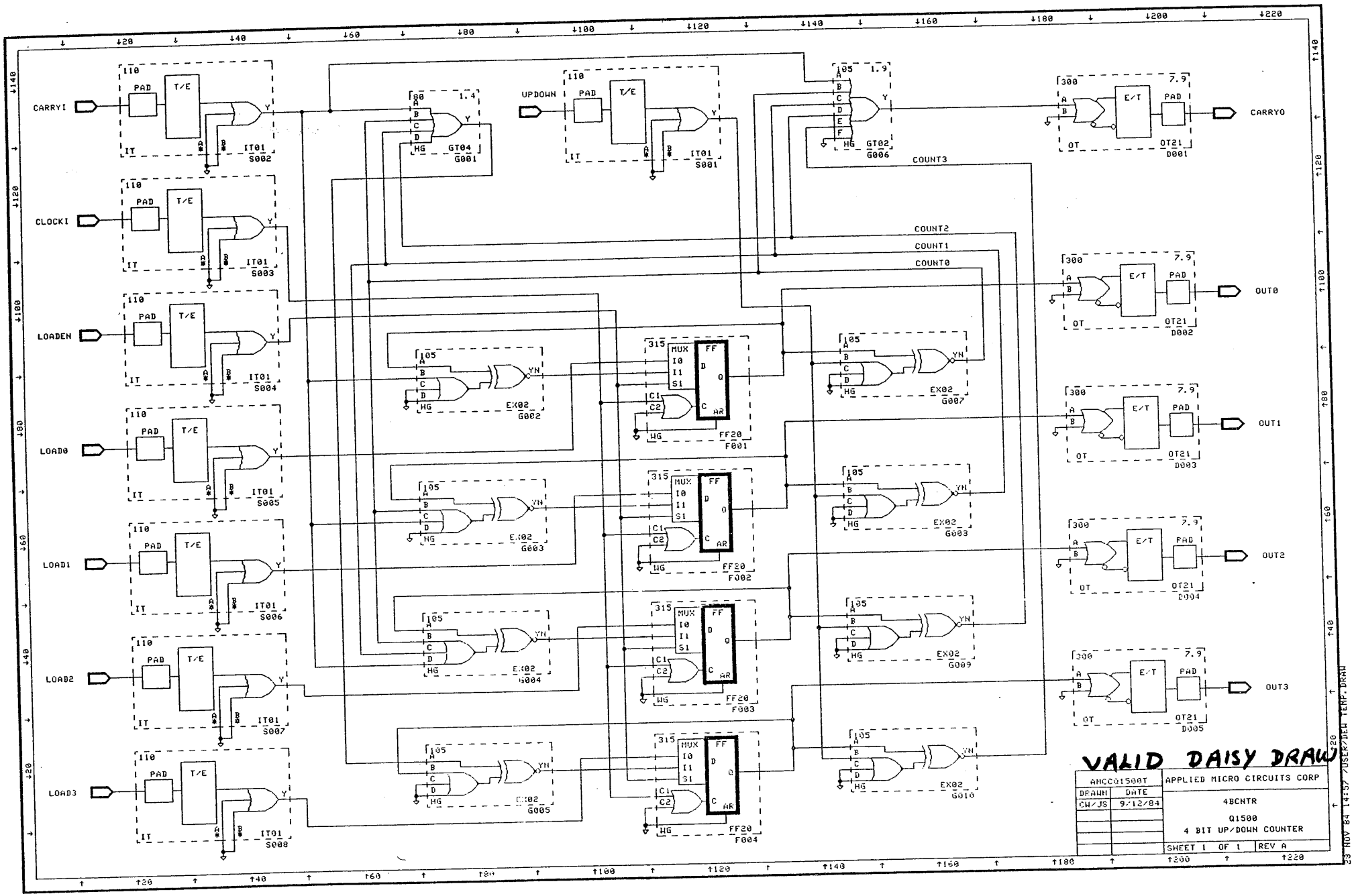
- THE Next EXAMPLE IS A 4-BIT PRELOADABLE UP-DOWN COUNTER DESIGNED WITH THE Q1500 MACROS

- THIS USED 9 CELLS

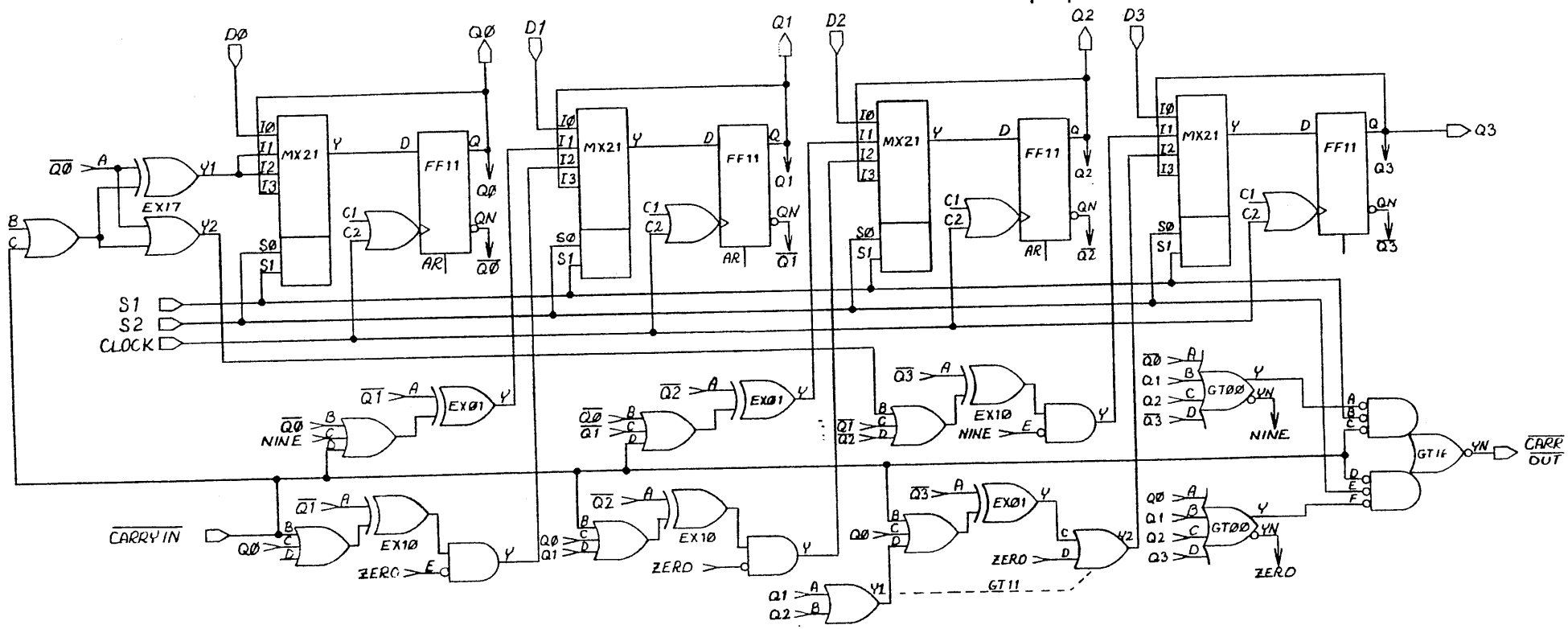
MACRO	SIZE	NUMBER	TOTAL
FF2025	1	4	4
EX02	1/2	8	4
GT04	1/2	1	.5
GT02	1/2	1	.5


FF20 ⇒ FF25
1 = NO TOGGLE
P0
P1
P2
D3
D2
D1
D0
CINN
LDN
CLK
DN/UPN
P3
P2
P1
P0
COUTN
HG_GT04
HG_EX02
HG_GT02
FF20
MUX
FF
SKETCH
AMCC01500N
APPLIED MICRO CIRCUITS CORI
DRAWN
DATE
01500
4 BIT UP DOWN COUNTER
SHEET
OF
REV

9-47


CARRYI
CLOCKI
LOADEN
LOAD0
LOAD1
LOAD2
LOAD3
UPDOWN
CARRYO
OUT0
OUT1
OUT2
OUT3
COUNT3
COUNT2
COUNT1
COUNT0
PAD
T/E
E/T
MUX
FF
EX02
FF20
OT21
VALID DAISY DRAW
ANCCQ1500T
APPLIED MICRO CIRCUITS CORP
DRAWN
DATE
CW/JS
9/12/84
4BCNTR
Q1500
4 BIT UP/DOWN COUNTER
SHEET 1 OF 1
REV A

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



MSI: 10137
NO. CELLS: 13½ L OR B CELLS
POWER: 26.5 MA
PERFORMANCE: f_{COUNT} = 113 MHZ TYP.
NO. PINS: 105

TOLERANCES UNLESS OTHERWISE SPECIFIED		
FRACTIONS	DEC	ANGLES
±	±	±

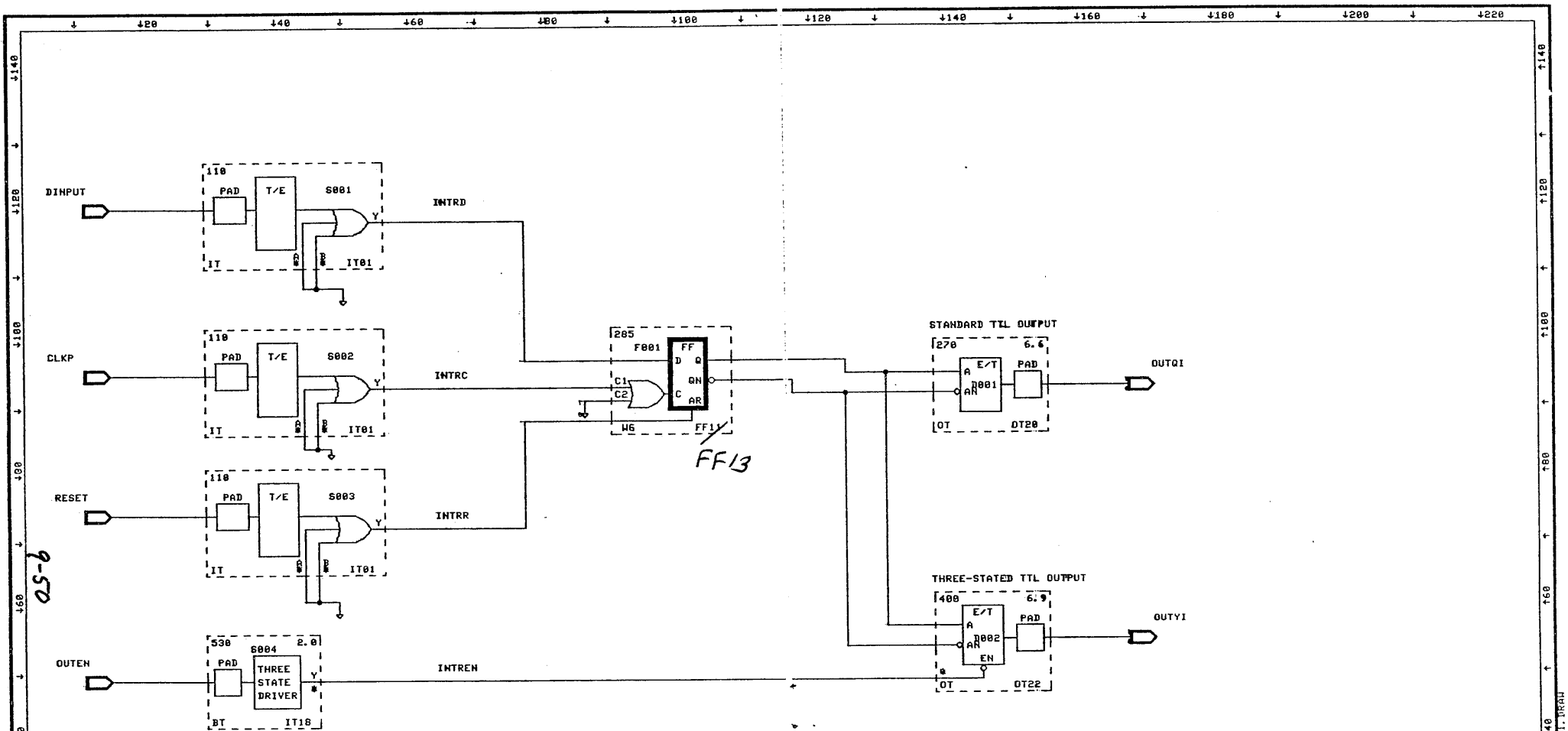
APPROVALS	DATE
DRAWN RW. SPENN	1-5-84
CHECKED	

AMCC San Diego, CA
APPLIED MICRO CIRCUITS CORPORATION

UNIVERSAL DECADE COUNTER
EQUIVALENT TO 10137

SCALE	SIZE	DRAWING NO.
	B	Q1500-83-MSI

DO NOT SCALE DRAWING — SHEET 1 OF 1

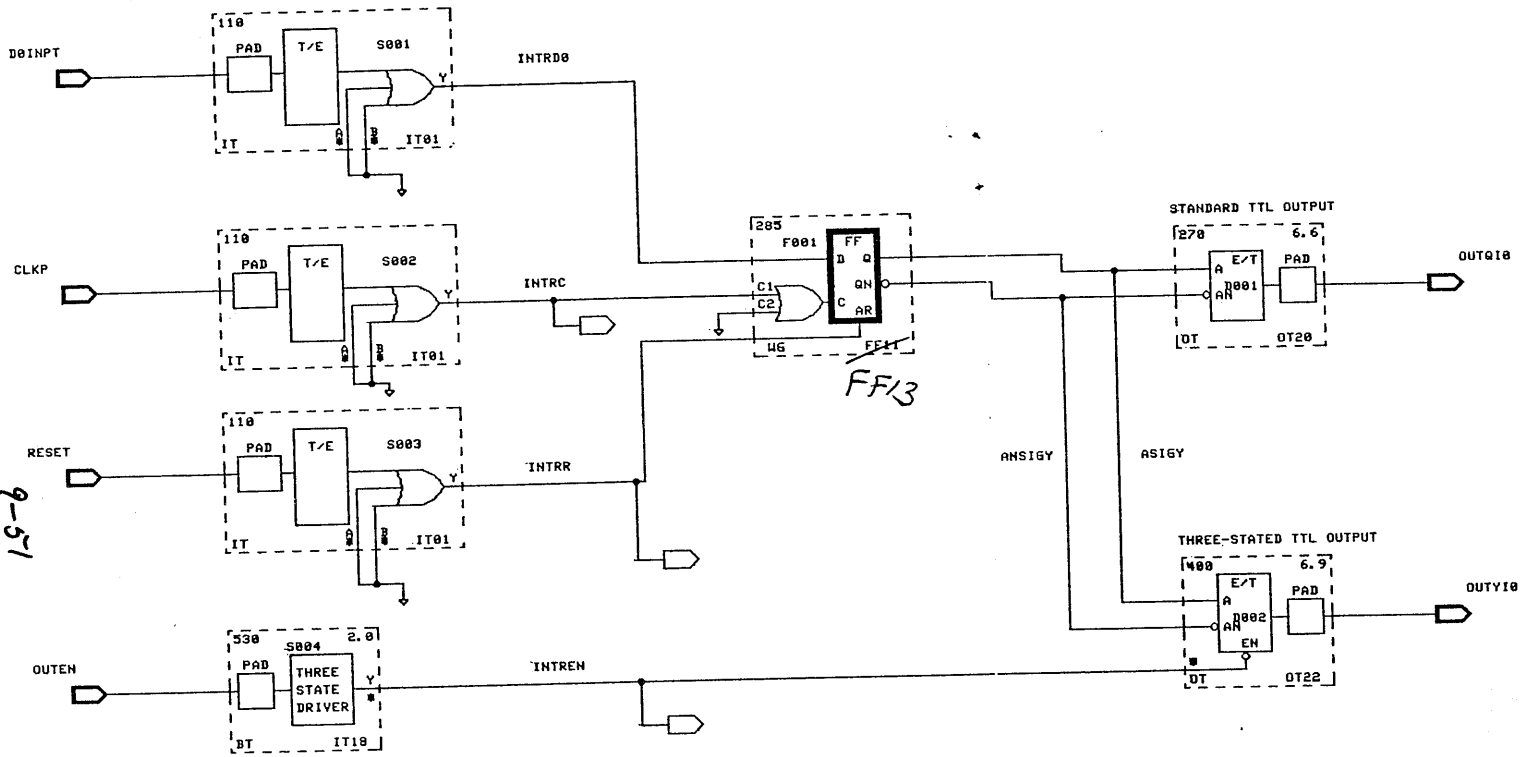


9-50

1 D Cell Register - Dual Output

AMCC01500T		APPLIED MICRO CIRCUITS CORP
DRAWN	DATE	REG1S Am2918 CELL D REGISTER WITH STANDARD AND THREE-STATE OUTPUT
		SHEET OF REV

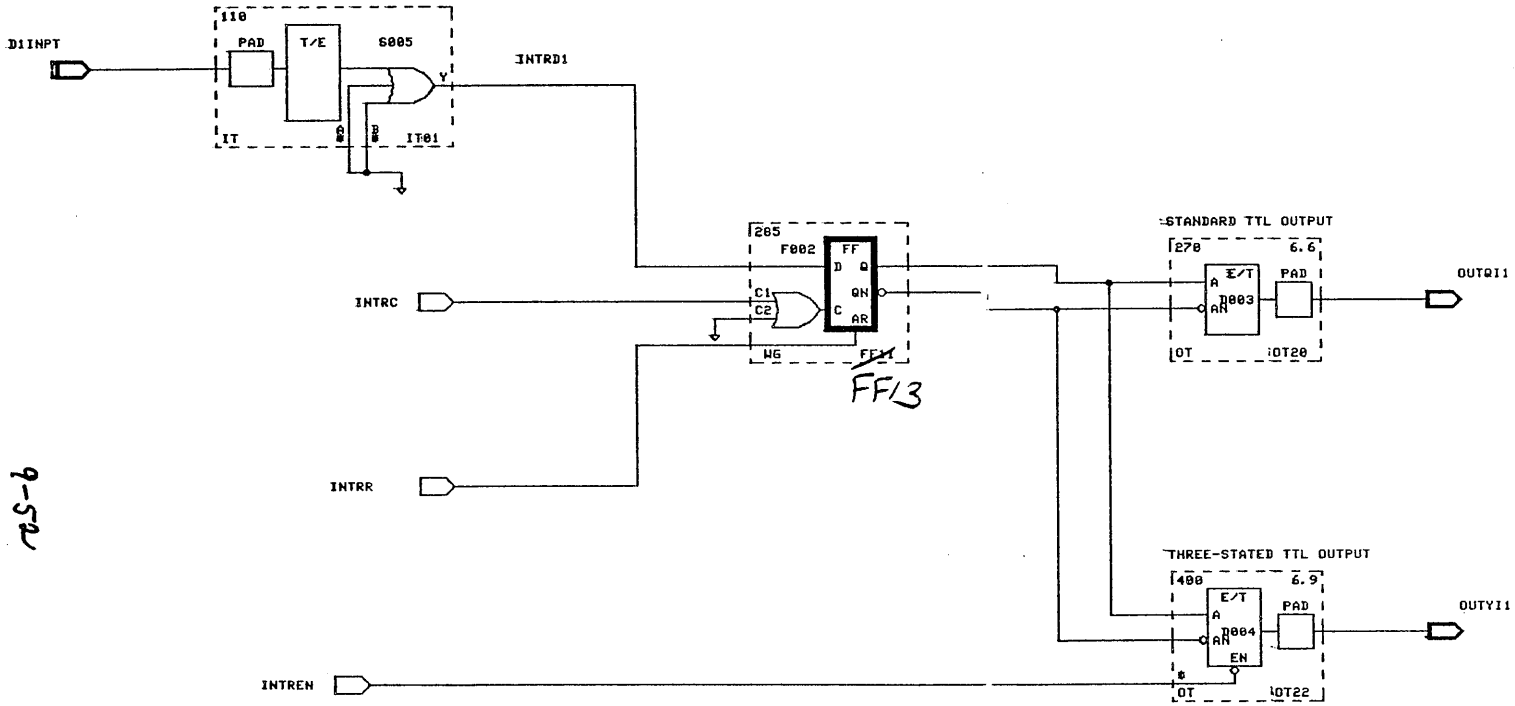
25 OCT 84 12:20 /USER/DEW/DTEMP/015EXAM 1.DRAW



9-51

4- Bit D Reg - Dual Outputs

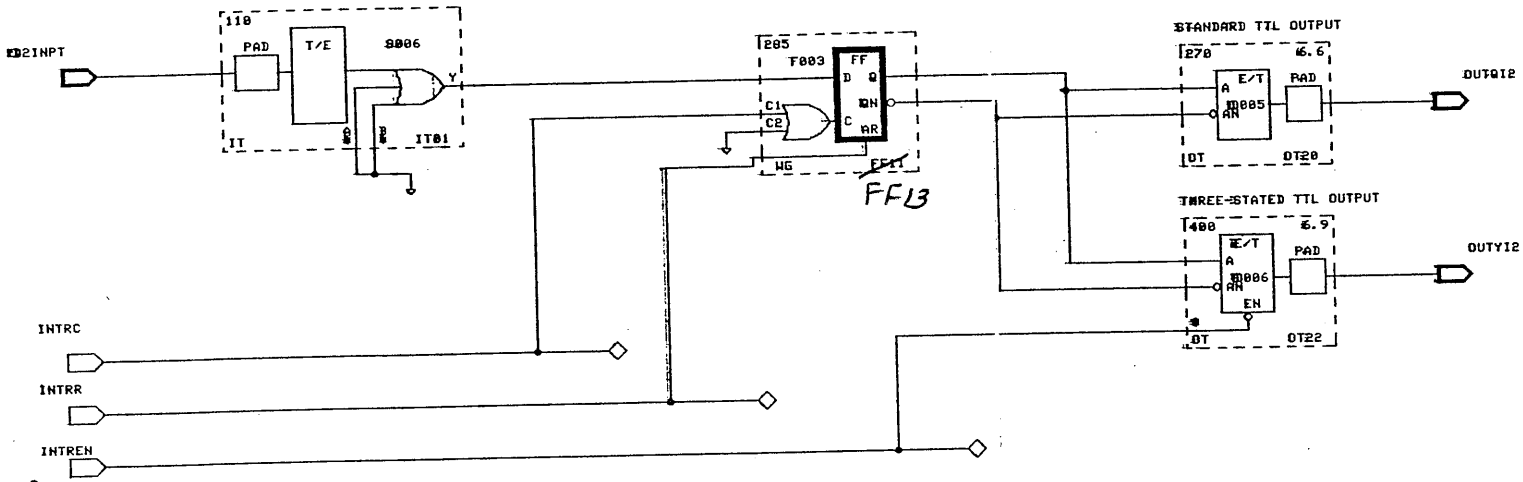
AMCCQ1500T		APPLIED MICRO CIRCUITS CORP
DRAWN	DATE	REGIS Am2918 CELL D REGISTER WITH STANDARD AND THREE-STATE OUTPUT
		SHEET 9 OF 57 REV



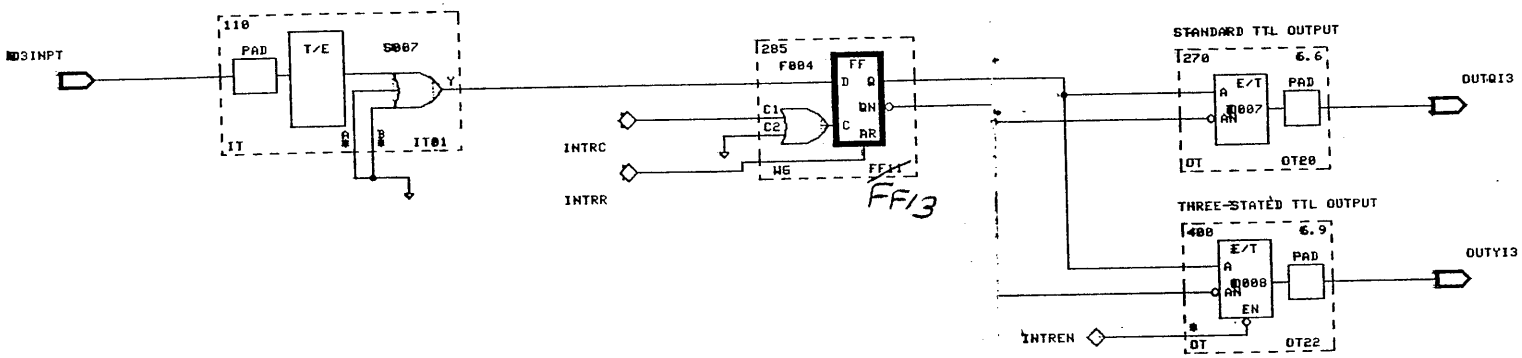
9-56

AMCC81500T		APPLIED MICRO CIRCUITS CORP
DRAWN	DATE	REGIS2 Am2918 CELL
		SHEET 2 OF 3 REV

25 OCT 84 14:24 /USER/DEN/JDTEMP/81SEXAM 2.DRAW



9-53



AMCCQ1500T	APPLIED MICRO CIRCUITS CORP
DRAWN / DATE	REGIS3 Am2918 CELL
	SHEET 3 OF 3 REV

Date/Time: 25-OCT-1984 14:38
Directory: /USER/DEW/JDTEMP/Q15EXAM/ERC
File: MACRO_TAB.DOC

NOTE: In the CURRENT CALCULATIONS TABLE, the subtotals columns will only contain values if the Icc and/or Iee totals will exceed 32Ø.ØØ mA. Addition is done in integer basic, and its range is <-32ØØØ,+32ØØØ> ,where for our purposes cannot exceed 32Ø.ØØ mA. Therefore, values in either subtotals column must be added manually.

TABLE OF MACRO OCCURENCES

INDEX	MACRO NAME	# OF OCCURENCES
1	~~FF11~~ FF13	4
2	ITØ1	6
3	IT18	1
4	OT2Ø	4
5	OT22	4

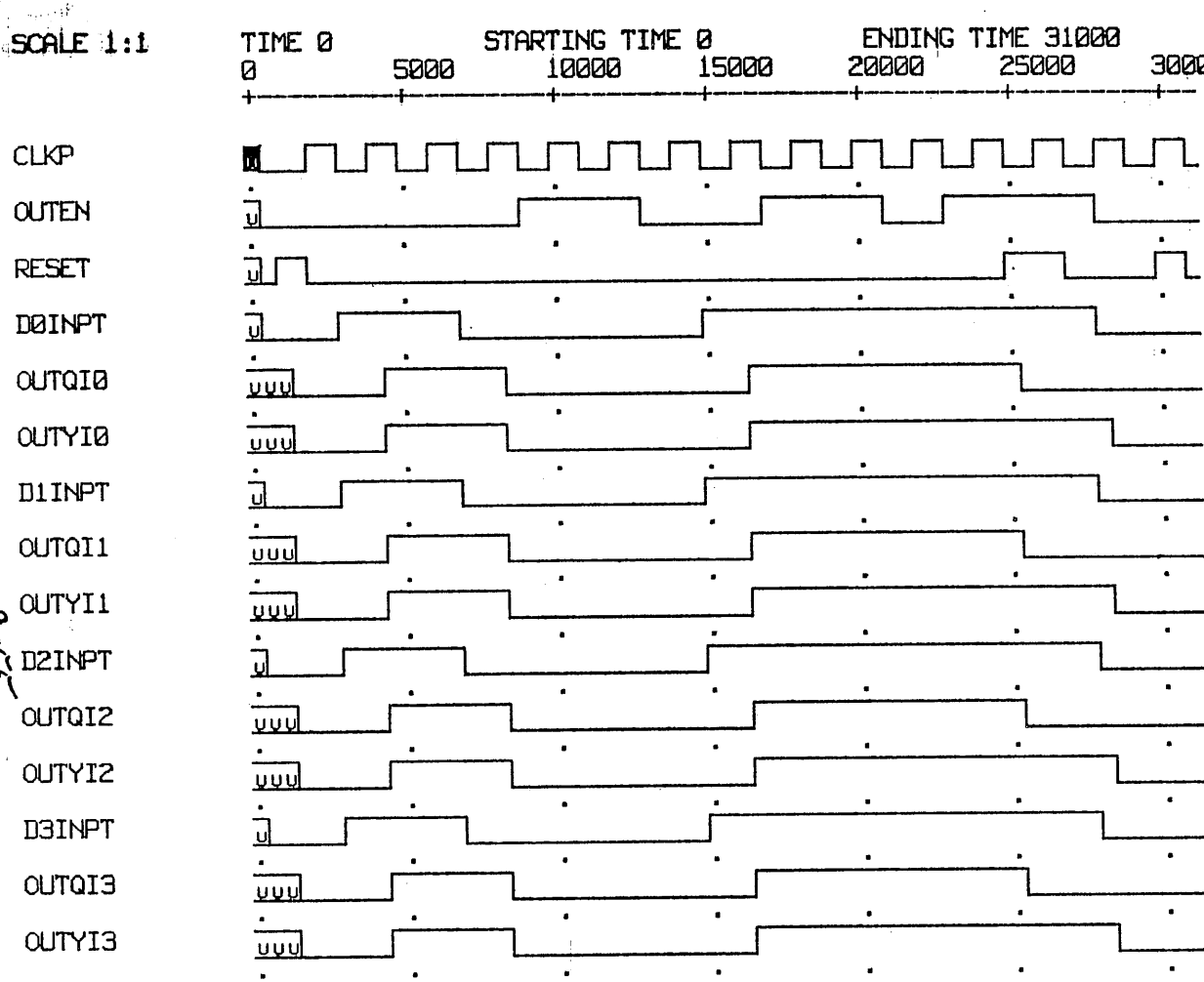
CELL TYPE	TOTAL
I/O	15
FUNCTION	4

CURRENT CALCULATIONS

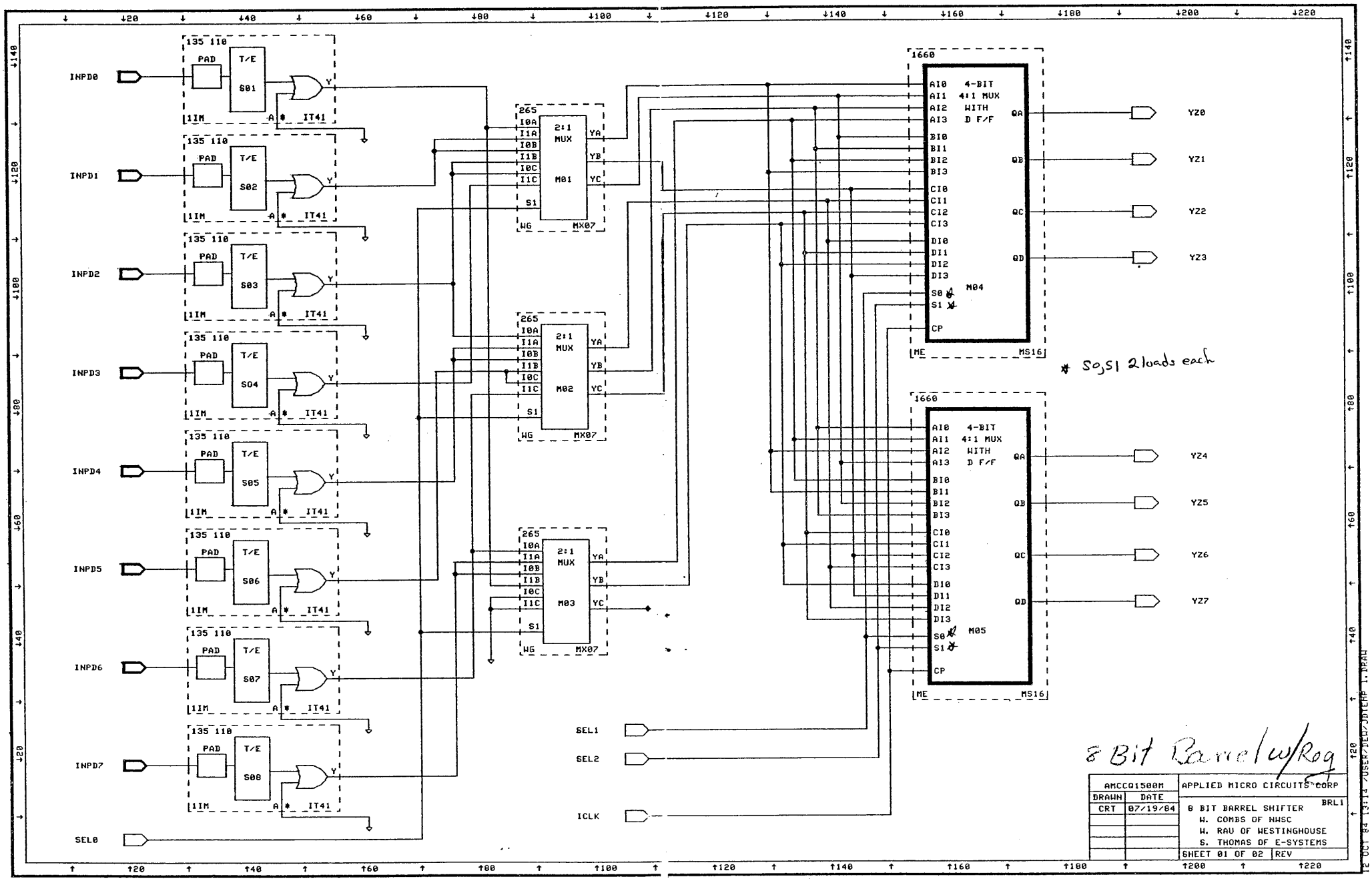
	SPECS		TOTAL		SUBTOTALS		POWER DEPENDS ON TERMINATION
	ICC	IEE	ICC	IEE	ICC	IEE	
	2.85		11.4Ø		.	.	
	1.1Ø		6.6Ø		.	.	
	5.3Ø		5.3Ø		.	.	
	2.7Ø		1Ø.8Ø		.	.	
	4.ØØ		16.ØØ		.	.	
XXXXXXXX	TOTALS		5Ø.1Ø		CALCULATE	CALCULATE	XXXXXXXXXXXXX

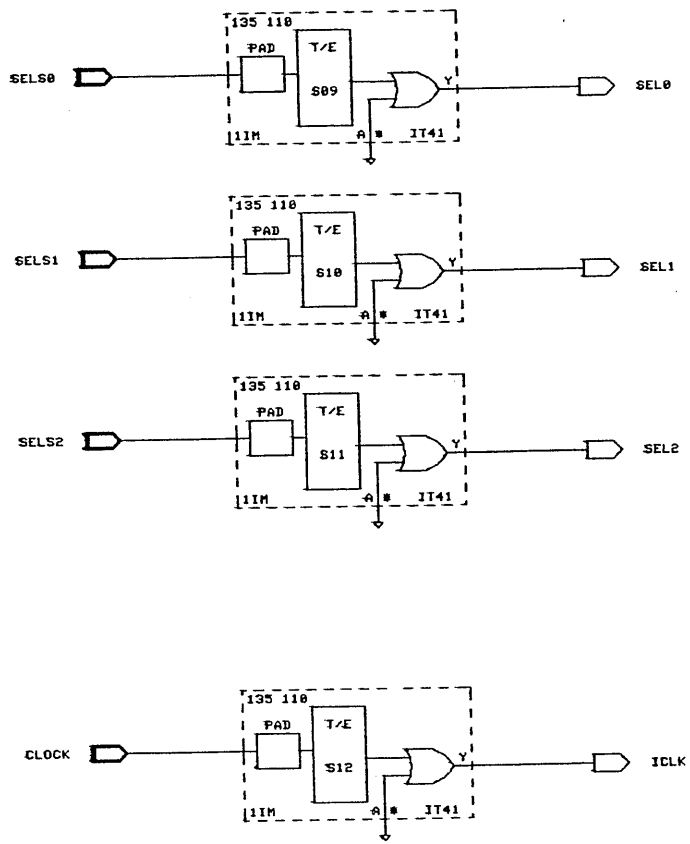
Calaulations for Icc and Iee subtotals:

1.5-6

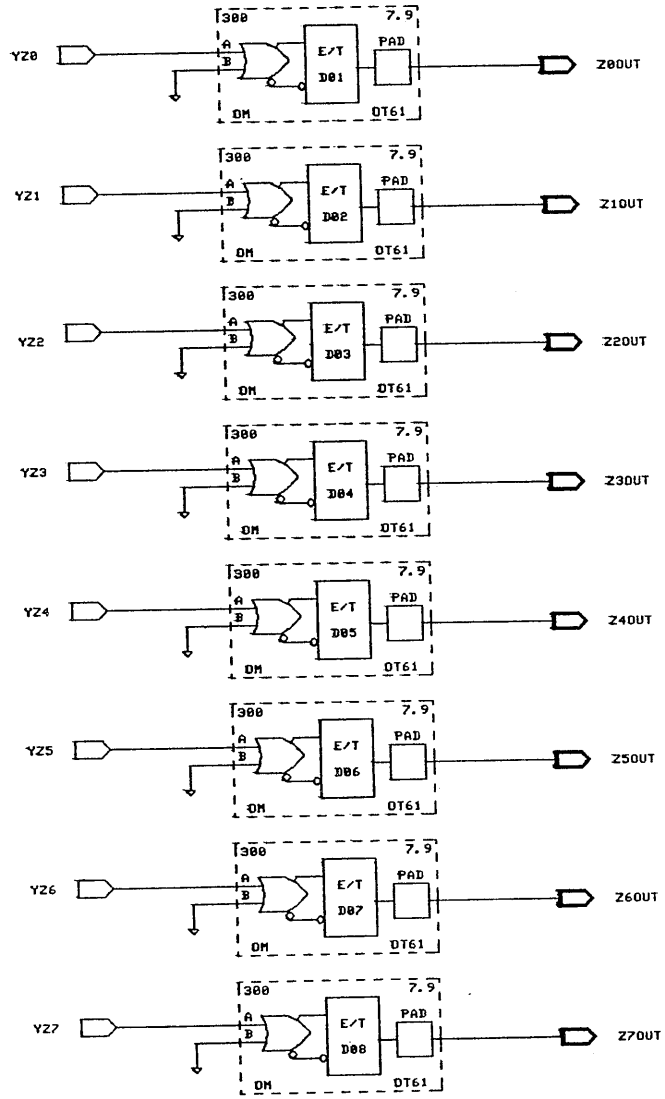



```
$T\
I/O
$FORMAT$
TIME_VALUE
$TOTAL_COLUMNS$
10 15
$BASE$
D B
$FIELD$ 1
@Q15EXAM 1:CLKP 1
$FIELD$ 2
@Q15EXAM 1:OUTEN 2
$FIELD$ 3
@Q15EXAM 1:RESET 3
$FIELD$ 4
@Q15EXAM 1:D0INPT 4
$FIELD$ 5
@Q15EXAM 2:D1INPT 5
$FIELD$ 6
@Q15EXAM 3:D2INPT 6
$FIELD$ 7
@Q15EXAM 3:D3INPT 7
$FIELD$ 8
@Q15EXAM 1:D001 8
$FIELD$ 9
@Q15EXAM 1:D002!PO 9
$FIELD$ 10
@Q15EXAM 2:D003 10
$FIELD$ 11
@Q15EXAM 2:D004!PO 11
$FIELD$ 12
@Q15EXAM 3:D005 12
$FIELD$ 13
@Q15EXAM 3:D006!PO 13
$FIELD$ 14
@Q15EXAM 3:D007 14
$FIELD$ 15
@Q15EXAM 3:D008!PO 15
$END$
0          00000000########
1000       00100000########
1128       00100000L!L!L!L!
1131       00100000LLLLLLLL
2000       10000000LLLLLLLL
3000       00011111LLLLLLLL
4000       10011111LLLLLLLL
4114       10011111L1L1L1L
4117       10011111111111
5000       00011111111111
6000       10011111111111
7000       00000000111111
8000       10000000111111
8114       10000000L1L1L1L1
8117       10000000LLLLLLLL
9000       01000000LLLLLLLL
9041       01000000L-L-L-L-
10000      11000000L-L-L-L-
11000      01000000L-L-L-L-
12000      11000000L-L-L-L-
13000      00000000L-L-L-L-
13110      00000000LLLLLLLL
14000      10000000LLLLLLLL
15000      00011111LLLLLLLL
16000      10011111LLLLLLLL
16114      10011111L1L1L1L
```


INPD0
INPD1
INPD2
INPD3
INPD4
INPD5
INPD6
INPD7
SEL0
SEL1
SEL2
ICLK
135 110
PAD
T/E
S01
S02
S03
S04
S05
S06
S07
S08
1IM
IT41
265
2:1
MUX
M01
M02
M03
MX07
1660
4-BIT
4:1 MUX
WITH
D F/F
M04
M05
MS16
YZ0
YZ1
YZ2
YZ3
YZ4
YZ5
YZ6
YZ7
S0,S1 2loads each
8 Bit Barrel w/Reg
AMCC01500M
APPLIED MICRO CIRCUITS CORP
DRAWN
DATE
CRT
07/19/84
8 BIT BARREL SHIFTER
W. COMBS OF NWSC
W. RAU OF WESTINGHOUSE
S. THOMAS OF E-SYSTEMS
SHEET 01 OF 02
REV
BRL1



TTL INPUTS FOR STANDARD MIXED-MODE CIRCUIT



TTL OUTPUTS FOR STANDARD MIXED-MODE CIRCUIT

AMCCQ1500M	
DRAWN	DATE
CRT	07/19/84

APPLIED MICRO CIRCUITS CORP

8 BIT BARREL SHIFTER BRL2

W. COMBS OF NSWC

W. RAU OF WESTINGHOUSE

S. THOMAS OF E-SYSTEMS

SHEET 02 OF 02 REV

9-57

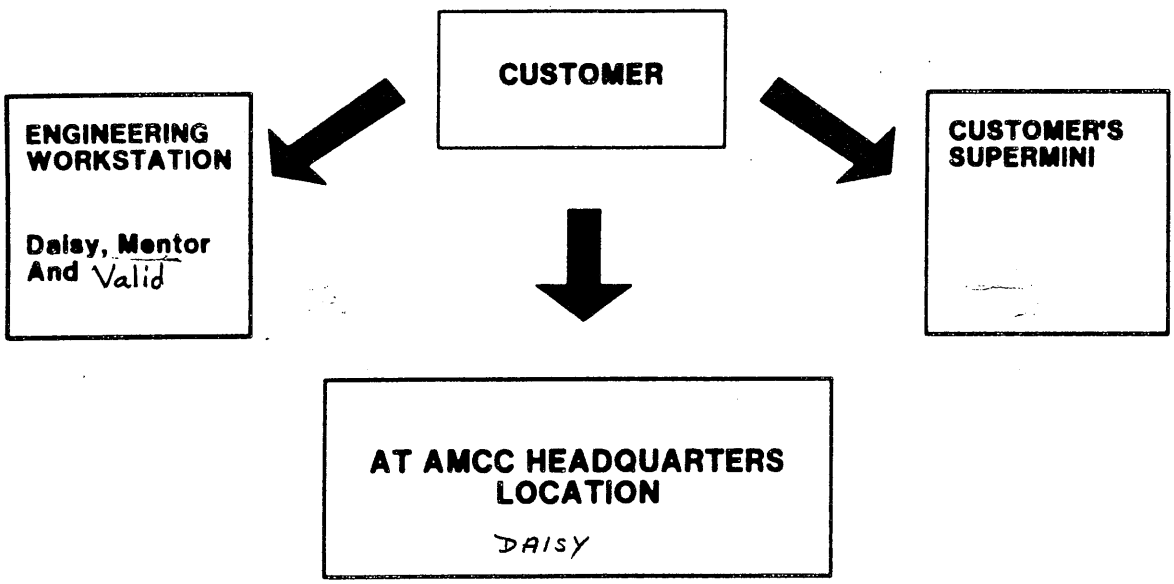
AMCC
APPLIED MICRO CIRCUITS CORPORATION

COMPUTER AIDED DESIGN

CHAP 10 - COMPUTER AIDED DESIGN - A-Z
Detailed look at the DAISY EWS steps
from schematic capture
through QUASAR
to wafer fab

AMCC
APPLIED MICRO CIRCUITS CORPORATION

FLEXIBLE COMPUTER-AIDED DESIGN



STEP 1:

- SPECIFICATION
- CONTRACT
- DECIDE WHAT IS TO BE DESIGNED
- WHICH ARRAY
- WHO IS DOING WHICH STEPS
- WHICH EWS or WHAT OTHER MEANS
- COMPLETION DATE
- ANY OTHER PRELIMINARY REVIEWS, ETC.
    - ESTIMATED PIN COUNT
    - ESTIMATED CELL UTILIZATION
    - REQUIRED SPEED
    - REQUIRED TESTING
    - ESTIMATED CRITICAL PATH
    - INITIAL DEFINITION OF TESTS

STEP 3:

- IDENTIFY NEEDED CUSTOM MACROS
- THESE WILL BE DEVELOPED BY AMCC
  AND ADDED TO THE DESIGN DATA BASE
  USING MEDIC - MACRO EDITOR

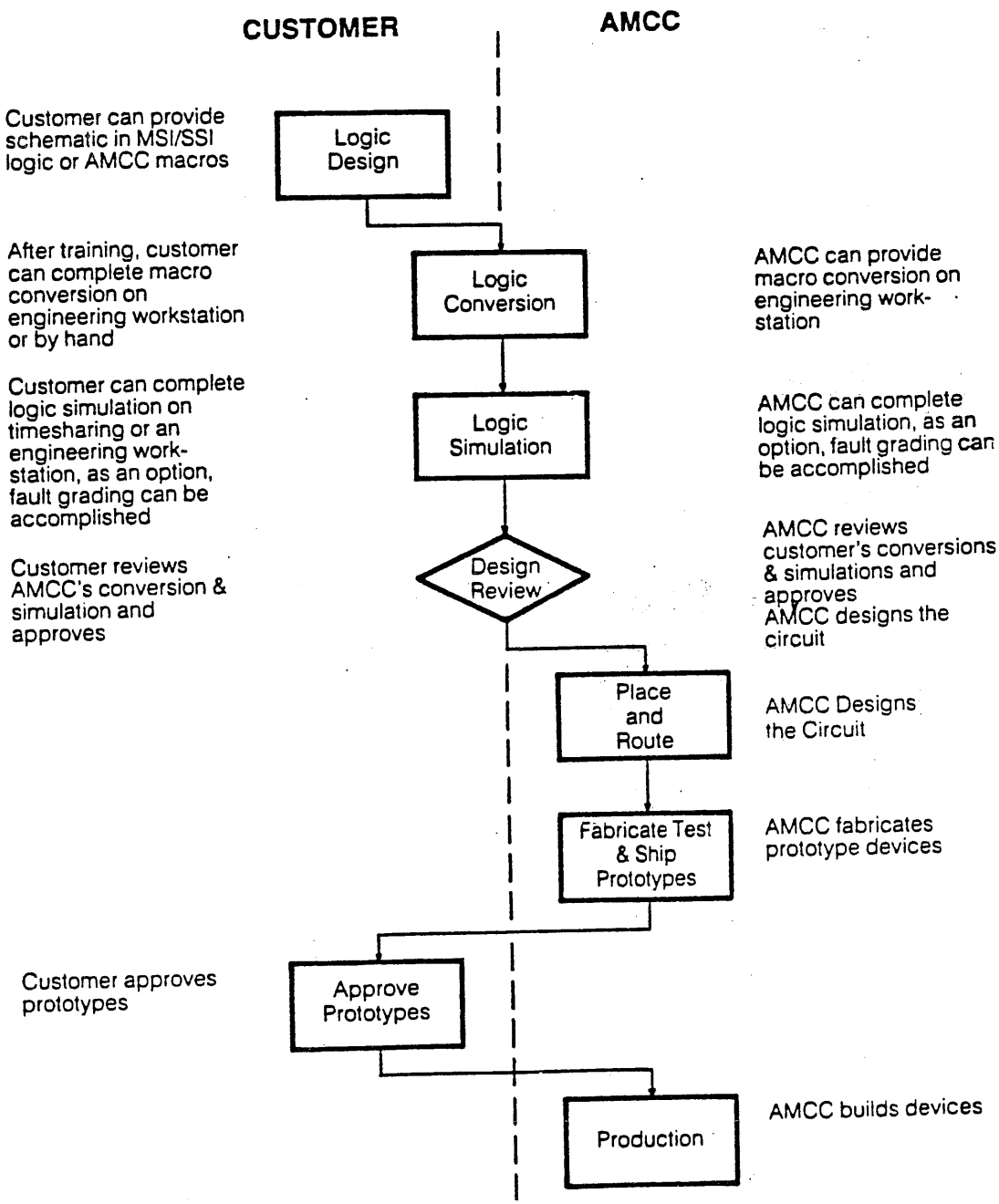
STEP 4:

- PERFORM SCHEMATIC CAPTURE
- IF ON AN EWS:
  - DAISY LOGICIAN
  - MENTOR - JUST COMING UP
  - VALID - LIBRARY UNDER DEVELOPMENT
- IF TEGAS NETLIST -

DESIGN INTERFACE AND SUPPORT

The AMCC circuit development interface has been structured to be highly flexible with respect to the customer's desired level of involvement. The basic steps are summarized below:

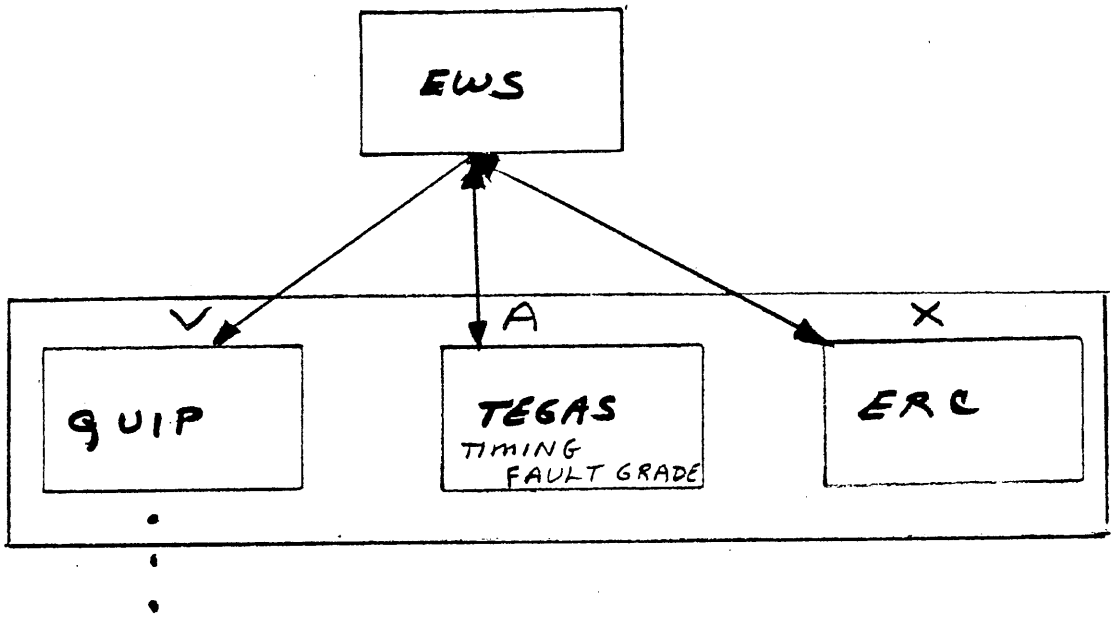
DEVELOPMENT INTERFACE



ASSUMING DAISY:

STEP 5:

- DANCE ON DAISY
- DRINK ON DAISY
- CREATE AGIF FILE ON DAISY
- ERC ON VAX
    - ERC OUTPUT INCLUDES TEGAS FILE
- SIFT ON DAISY
- SING ON DAISY
- EDIT SOM CONTROL FILE(S) ON DAISY
- CREATE DATA FILE(S), IF ANY
- EXECUTE SOM ON DAISY
- DLS ON DAISY
- DTV ON DAISY



AGIF → VAX
- FOR ERC SOFTWARE
- TEGAS FILE

AMCC
APPLIED MICRO CIRCUITS CORPORATION

STEP 6:

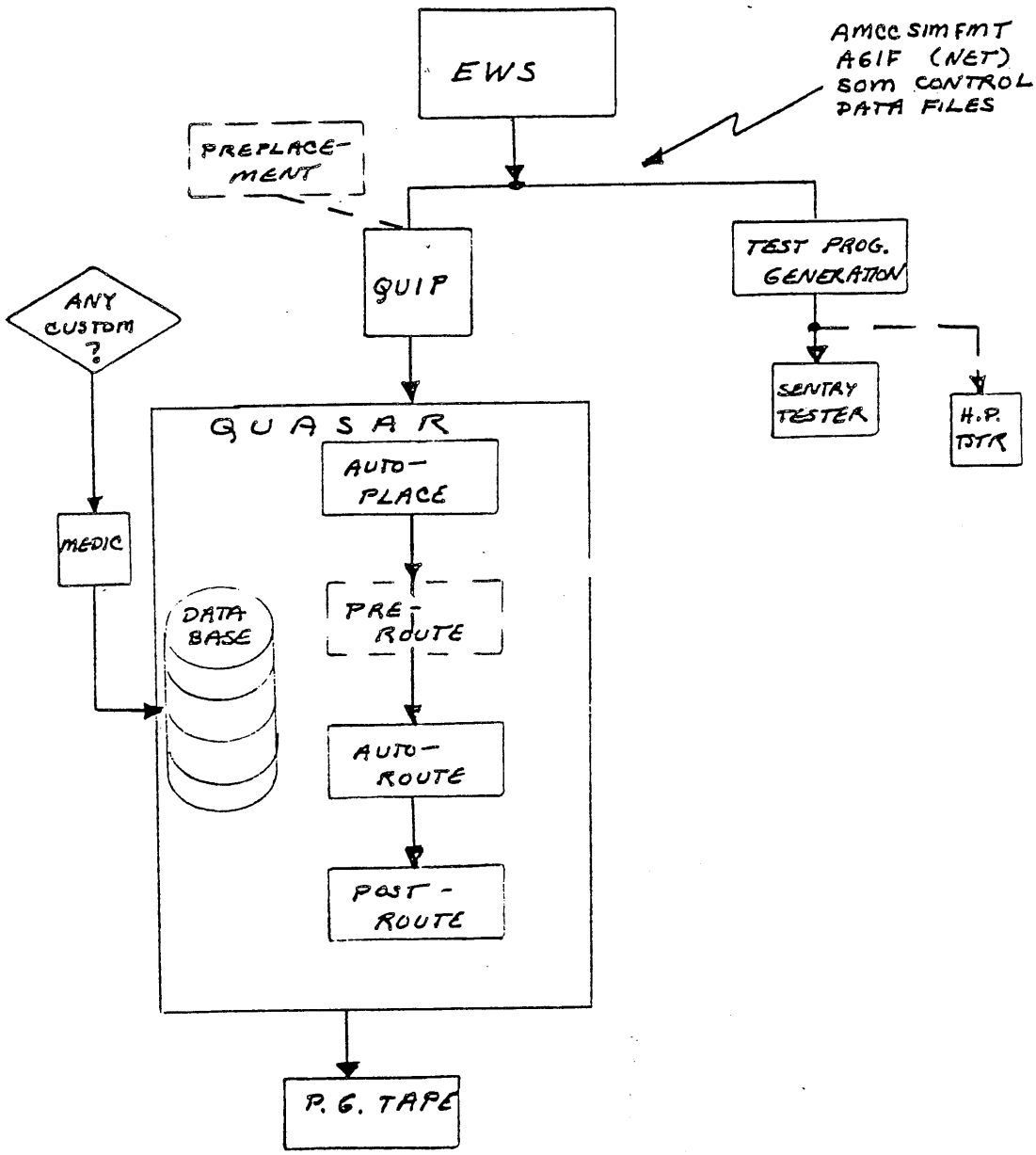
- DLS/DTV STEP INCLUDES THE CREATION OF THE AMCCSIMFMT TEST FILE(S)
- SUBMIT THESE TO AMCC FOR SUBMISSION TO TEST
    - PIN/PAD DIAGRAM (PIN-OUT)
    - AGIF FILE
    - SOM CONTROL FILE(S)
    - DATA SOURCE FILE(S)
    - AMCCSIMFMT OUTPUT FILE(S)
    - TEST INSTRUCTIONS
    - ADDITIONAL TESTS (AC, ETC)
    - ANY OTHER PERTINENT TESTING INFORMATION
    - AMCC ENGINEERING/AMCC ACCOUNT MANAGER WILL COORDINATE THE P.I.F (PROJECT INFORMATION FILE)

STEP 7:

- SUBMIT PREPLACEMENT, IF ANY
- EWS OUTPUT TRANSFERS TO THE VAX FOR THE NEXT STEP

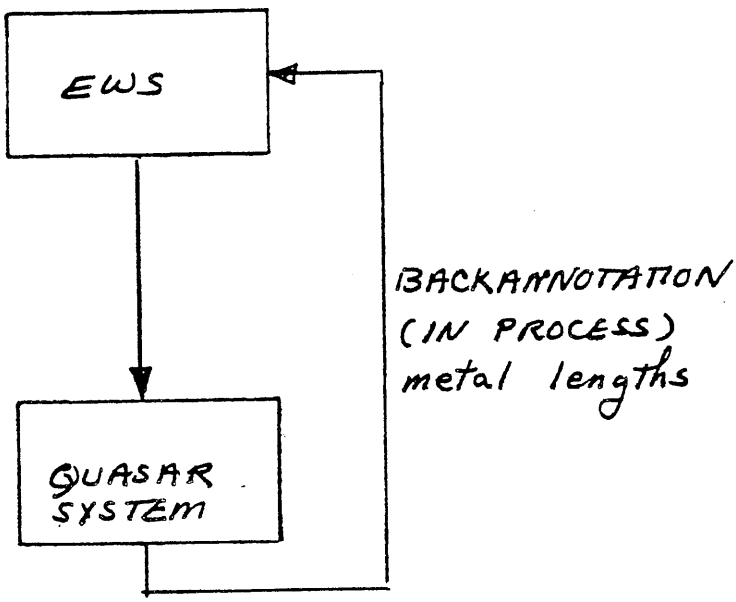
STEP 8:

- QUIP - QUASAR INPUT PROCESSOR
  - INTEGRATES THE EWS OUTPUT FILE AND THE PREPLACEMENT INFORMATION
  - PREPARES DATA FOR QUASAR RUN

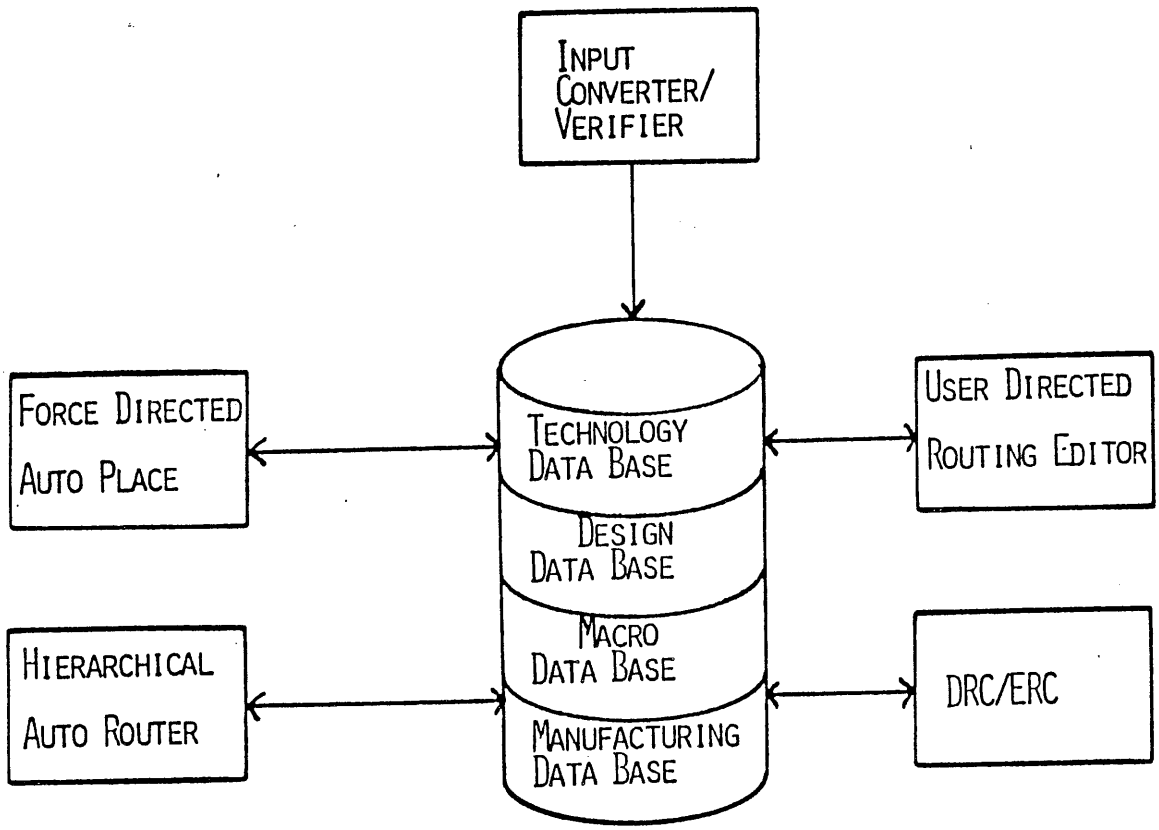

EWS
AMCC SIM FMT
A61F (NET)
SOM CONTROL
DATA FILES
PREPLACE-
MENT
QUIP
TEST PROG.
GENERATION
ANY
CUSTOM
?
SENTRY
TESTER
H.P.
TSTR
QUASAR
AUTO-
PLACE
MEDIC
DATA
BASE
PRE-
ROUTE
AUTO-
ROUTE
POST-
ROUTE
P. G. TAPE

STEP 9:

- QUASAR
  - AUTOPLACE RUN
  - IF ANY PRE-ROUTING, ADDED HERE
  - AUTOROUTE RUN
  - POST-ROUTING, IF ANY, DONE HERE
- WORKS FROM THE SYSTEM DATABASE
  - MACROS AND THEIR RELATED FILES
  - REQUIRES THAT ANY CUSTOM MACRO EXIST ON THE DATABASE
- DRC - DESIGN RULE CHECKS - INCORPORATED IN THE QUASAR SOFTWARE
  - DESIGN BY CORRECTNESS

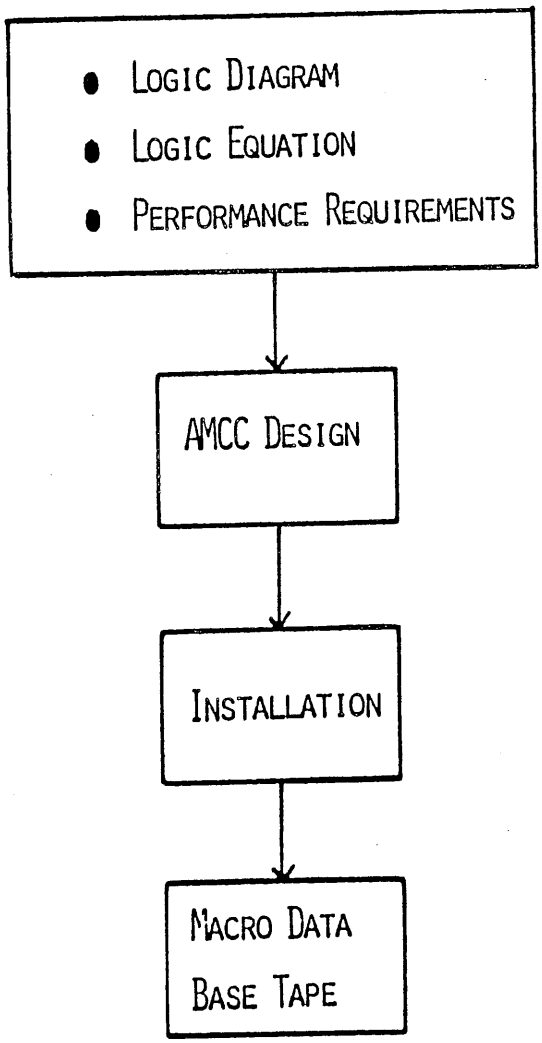

EWS
QUASAR SYSTEM
BACKANNOTATION
(IN PROCESS)
metal lengths

AUTOMATIC LAYOUT SOFTWARE



AMCC
APPLIED MICRO CIRCUITS CORPORATION

CUSTOM MACROS



IF OK,

- THE MASK VENDOR GENERATES THE RETICLE, THE ACTUAL 3 LAYERS (METAL 1; VIA; AND METAL 2)

IF OK,

- MAKE THE MASKS
- WAFER FAB
- TEST SORT

IF OK,

- ASSEMBLY
- FINAL TEST AND QA
- SHIP

COMMITMENT TO QUALITY